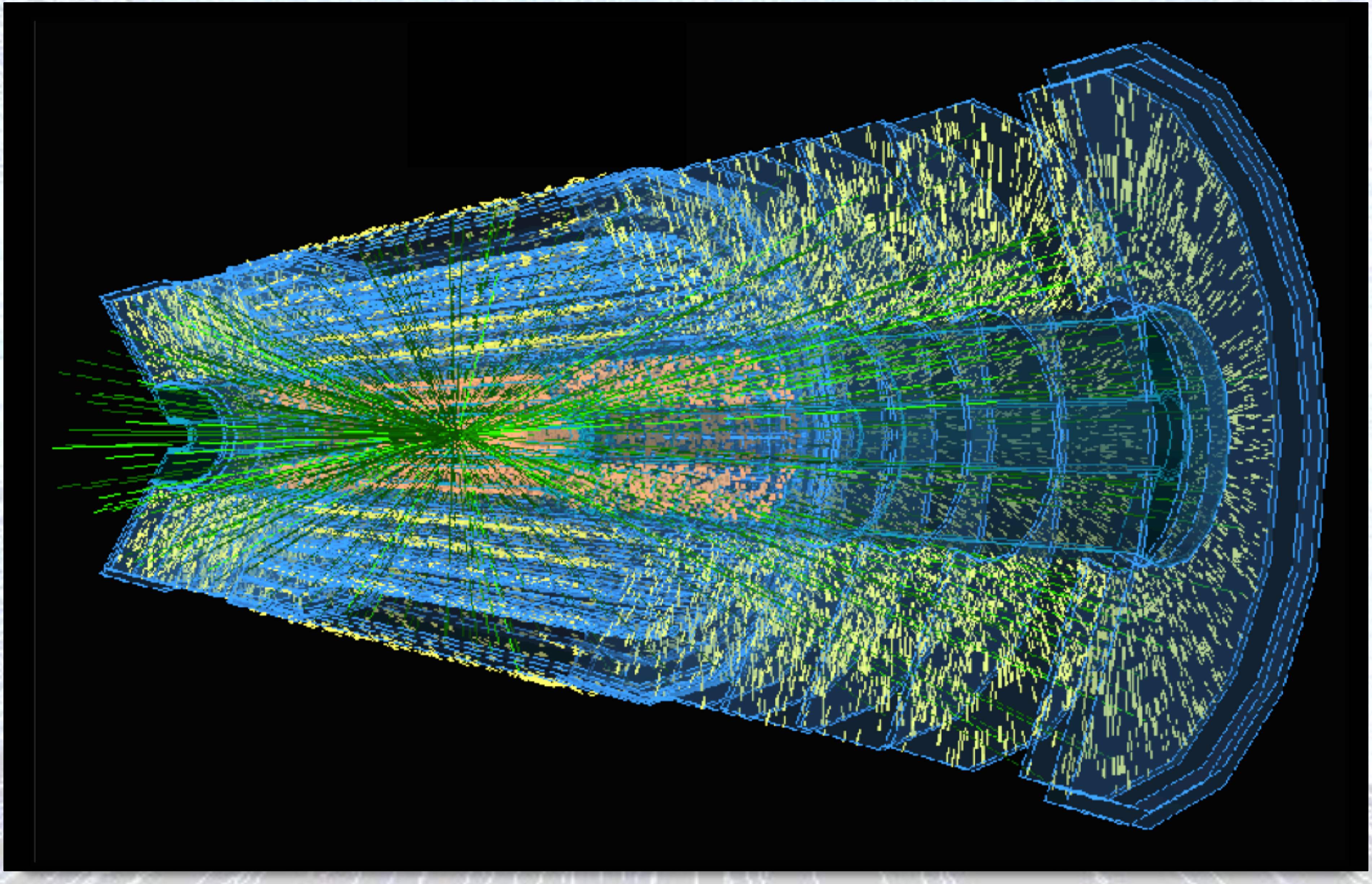
ATLAS upgrade

Theodore Todorov

21/03/2013



LHC Time-line (CERN DG at ICHEP 2012)

2009

Start of LHC

Run 1: 7 and 8 TeV centre of mass energy, luminosity ramping up to few 10^{33} cm^{-2} s^{-1}, few fb^{-1} delivered

LS1
Phase 0
Upgrade

2013/14

LHC shut-down to prepare machine for design energy and nominal luminosity

Run 2: Ramp up luminosity to nominal (10^{34} cm^{-2} s^{-1}), ~50 to 100 fb^{-1}

(Could already go further so need some headroom)

LS2
Phase I
Upgrade

2018

Injector and LHC Phase-I upgrades to go to ultimate luminosity

Run 3: Ramp up luminosity to 2.2 x nominal, reaching ~100 fb^{-1} / year accumulate few hundred fb^{-1}

(We assume up to 3×10^{34}cm^{-2}s^{-1} and 25ns, so should plan for μ up to 81)

LS3
Phase II
Upgrade

~2022

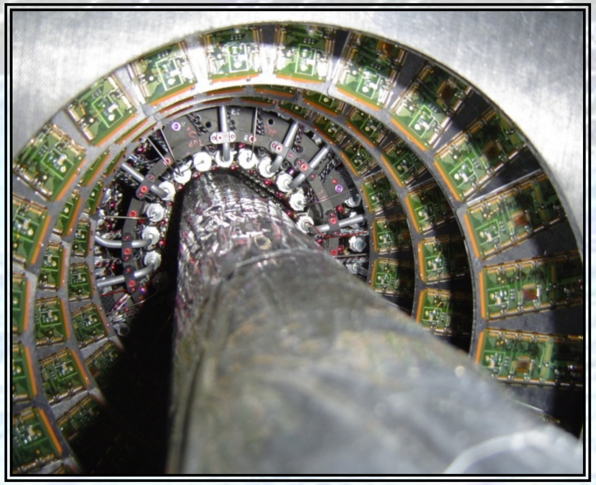
Phase-II: High-luminosity LHC. New focussing magnets for very high luminosity with levelling

Run 4: Collect data until > 3000 fb^{-1}

2030

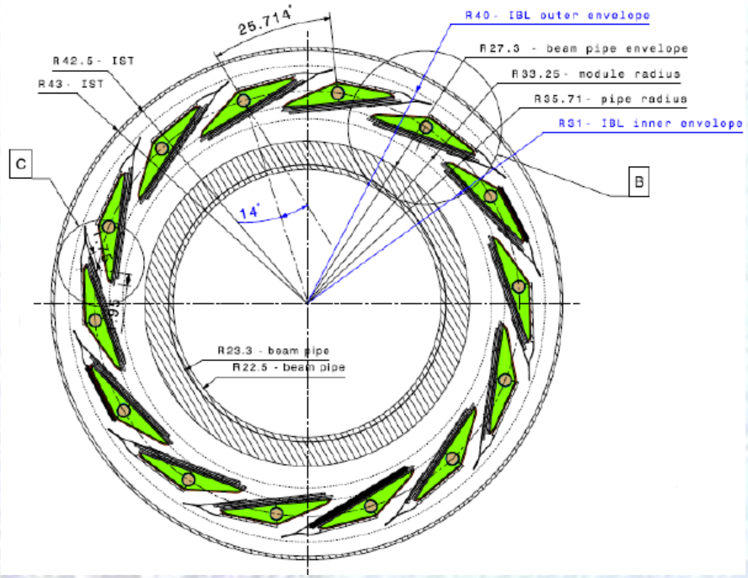
The ATLAS Upgrades

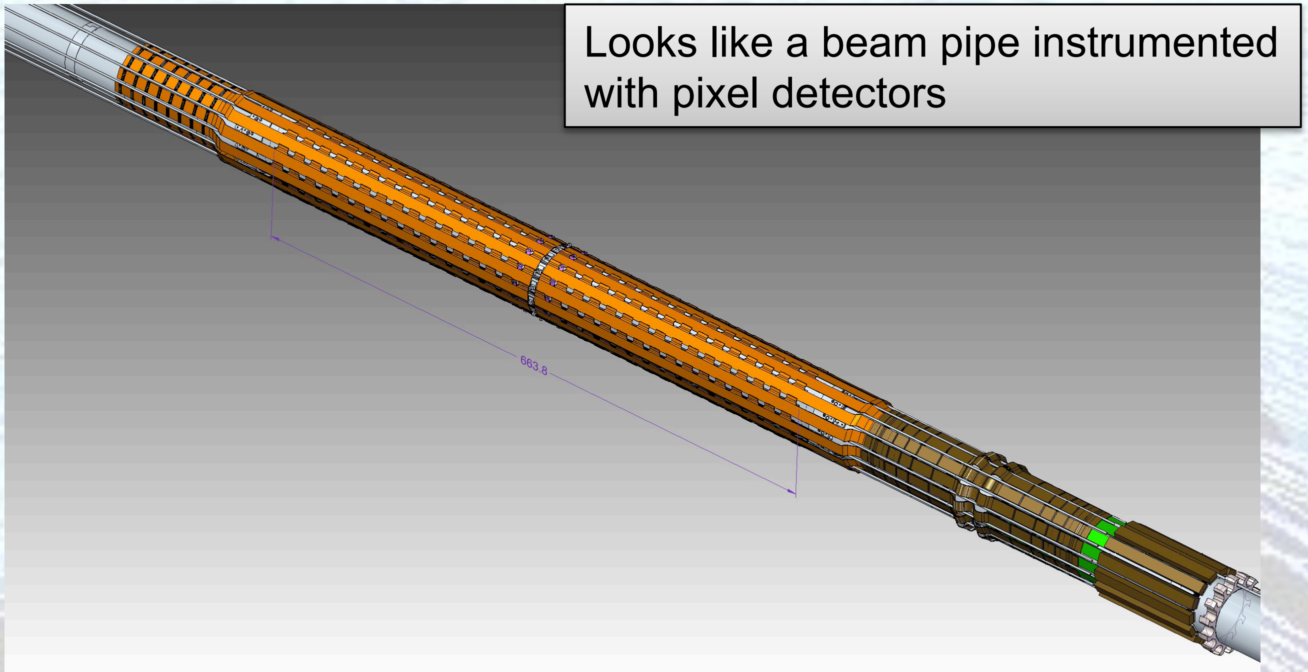
- Three distinct upgrade periods
  - Phase 0 (2013-2014) Now!
  - Phase I (~2018)
  - Phase II (~2022)
- Too many things will be upgraded to describe in this presentation
  - Will focus on a few main items



Insertable B Layer

- 4th pixel layer closer to the IP
- Robust tracking in case of present pixel failures
- New front end chip
  - Reduced inefficiency at high pile-up
- Finer Z pitch, less material, smaller R
  - improved performance
- 14 “staves”, 42 institutes – big R&D effort
- Proving ground for future upgrade concepts

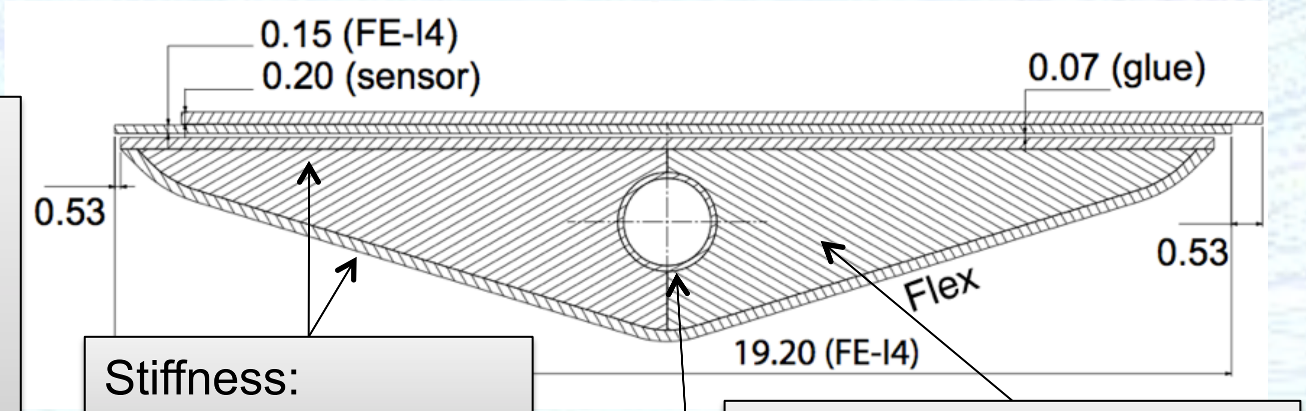




Looks like a beam pipe instrumented with pixel detectors

The IBL stave concept

Self-supporting structure provides
- mechanical support over ~70cm
- high performance cooling
    - coolant – sensor deltaT ~12^{o}
- electrical services via glued flex for the pixel modules

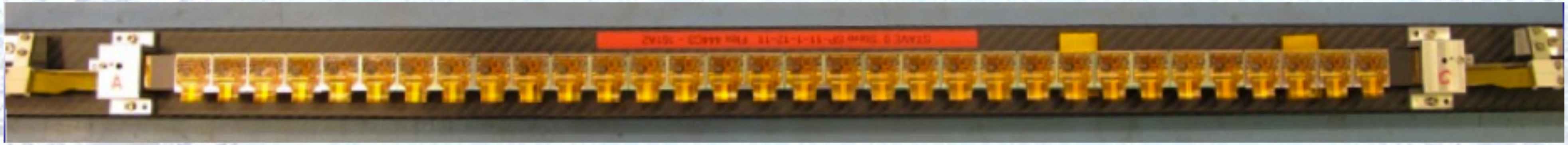


Stiffness:
Carbon fibre skin

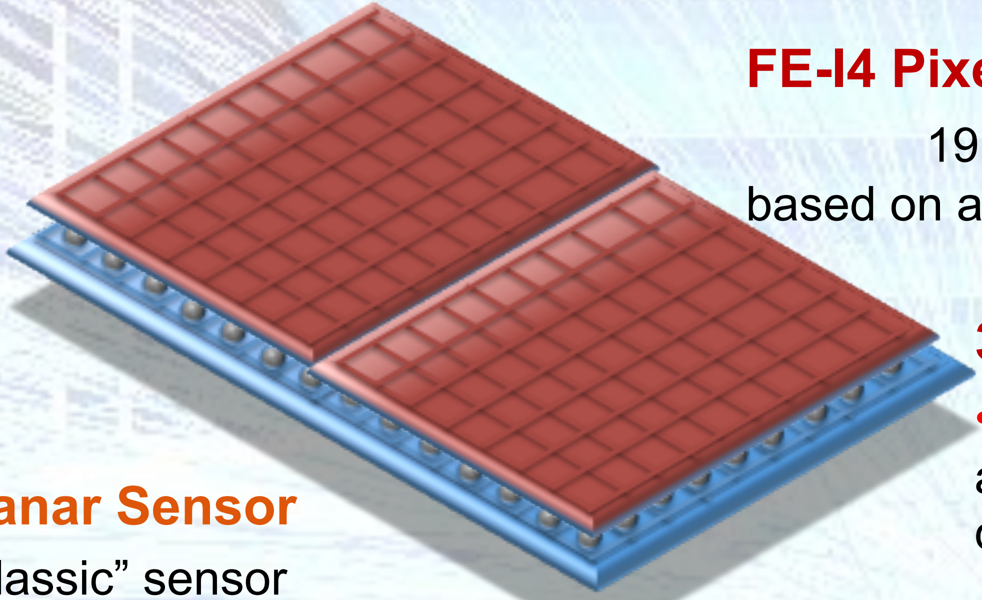
Heat transport:
Low density C foam

Cooling:
2-phase CO2 in thin Ti pipe

~0.50 % X/X_0 material in the mechanical stave

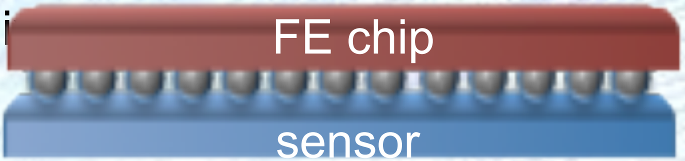


Insertable B-Layer



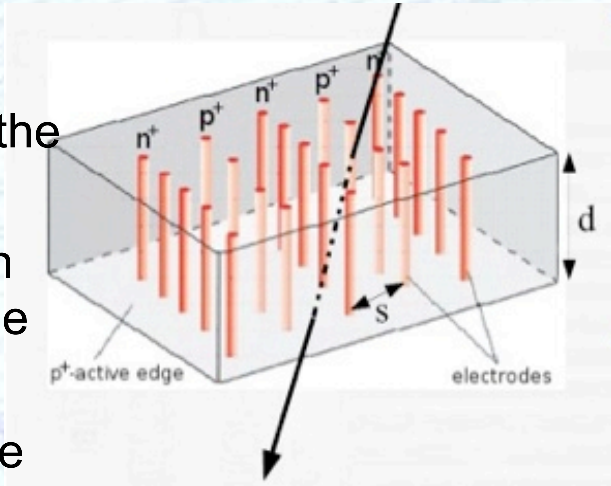
FE-I4 Pixel Chip (26880 channels)

19 x 20 mm^2 130 nm CMOS process, based on an array of 80 by 336 pi (each 50 x 250 µm^2)



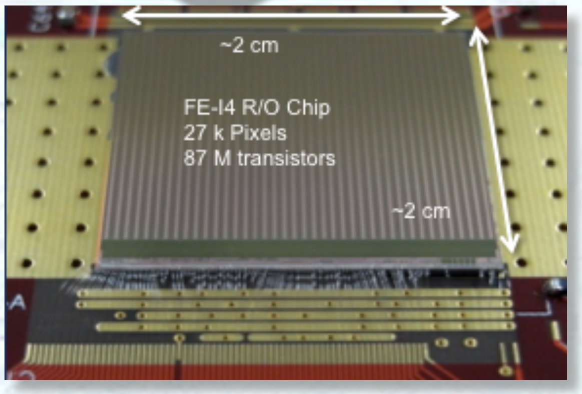
3D Sensor

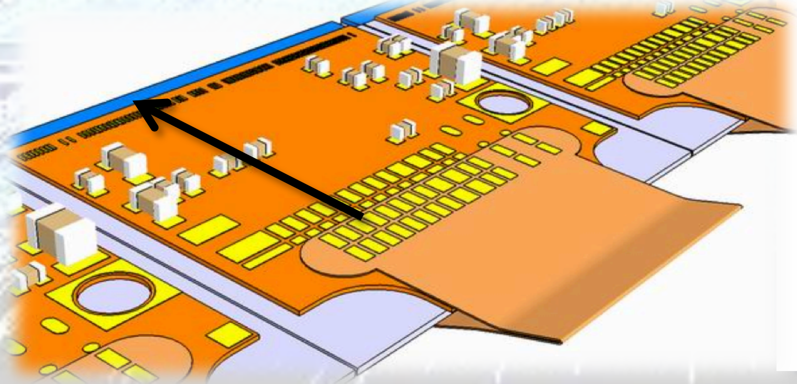
- Both electrode types are processed inside the detector bulk
- Max. drift and depletion distance set by electrode spacing
- Reduced collection time and depletion voltage

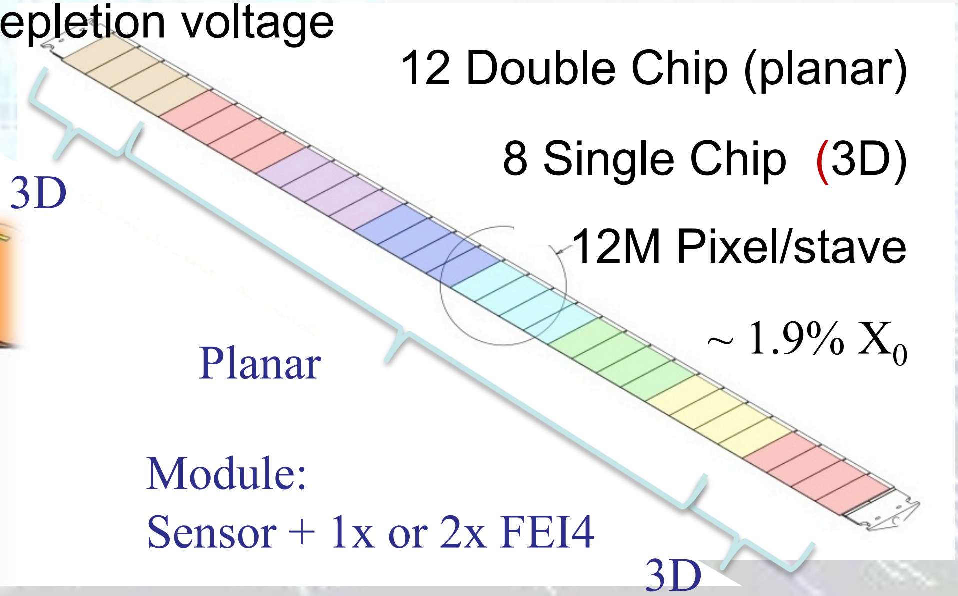


Planar Sensor

- “classic” sensor design
- oxygenated n-in-n
- 200µm thick
- Minimize inactive edge by shifting guard-ring under pixels (215 µm)
- Radiation hardness proven up to 2.4×10^{16} p/cm^2







12 Double Chip (planar)

8 Single Chip (3D)

12M Pixel/stave

~ 1.9% X_0

Module:
Sensor + 1x or 2x FEI4

2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	…	2030
Prepare for:		Phase 0,I		**LS1**			Phase I,II		**LS2**		Phase II		**LS3**			

“Phase-0” upgrade: consolidation
$\sqrt{s}$ = 13~14 TeV, 25ns bunch spacing
$L_{inst} \simeq 1 \times 10^{34}\ cm^{-2}s^{-1}$ ($\mu \simeq 27.5$)
$\int L_{inst} \simeq 50\ fb^{-1}$

“Phase-I” upgrades:
ultimate luminosity
$L_{inst} \simeq 2\text{-}3 \times 10^{34}\ cm^{-2}s^{-1}$ ($\mu \simeq 55\text{-}81$)
$\int L_{inst} \gtrsim 350\ fb^{-1}$

“Phase-II” upgrades:
$L_{inst} \simeq 5 \times 10^{34}\ cm^{-2}s^{-1}$ ($\mu \simeq 140$) w. leveling
$\simeq 6\text{-}7 \times 10^{34}\ cm^{-2}s^{-1}$ ($\mu \simeq 192$) no level.
$\int L_{inst} \simeq 3000\ fb^{-1}$

ATLAS has devised a 3 stage upgrade program to optimize the physics reach at each Phase

- New Insertable pixel b-layer (IBL)
- New Al beam pipe
- New pixel services
- New evaporative cooling plant
- Consolidation of detector elements (e.g. calorimeter power supplies)
- Add specific neutron shielding
- Finish installation of EE muon chambers staged in 2003
- Upgrade magnet cryogenics

- New Small Wheel (nSW) for the forward muon Spectrometer
- High Precision Calorimeter Trigger at Level-1
- Fast TracKing (FTK) for the Level-2 trigger
- Topological Level-1 trigger processors
- New forward diffractive physics detectors (AFP)

- All new Tracking Detector
- Calorimeter electronics upgrades
- Upgrade part of the muon system
- Possible Level-1 track trigger
- Possible changes to the forward calorimeters

M. Nessi (29 October 2012 RRB)
https://indico.cern.ch/conferenceOtherViews.py?confId=204539&view=lhcrrb&showDate=all&showSession=1&detailLevel=contribution

What *can* be upgraded

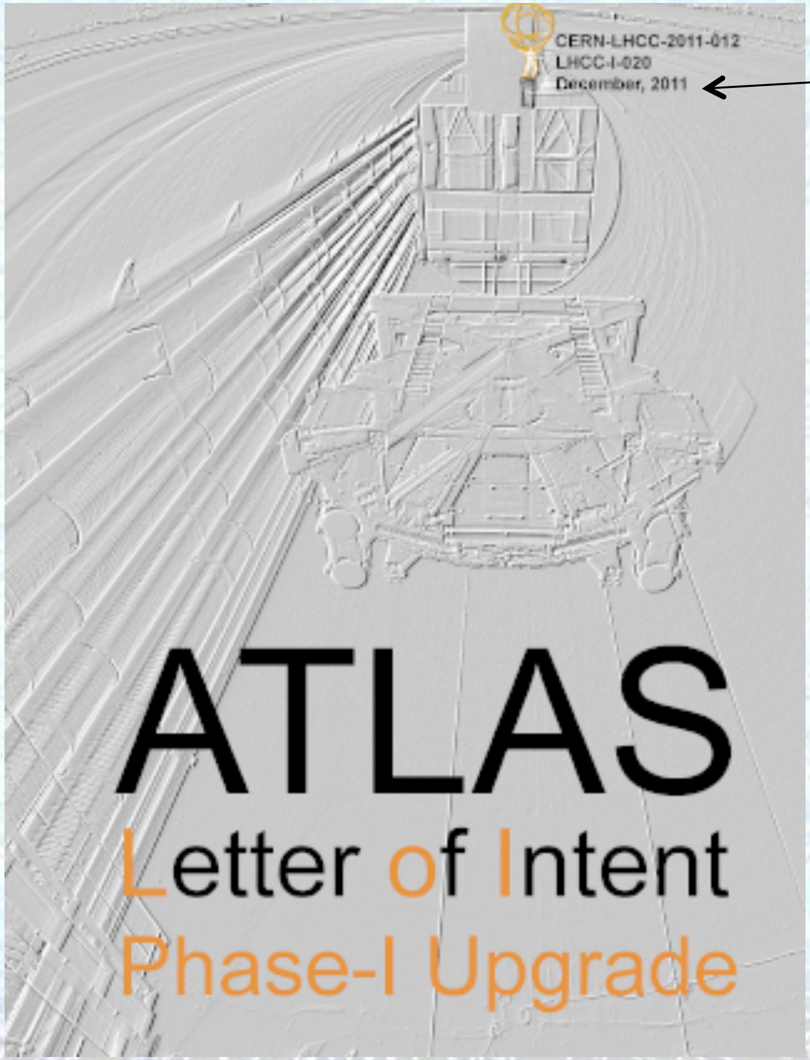
Photo of installation of part of the current Inner Detector in ATLAS

Only “small” parts of the detector, like the Inner Detector (tracker), can be replaced

The magnetic field system (toroids, solenoid) cannot be changed

Not possible to access all muon chambers in ~ 2 years

Phase-I



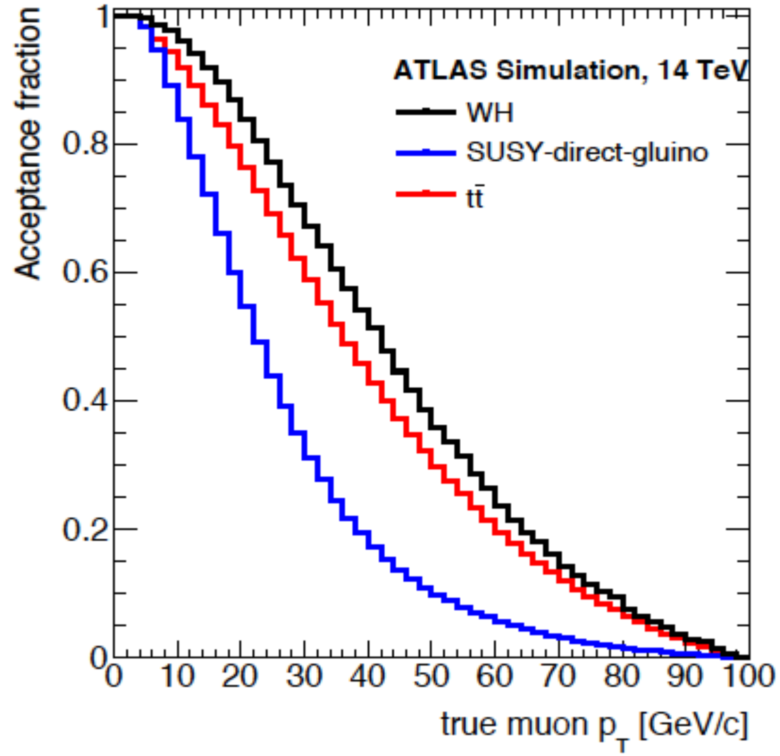
CERN-LHCC-2011-012
LHCC-I-020
December, 2011

ATLAS
Letter of Intent
Phase-I Upgrade

December2011

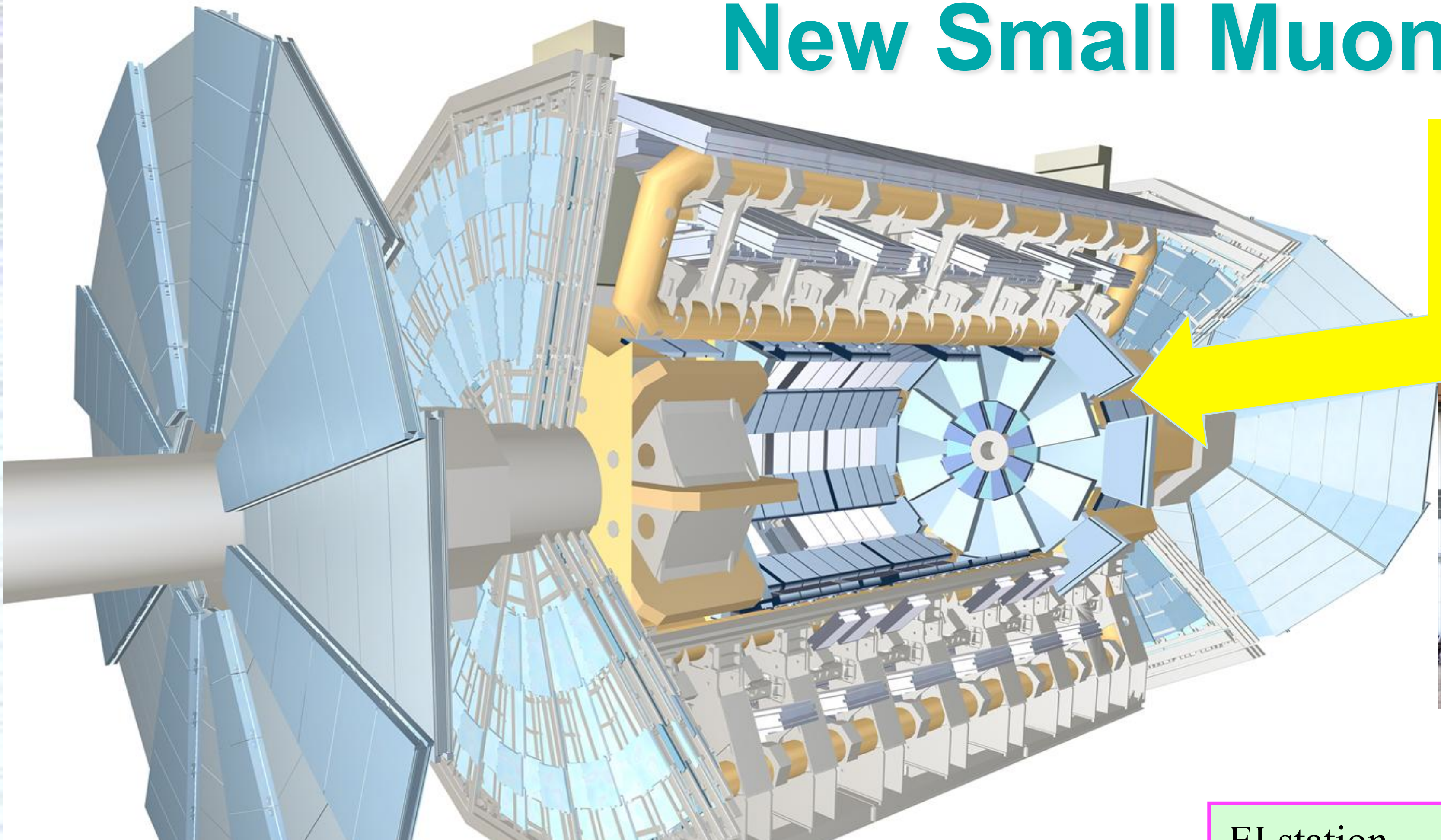
Retaining Low P_T Thresholds at Phase-I

- For a L1 rate upper limit of 100kHz until Phase-II, the impact of high luminosity is to require combinations of higher thresholds, pre-scaling, multi-object/topological triggering unless improved precision information can be made available to L1 (since backgrounds primarily from mis-measured lower P_T objects)
- Target single lepton rates each ≤~20kHz at P_T ~20 GeV as indicative of required performance to retain good sensitivity to key channels (such as those including vector bosons, like WH, WW, searches etc)
- Leads to main motivation to improve the detector resolution and background rejection in the key detector systems proving inputs to L1 in ATLAS



Acceptance vs muon momentum threshold

New Small Muon Wheels

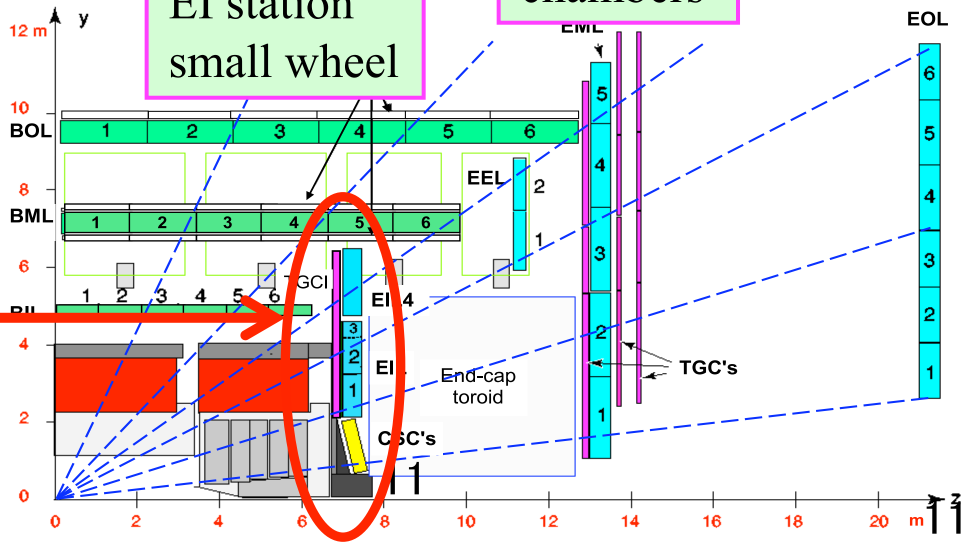


The innermost station of the muon end-cap

Located between end-cap calorimeter and toroid

EI station small wheel

L1 trigger chambers

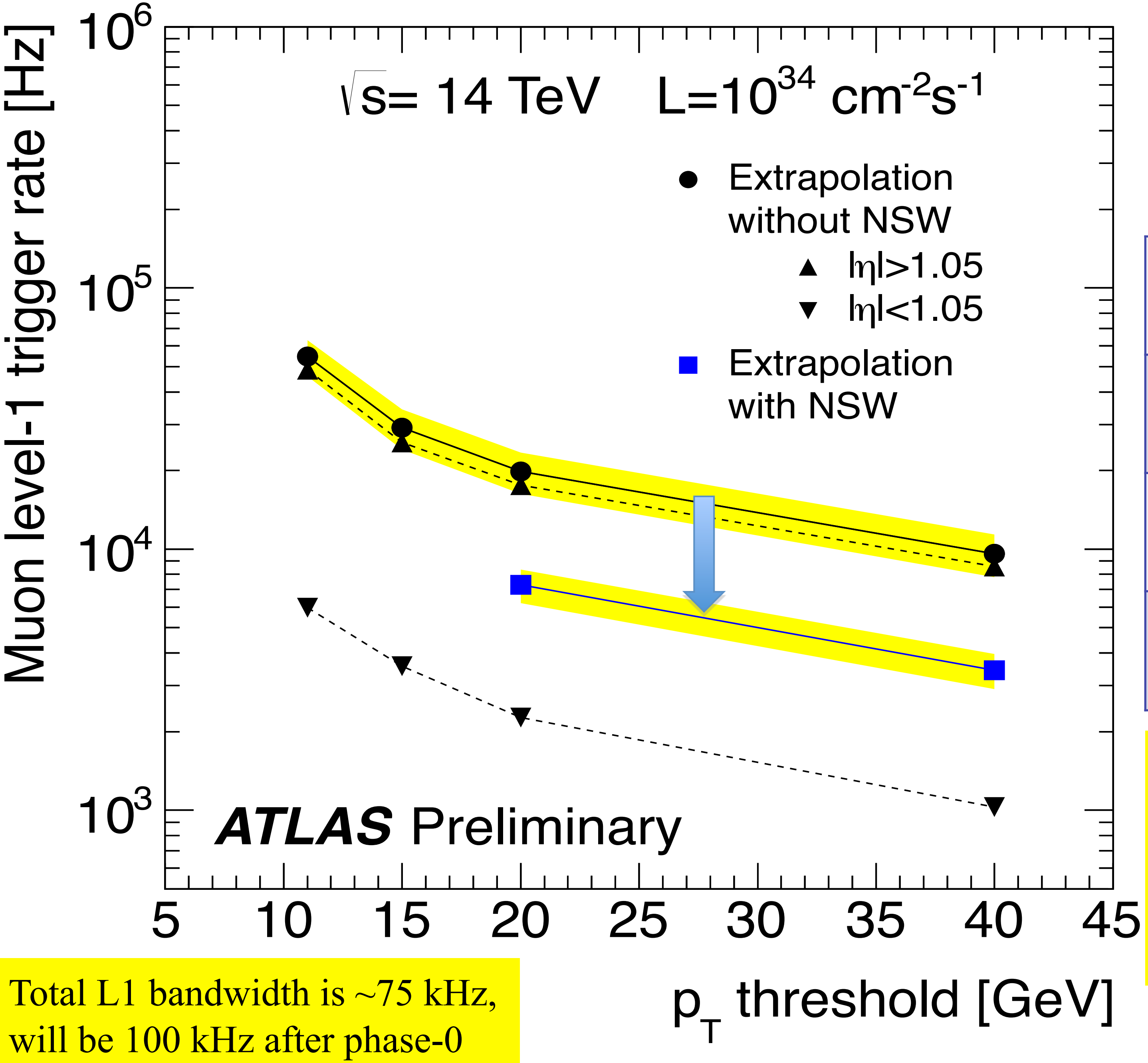


- In furthest forward direction, chamber efficiencies fall with hit rate as luminosity goes well above the design values
- Rate of L1 muon triggers exceeds available bandwidth unless thresholds raised

→ Replace "small" muon wheels

- Kill fake muon triggers by requiring high quality (σ_θ~ 1mrad) pointing to interaction region
- Precision chambers combine sTGC and micromegas technologies for robustness to Phase-II luminosities

Extrapolated L1 Rate (14 TeV, 25ns)



Total L1 bandwidth is ~75 kHz,
will be 100 kHz after phase-0

At L = 3x10^{34}

Single μ L1 rate (kHz)

	Mu20	**Mu40**
Without NSW	60	29
With NSW	22	10
NSW + phase-0	17	8

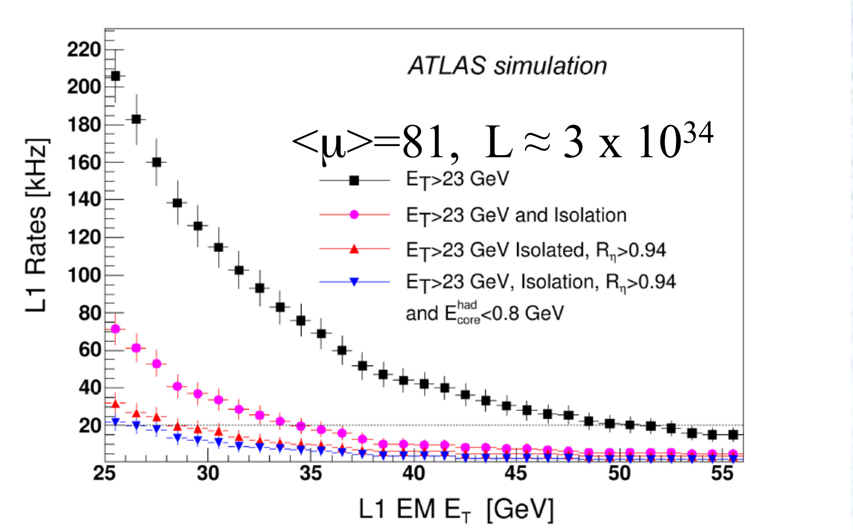
NSW is vital for running at high luminosity.

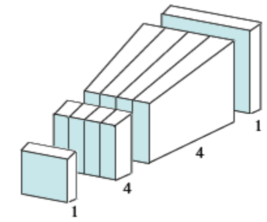
Allowing low p_T thresholds

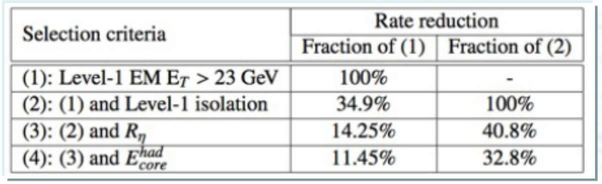
LAr Electronics and TDAQ Upgrades

- Key target (as for New Small Wheel) is to maintain high efficiency for Level-1 triggering on low P_T objects (here electrons and photons)
- In the LAr calorimeter this implies changes to the front-end electronics to allow greater granularity to be exploited at Level-1.
- Trigger upgrades include topological trigger, cluster and jet energy processor, feature extractors, muon sector logic and CTP

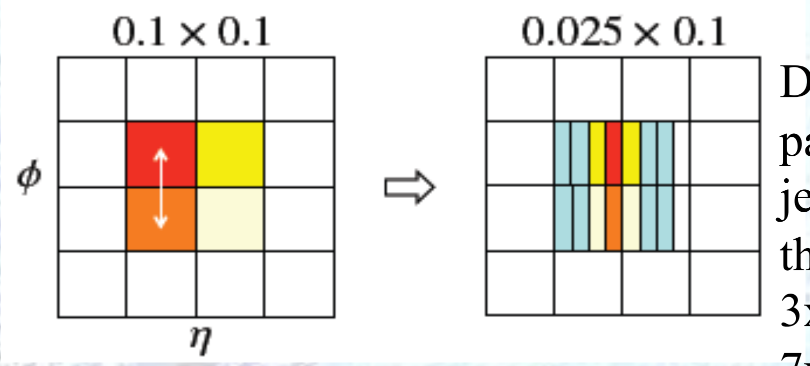
electron rate vs threshold



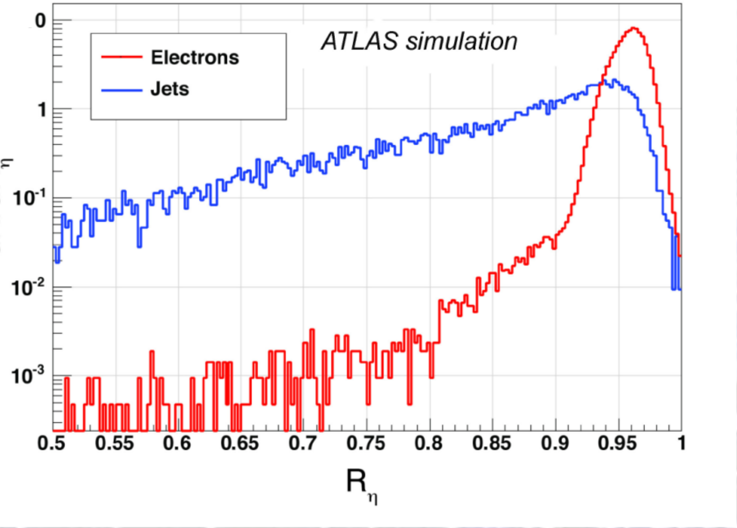




Selection criteria	Rate reduction	
	Fraction of (1)	Fraction of (2)
(1): Level-1 EM $E_T > 23$ GeV	100%	-
(2): (1) and Level-1 isolation	34.9%	100%
(3): (2) and R_η	14.25%	40.8%
(4): (3) and E_{core}^{had}	11.45%	32.8%



Distribution of the R_η parameter for electrons and jets, defined as the ratio of the energy in the 3x2 over the energy in the 7x2 clusters of the 2nd layer of the EM calorimeter.

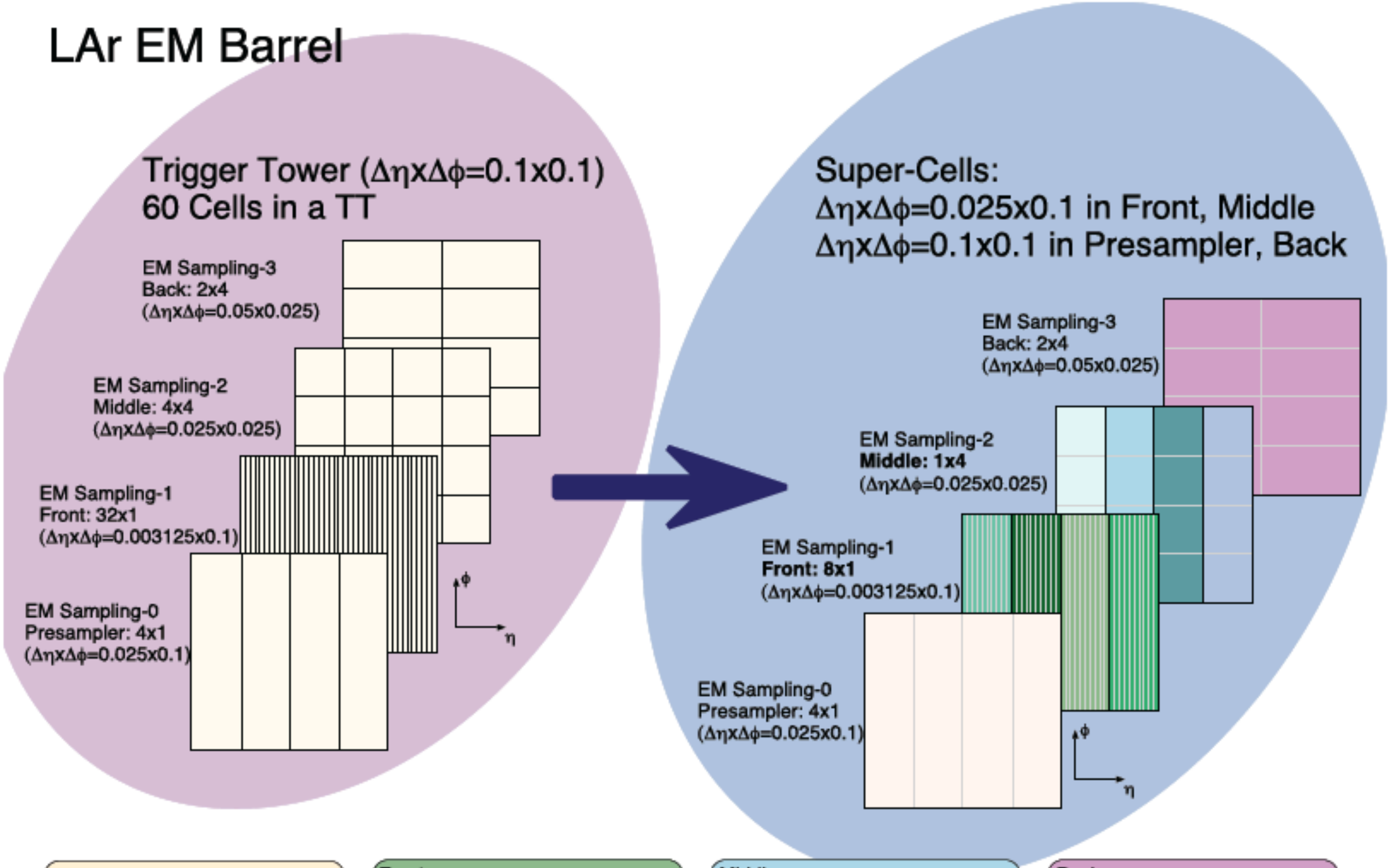


Increased segmentation

One Trigger Tower

↓

Ten Super-Cells
- 1 PS
- 4 Strips
- 4 Middle
- 1 Back



LAr EM Barrel

Trigger Tower ($\Delta\eta\mathrm{x}\Delta\phi$=0.1x0.1)
60 Cells in a TT

EM Sampling-3
Back: 2x4
($\Delta\eta\mathrm{x}\Delta\phi$=0.05x0.025)

EM Sampling-2
Middle: 4x4
($\Delta\eta\mathrm{x}\Delta\phi$=0.025x0.025)

EM Sampling-1
Front: 32x1
($\Delta\eta\mathrm{x}\Delta\phi$=0.003125x0.1)

EM Sampling-0
Presampler: 4x1
($\Delta\eta\mathrm{x}\Delta\phi$=0.025x0.1)

Super-Cells:
$\Delta\eta\mathrm{x}\Delta\phi$=0.025x0.1 in Front, Middle
$\Delta\eta\mathrm{x}\Delta\phi$=0.1x0.1 in Presampler, Back

EM Sampling-3
Back: 2x4
($\Delta\eta\mathrm{x}\Delta\phi$=0.05x0.025)

EM Sampling-2
Middle: 1x4
($\Delta\eta\mathrm{x}\Delta\phi$=0.025x0.025)

EM Sampling-1
Front: 8x1
($\Delta\eta\mathrm{x}\Delta\phi$=0.003125x0.1)

EM Sampling-0
Presampler: 4x1
($\Delta\eta\mathrm{x}\Delta\phi$=0.025x0.1)

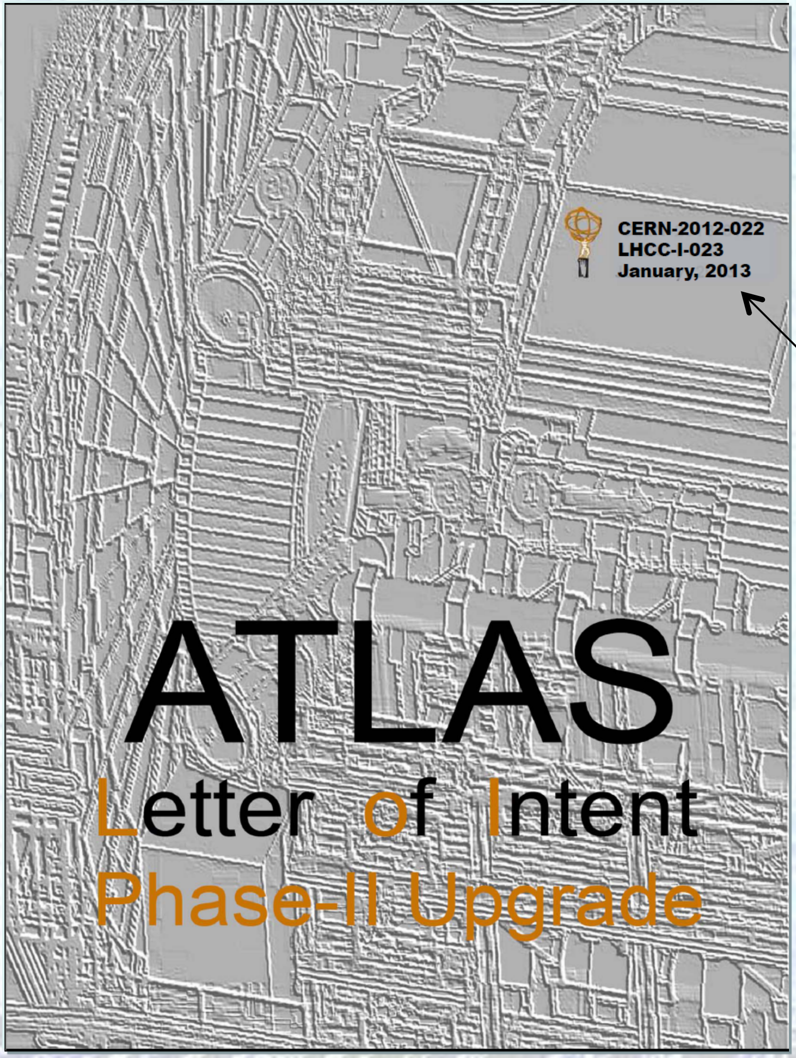
Presampler
SC_layer=0
SC_region=0
SC_eta=0...13 [$\Delta\eta$=0.1]
SC_region=1
SC_eta=14(15) [$\Delta\eta$~0.1(0.12)]
SC_phi=0...63 [$\Delta\phi$=0.1]

Front
SC_layer=1
SC_region=0
SC_eta=0...55 [$\Delta\eta$=0.025]
SC_region=1
SC_eta=56..58 [$\Delta\eta$=0.025]
SC_phi=0...63 [$\Delta\phi$=0.1]

Middle
SC_layer=2
SC_region=0
SC_eta=0...55 [$\Delta\eta$=0.025]
SC_region=1
SC_eta=56 [$\Delta\eta$=0.075]
SC_phi=0...63 [$\Delta\phi$=0.1]

Back
SC_layer=3
SC_region=0
SC_eta=0...12 [$\Delta\eta$=0.1]
SC_eta=13 [$\Delta\eta$~0.05]
SC_phi=0...63 [$\Delta\phi$=0.1]

Phase-II



CERN-2012-022
LHCC-I-023
January, 2013

ATLAS
Letter of Intent
Phase-II Upgrade

For the phase II upgrades we only have a Letter Of Intent

- No detailed designs yet
- Several alternatives for each sub-detector upgrade

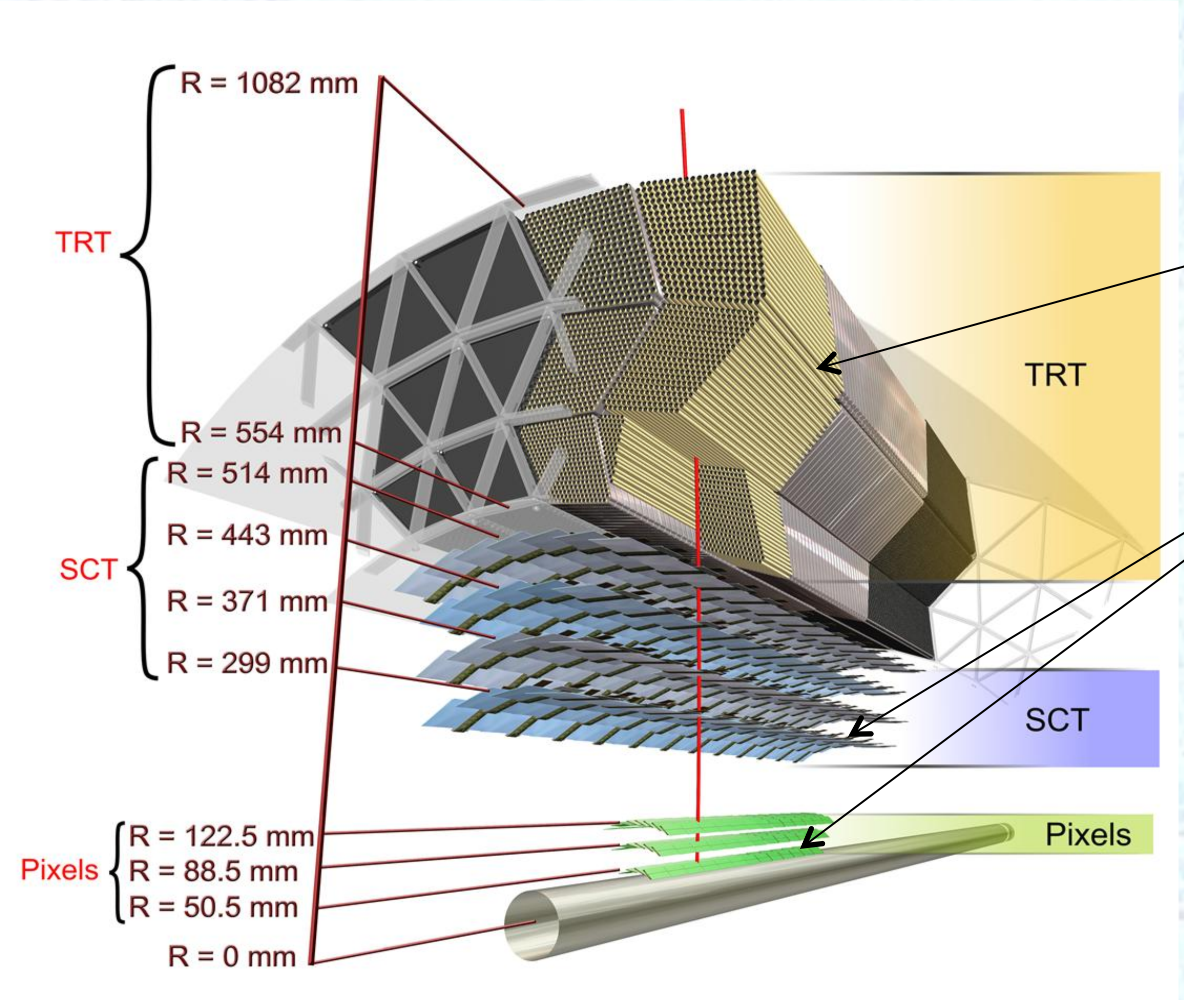
January 2013

We still have time for R&D

- Technical Design Reports not due until 2015 - 2016

What we eventually build may be very different from what is presented here…

The present ATLAS Inner Detector

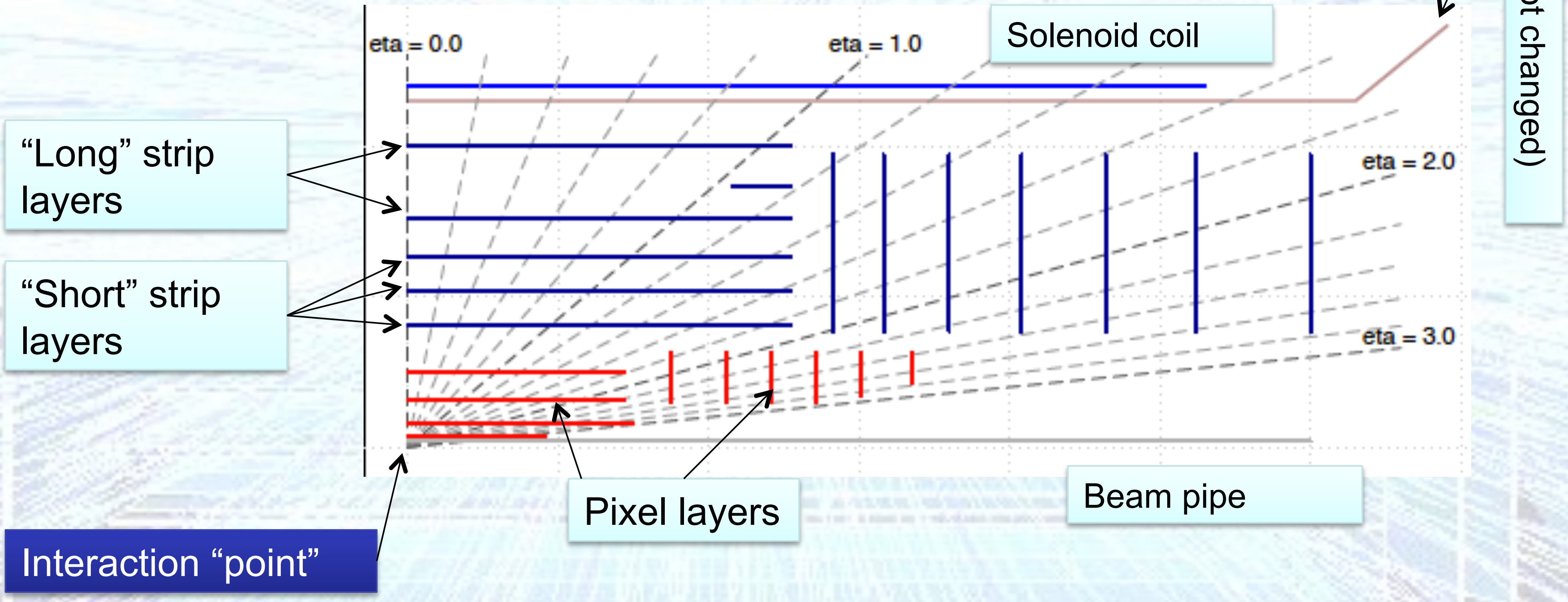


- beyond 2-3x10^{34} cm^{-2}s^{-1}
  - Occupancy in the TRT tubes ~ 50 %, several % in strips
  - Data rates in several layers beyond readout capacity
- Beyond radiation doses corresponding to 300-700 fb^{-1}
  - Radiation damage in sensors and electronics

Tracker upgrade baseline layout (LoI)

Classical layout with barrel cylinders and endcap disks

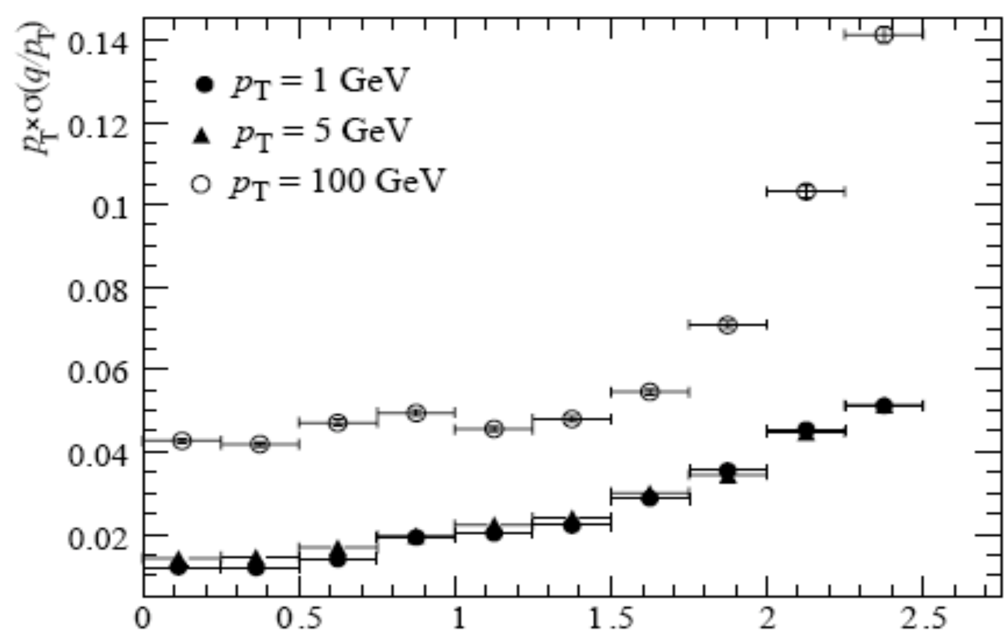
- optimizes use of the available space, within engineering constraints
- used to establish baseline performance and cost
- no special triggering layers

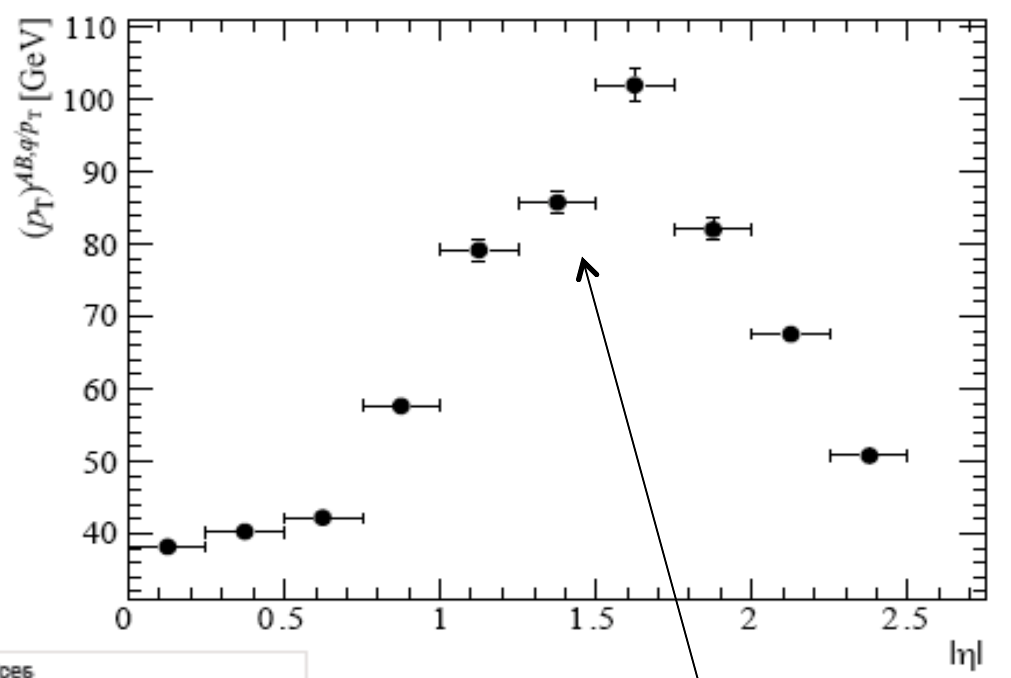


Tracker layout optimizations

- The tracking performance is determined by
  - Sensor resolutions
  - Amount and distribution of material traversed by tracks
  - Sensor position stability

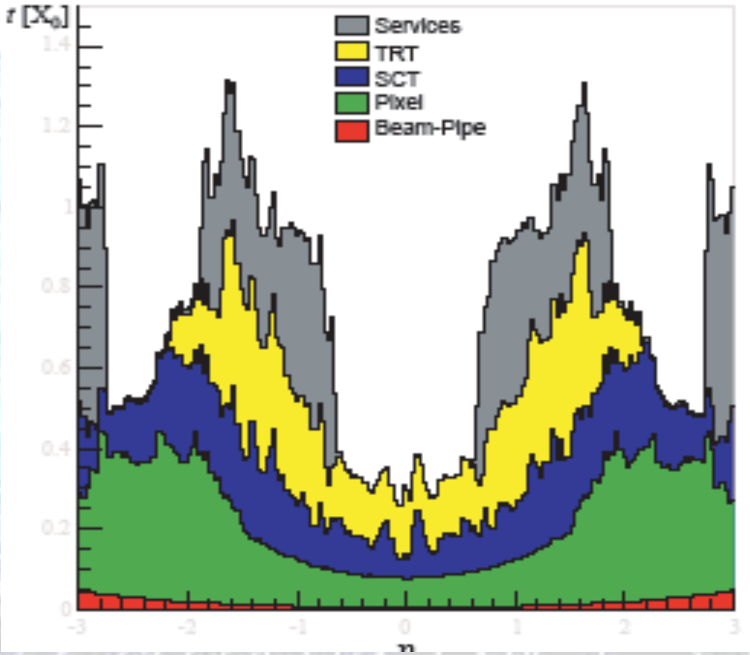
Effect of material on single track resolution (q/p_T)





Momenta at which multiple scattering and detector precision have same effect on resolution

Present ATLAS

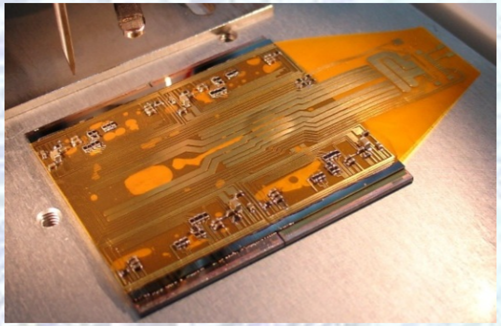


New All-silicon Inner Tracker

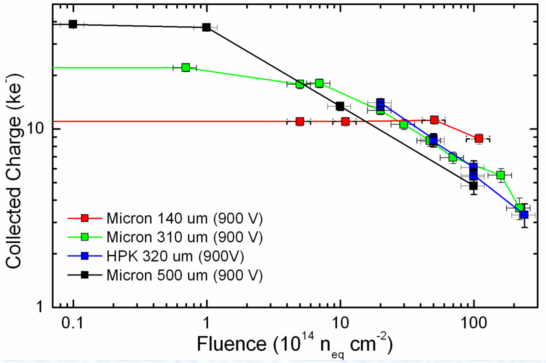
Pixel Detector

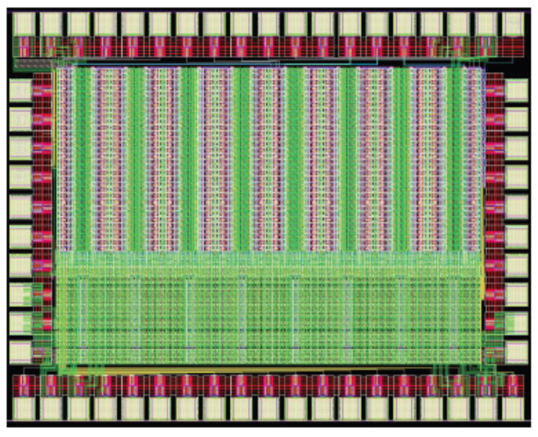
FE-I3

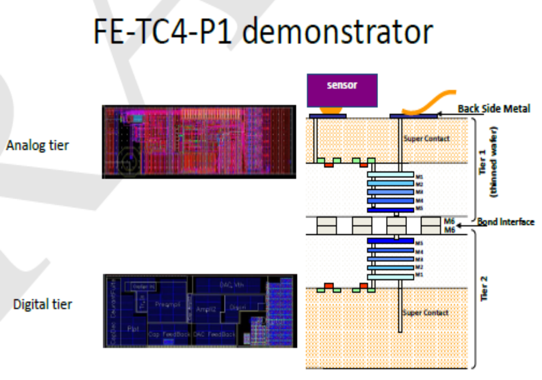
- Pixel sensors in several technologies proved to high doses (planar/3D/diamond shown to $2\times10^{16} n_{eq}/cm^2$)
- IBL pixel (50×250µm) OK for outer pixel layers, but can go down to 25µm×125µm pixels with 65 nm CMOS
- Square pixel (50×50µm and smaller) investigated
- Test structures in 65nm produced and even studies after irradiation
- Larger area sensors (n-in-p) quads/sextuplets produced on 150mm diameter wafers with several foundries
- Quad pixel module produced, being tested and results look promising



Quad module prototype



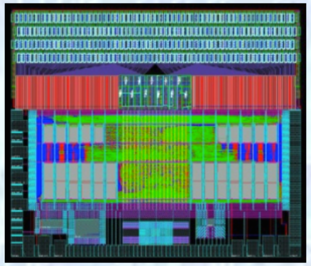


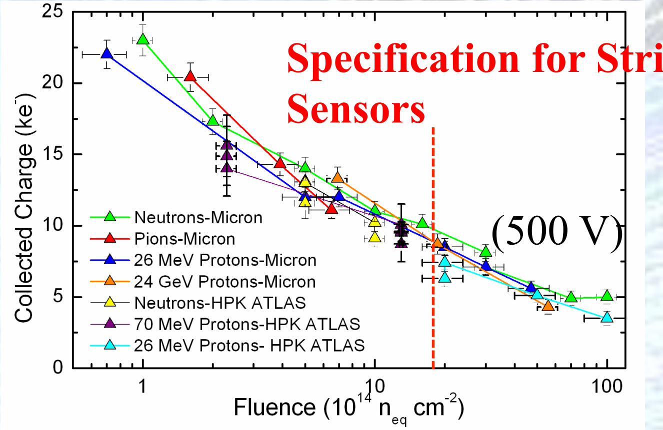


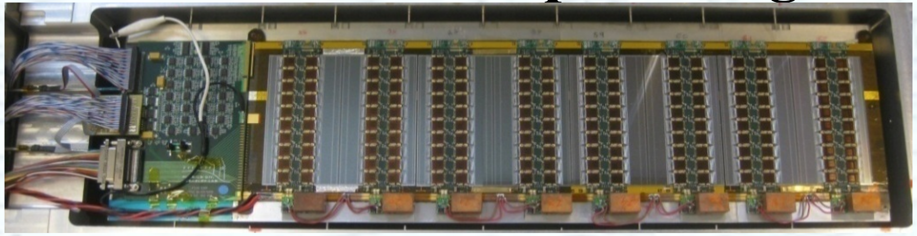
New All-silicon Inner Tracker

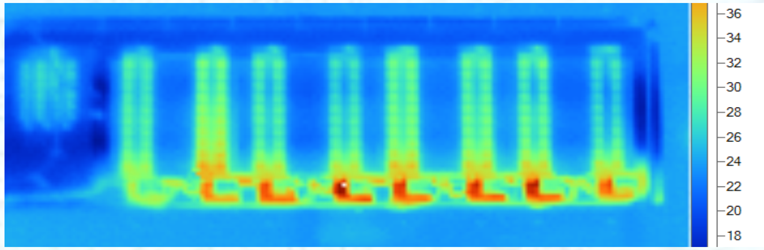
Strip Detector

- Next iteration sensors being ordered
- Next (256 channel) ASIC: FDR completed
- Many strip modules prototyped with ABCN250 ASICs
- First forward module prototypes produced
- Serial and DC-DC powering studied in detail on short versions of the stave

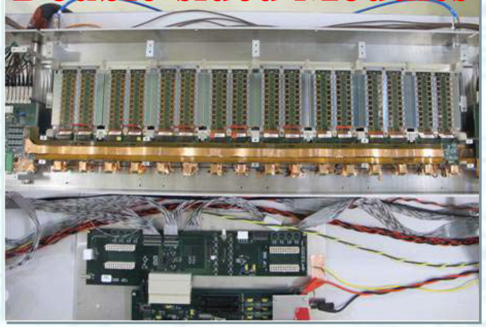




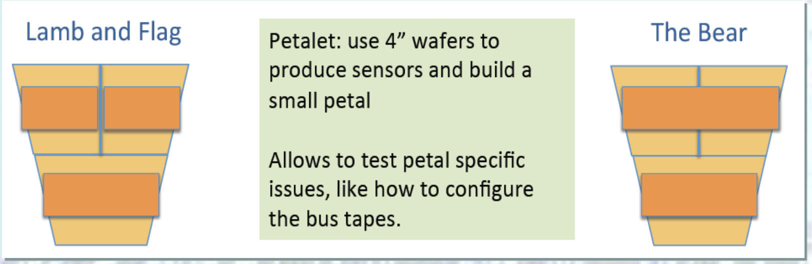




Double-sided Modules

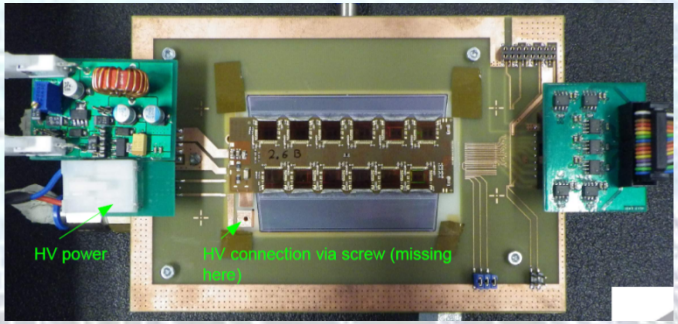


- R-phi pitch75 µm
- Z segmentation 25 mm “short strip”, 100 mm “long strip”
- Shorter strips investigated



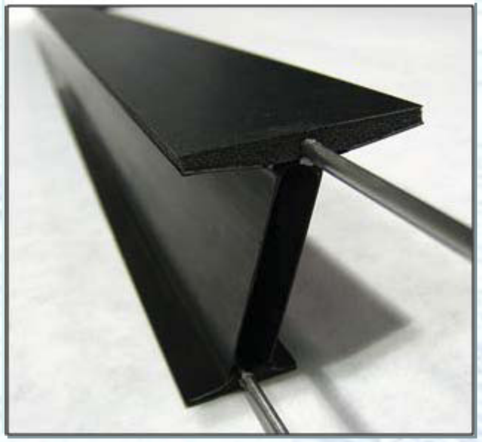
Petalet: use 4” wafers to produce sensors and build a small petal

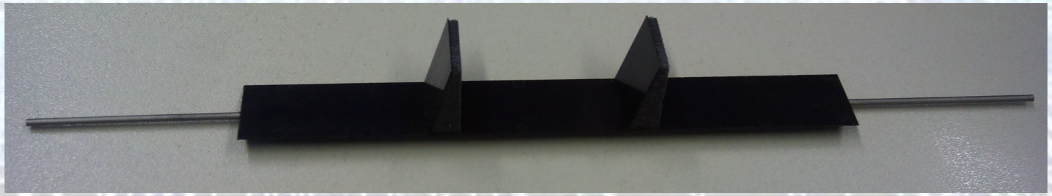
Allows to test petal specific issues, like how to configure the bus tapes.



Material reduction

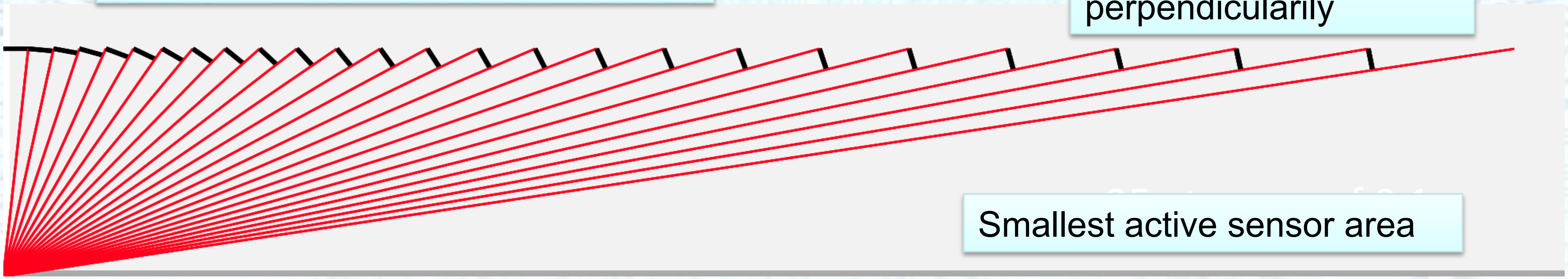
- On detector modules
  - Thinning of sensors
    - Present PIXEL: 300μm, IBL : 200μm
  - Thinning of on-module readout chips
    - Present PIXEL: 300μm, IBL : 150μm, 100μm produced
- Sensor supports (staves, petals)
- Services (cables, tubes, connectors, …)
- **Layout**





Layout optimization

The theoreticaly ideal tracking layer for LHC



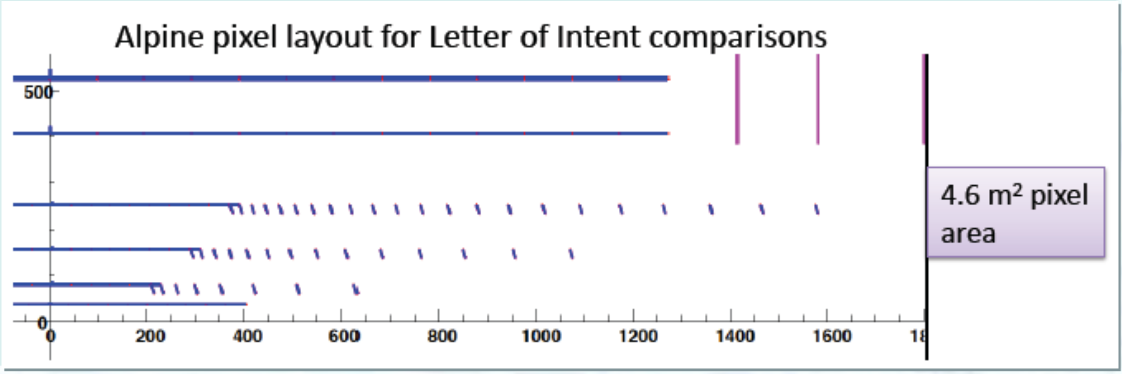
Constant radius (for solenoidal field)

Tracks cross detectors perpendicularily

Smallest active sensor area

- Unfortunately impossible to realise
  - Especially with rectangular sensors
  - Sensors need mechanical support, cooling, electrical connections…
  - If this geometry is realised on a stave, it seems impossible to achieve phi hermeticity (overlaps)
- It only makes sense to design a layout within a practical technology for sensors, services and mechanical support

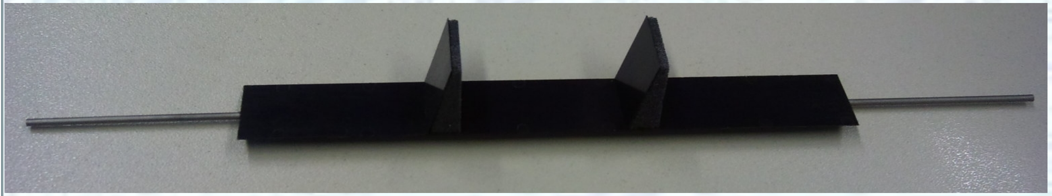
Layout variations: Alpine pixel

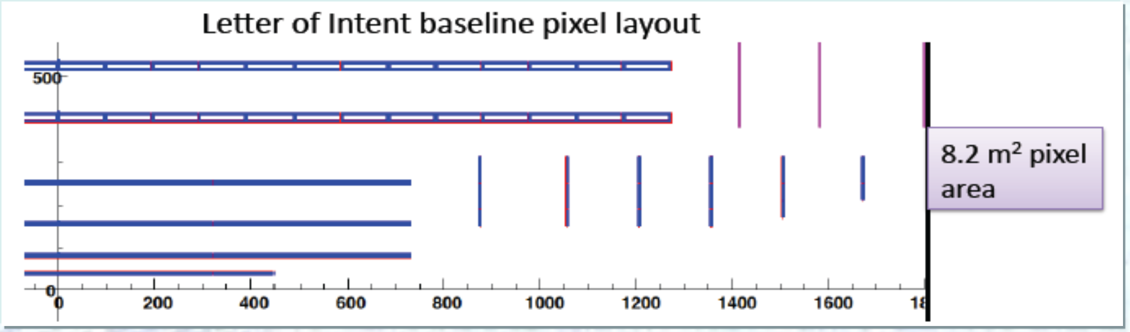


Alpine pixel layout for Letter of Intent comparisons

4.6 m^2 pixel area

Uses the same stave for barrel and endcap modules



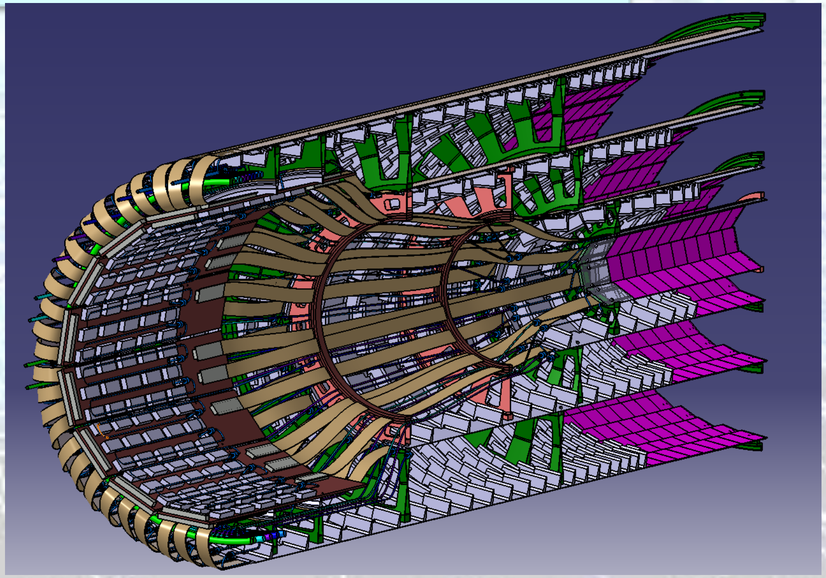


Letter of Intent baseline pixel layout

8.2 m^2 pixel area

No barrel-endcap transition region

- Less services material
- Simplified mechanical support



Large reduction in sensor area

Alpine stave material vs. eta

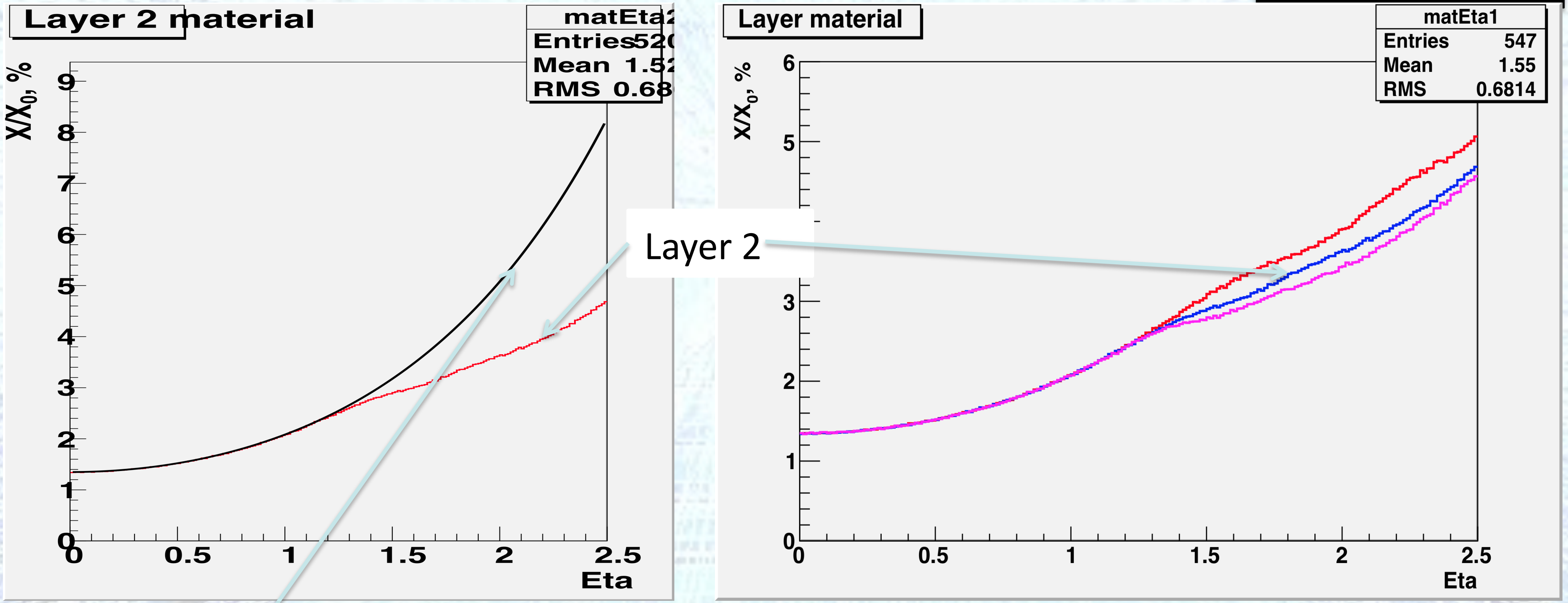
Almost 2x less material at eta 2.5 compared to “barrel-only”

Never worse than long barrel

Red – layer 1

Blue – layer 2

Magenta – layer 3



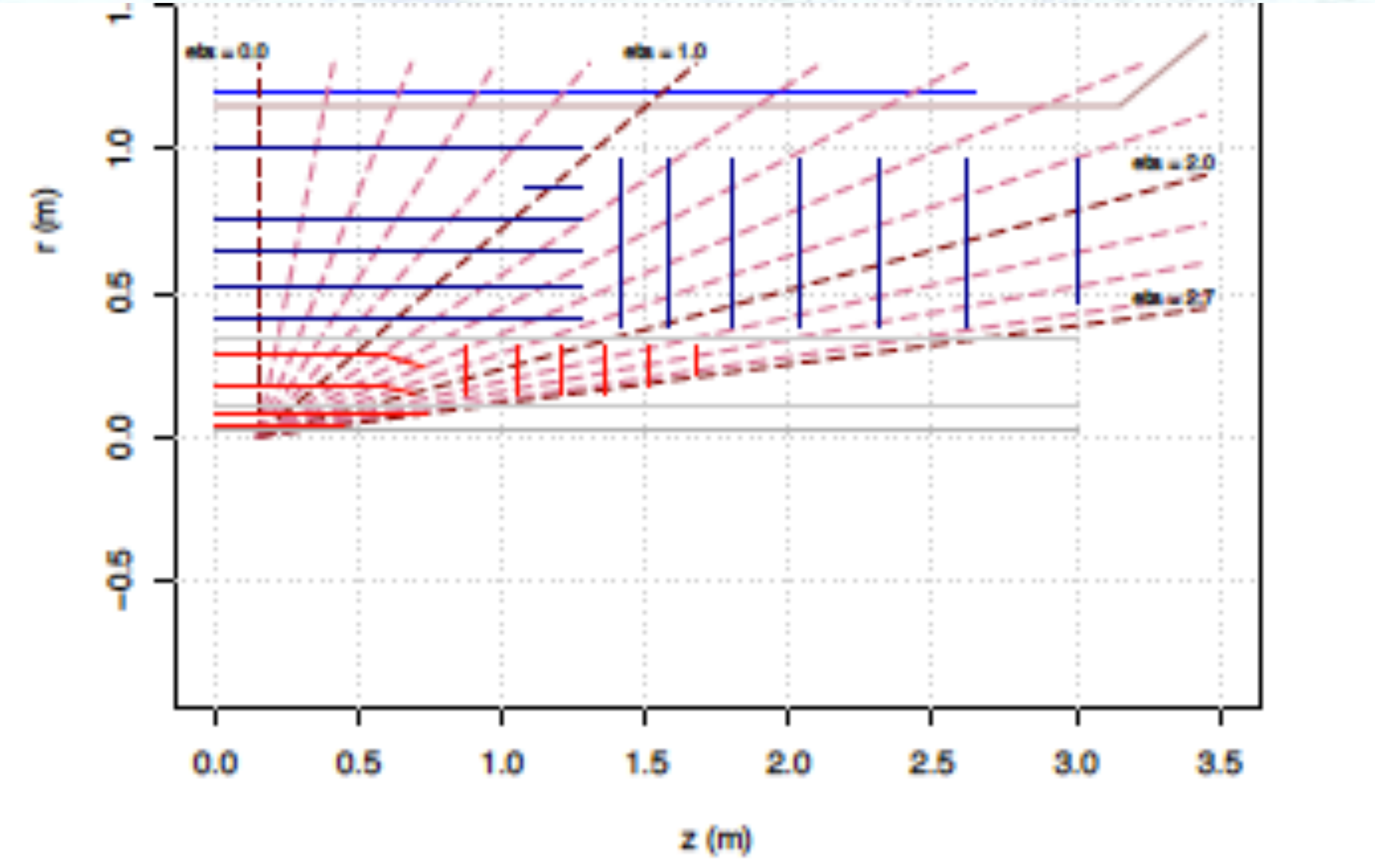
Layer 2

1/sin(theta) (long barrel)

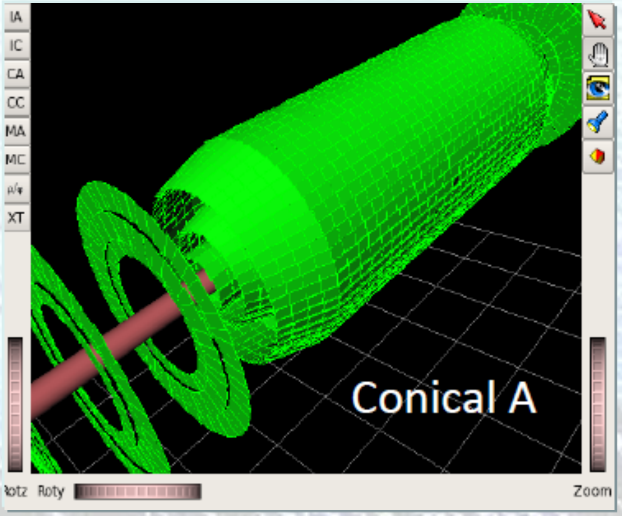
Smeared primary vertex

Layout variations: Conical pixel

Uses bent staves on outer barrel pixel layers

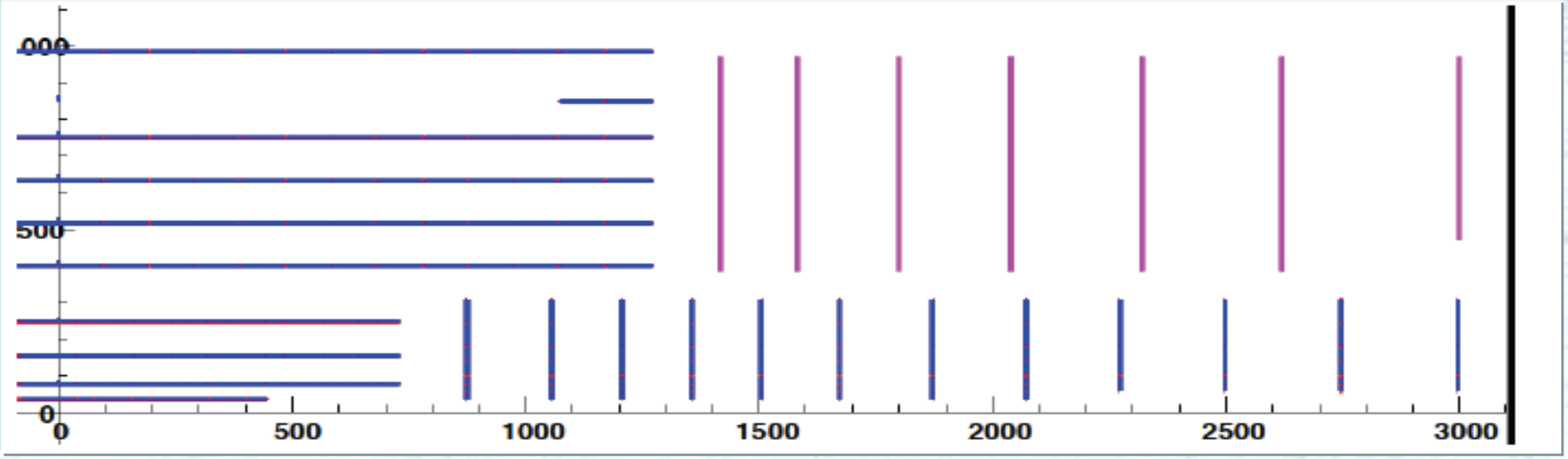


Improves hermeticity and material in transition region



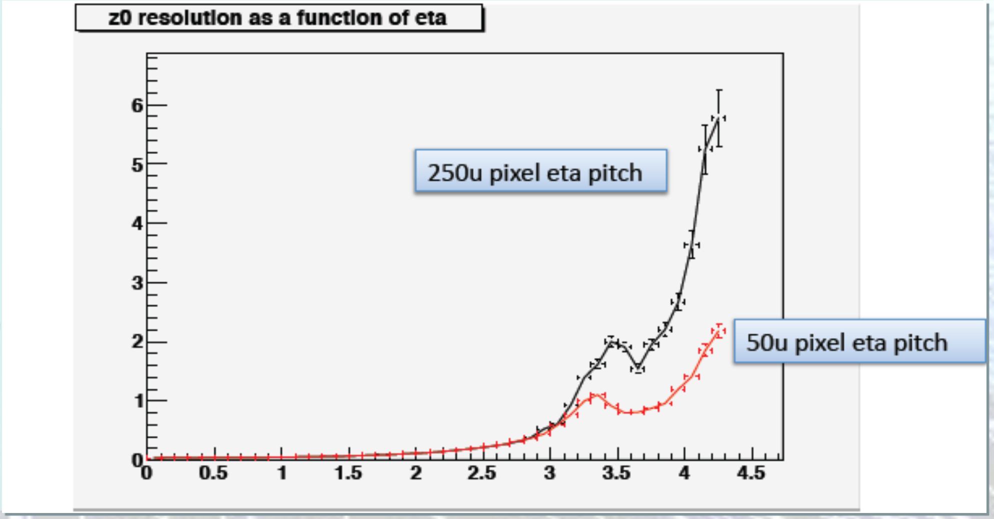
Layout variations: Very forward tracking

Straightforward extension of base-line layout
Can also be achieved with alternative layouts (Alpine)



Extends tracking to ~eta=4

- EM ~precise calorimetry in ATLAS up to eta=3.2
- Forward calorimetry up to eta=4.9



Currently quantifying benefit for physics

Summary

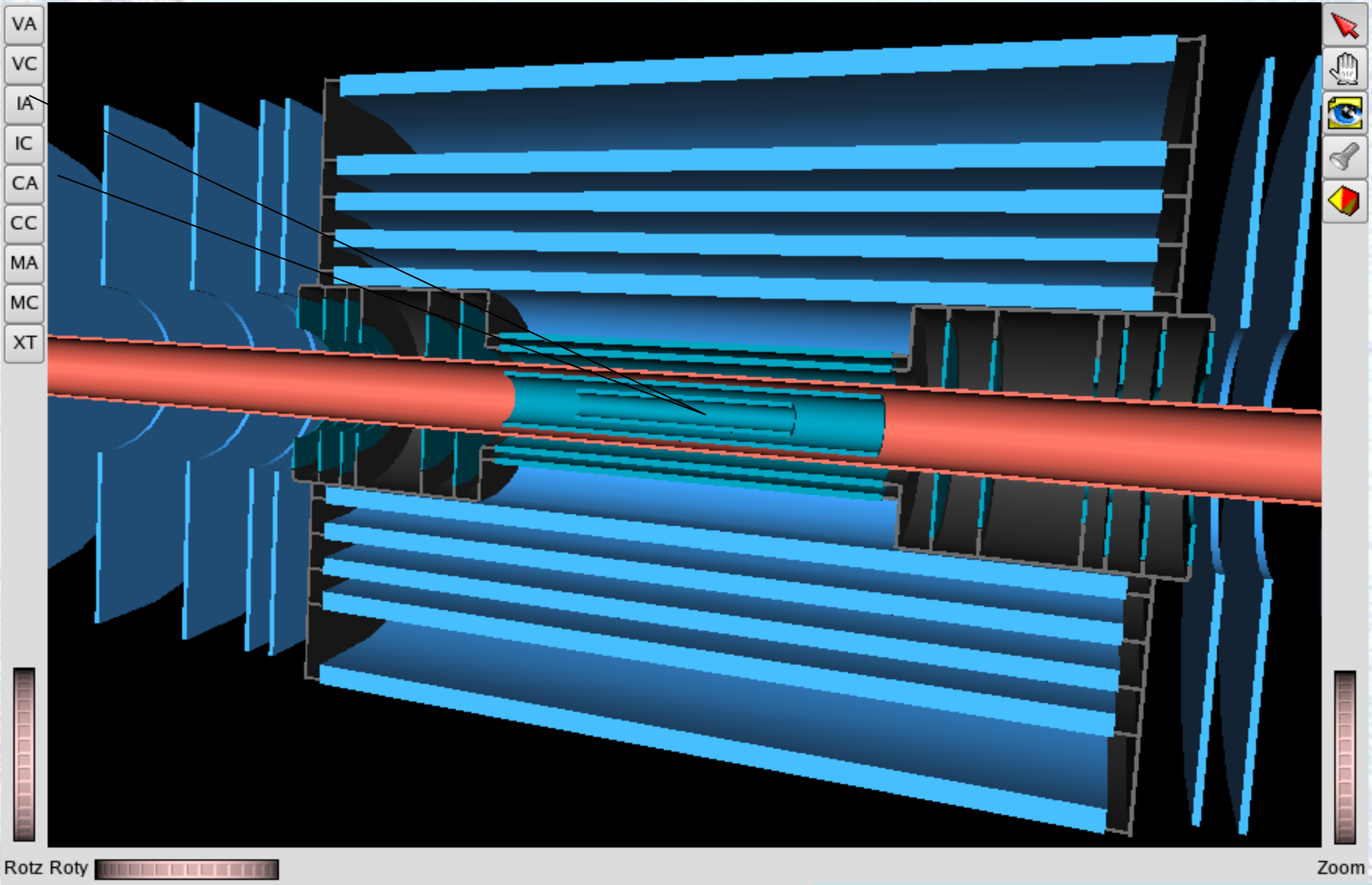
- ATLAS has a large upgrade program to meet the challenges of high luminosity LHC physics
  - Phase 0 upgrades happening now
  - Phase I in final design stages, for installation in ~2018
  - Phase II forseen for ~2022
    - Requires full replacement of the inner detector (tracker)
    - We have 2-3 years to complete the R&D and to choose between alternative developments
- The minimal goal of the upgrades is to preserve performance while luminosity increases
  - And in several cases we can improve / extend the performance

BACKUP

Material distribution:Services routing

Service volumes in black, Pixel Support Tube in brown, active layers in blue

Tracks cross the same services 3-4 times



Sensors crossed at shallow angles (<<45^{o})

A previously studied ATLAS layout