ATLAS Tile Calorimeter Readout Electronics Upgrade Program for the High Luminosity LHC

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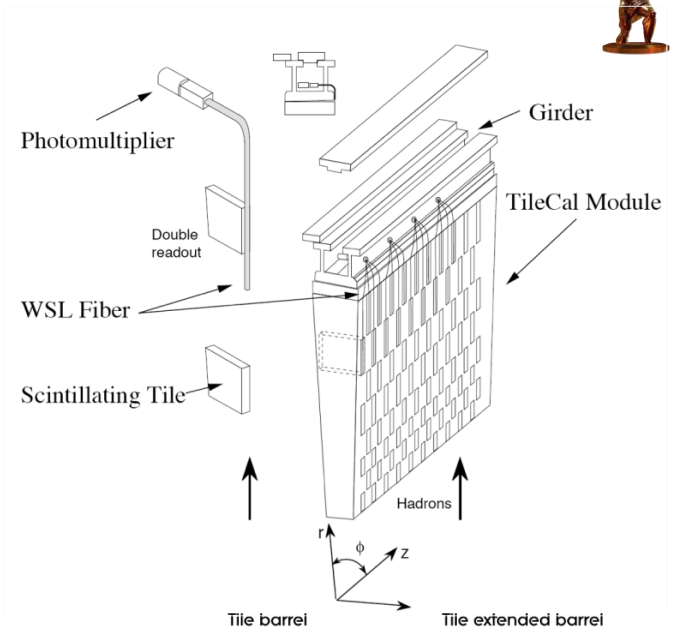
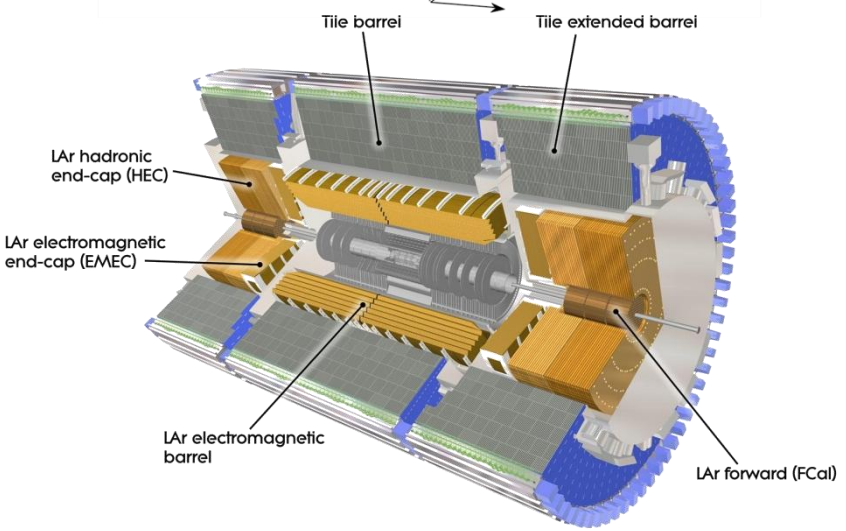
Outline

- The ATLAS Tile Calorimeter (TileCal) at LHC
- Motivation for upgrading
- Overview of TileCal readout electronics components
- On-detector electronics upgrade
- Off-detector electronics upgrade
- Status
- Conclusions

TileCal

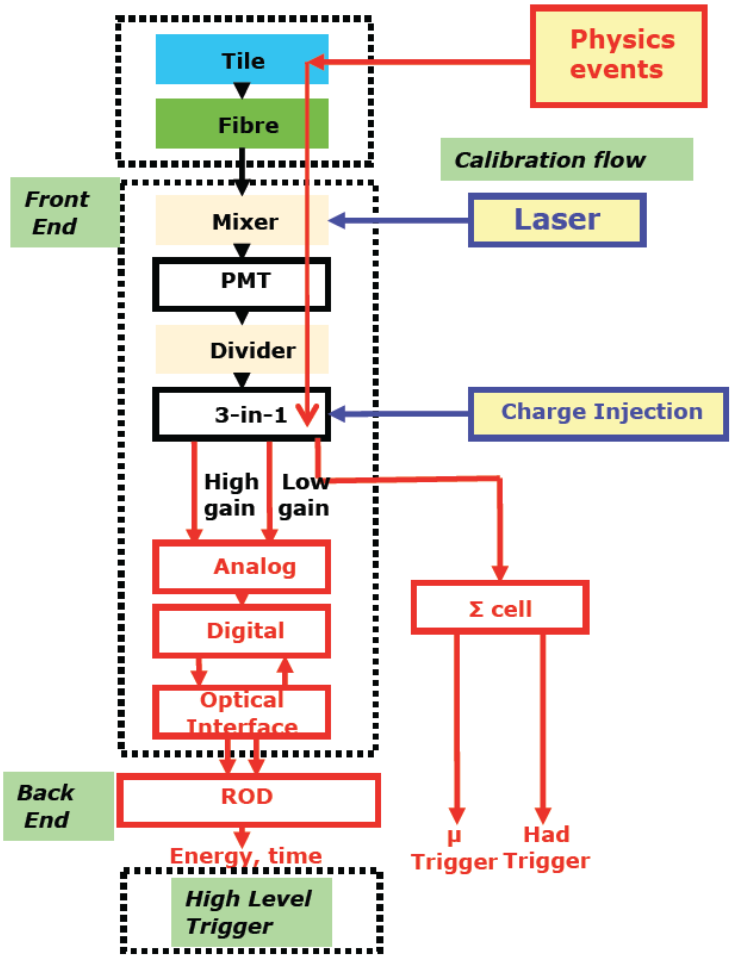
- ATLAS hadronic calorimeter
- Sampling calorimeter with steel plates as absorber material and plastic scintillating plates (tiles) to sample the energy
- Optical fibers transmit the light to PMT cells located inside the girder (electronics drawer)
- Cylindrical structure divided in 1 central barrel and 2 extended barrels formed by 64 modules each
- More than 10,000 readout channels





TileCal Signal Chain

- PMT signals are conditioned and amplified by two channels with gain ratio of 1:64 (**3-in-1 card**)
- Pulses are digitized by 10-bit ADC at 40MHz (**Digitizer**)
- The digital signals are sent to back-end through an optical interface (**Interface Board**)
- Compact information (tower sum) is sent to ATLAS LVL1 Trigger (analog signals) (**Trigger Boards**)

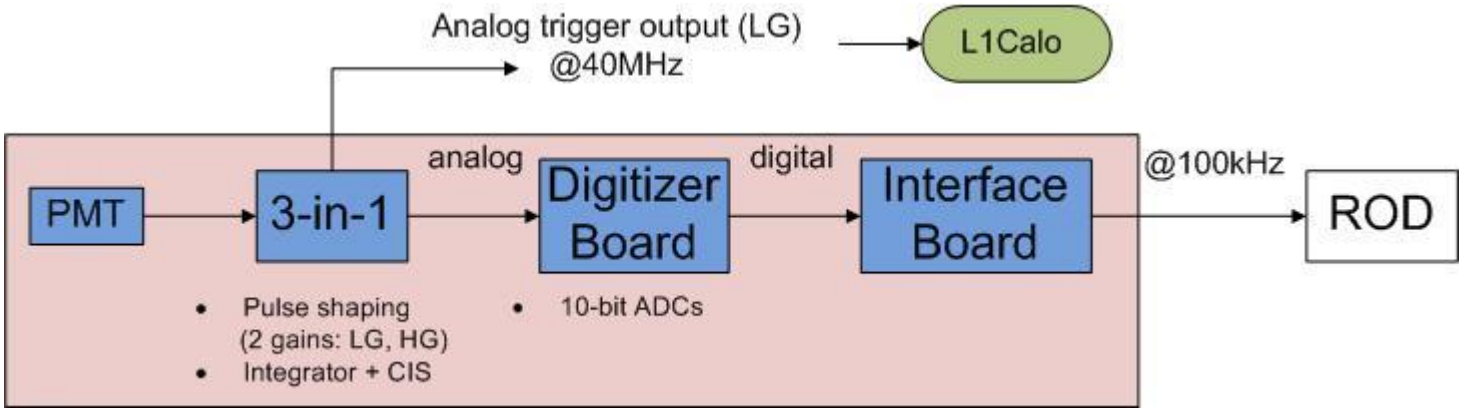


Why upgrade?

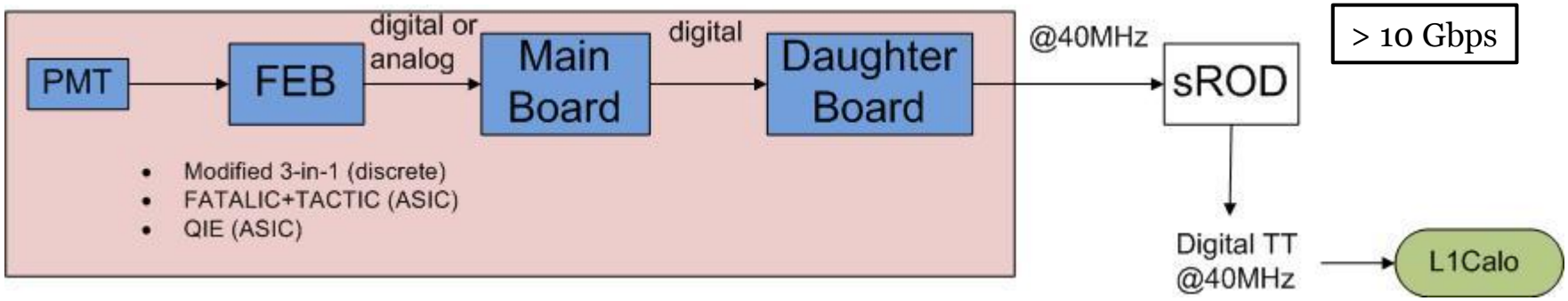
- Increase of LHC luminosity at phase II (10^{34} to $\approx 10^{35}$ $cm^{-2}s^{-1}$)
  - The system need to cope with higher initial event-rates
  - On-detector electronics exposed to higher radiation levels
  - More fake muons
- More selective trigger system – more complex algorithms
  - Introduce lvl0 trigger to reduce lvl1 input rate
  - Use track trigger at lvl1
  - Trigger towers with improved spatial resolution
  - Topological trigger at lvl1
  - Better muon identification

Overview: Current vs New Architecture

- Current architecture

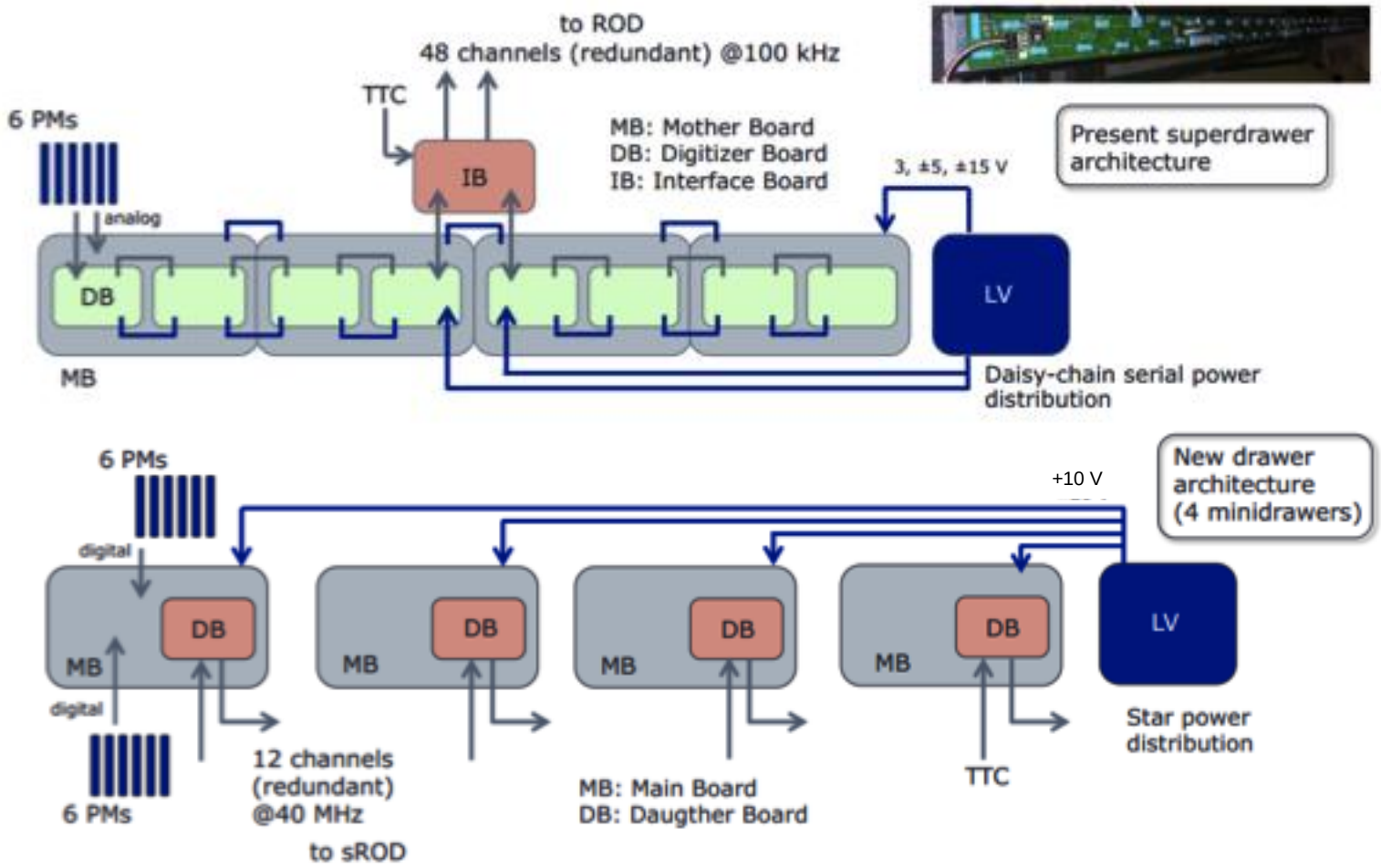


- Phase II architecture



Overview: Current vs New Architecture

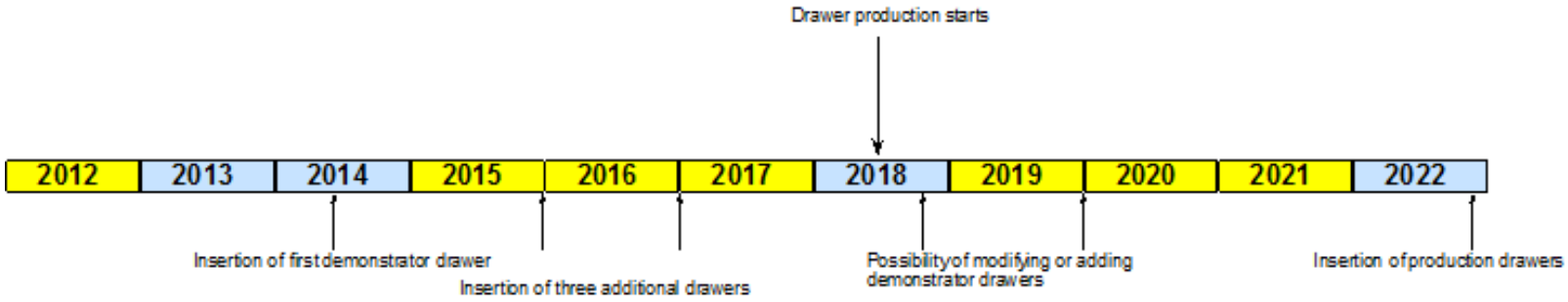
- TileCal Super Drawer



Upgrade Electronics

- On-detector Electronics:
  - New Front-End Board:
    - Three options are under evaluation and the one with the best performance will be choose for Phase II (Modified 3-in-1,QIE and FATALIC)
  - New Main Board (data processing and control)
  - New Daughter Board (data transmission)
- Off-detector Electronics:
  - “super” Read Out Driver (sROD) (back-end electronics)

Schedule for the Upgrade Activities



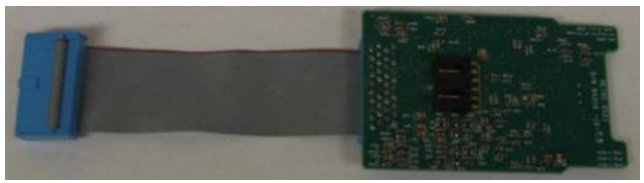
- 2013
  - One upgraded drawer (demonstrator) available in lab for tests with new front-end (FE) electronics, new Main Board, new Daughter Board, new sROD prototype
    - **Backwards compatible DEMONSTRATOR**
- 2013-14 shutdown
  - Install one demonstrator drawer into detector
- 2014-2018
  - Extensive tests and decision of FE architecture
- 2018-2020
  - Production of the new system

Demonstrator Drawers

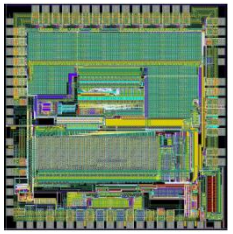
- Should contain as much of the final phase 2 design as possible while being compatible with the present system
- However, the demonstrator may be modified on several occasions to verify new solutions
- But to stay compatible all versions must deliver analog trigger data, i.e. The FEB must be 3-in-1
- The FEBs will be evaluated in test beams probably starting in 2015

On-detector Upgrade (Front-end)

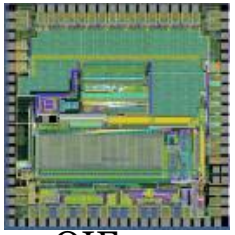
1. Modified 3-in-1 card (discrete) (Chicago)
   - Based on original 3-in-1 cards
   - Conditioning PMT, 2 gains
   - Calibration capabilities
   - Better linearity than current 3-in-1
   - Passed radiation tests



2. FE-QIE (ASIC) (ANL)
   - Design based on the QIE chip (Fermilab)
   - No pulse shaping, 4 different gains
   - Onboard flash ADC
   - 40 MHz operation
   - Calibration capabilities
   - First fully functional QIE designed



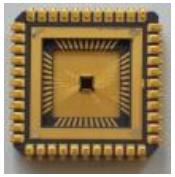
QIE 10_P5



QIE 10.3

3. FE-FATALIC (ASIC) (Clermont-Ferrand, LPC)
   - Combined ASIC solution (FATALIC 3+TACTIC)
   - FATALIC 3: Shaping stage, 3 different gains
   - TACTIC: Digitization with 12-bit ADC at 40MHZ
   - Calibration capabilities
   - FATALIC 1 and 2 validated
   - New version of FATALIC 3 under validation

FATALIC 1 (0.8 cm)

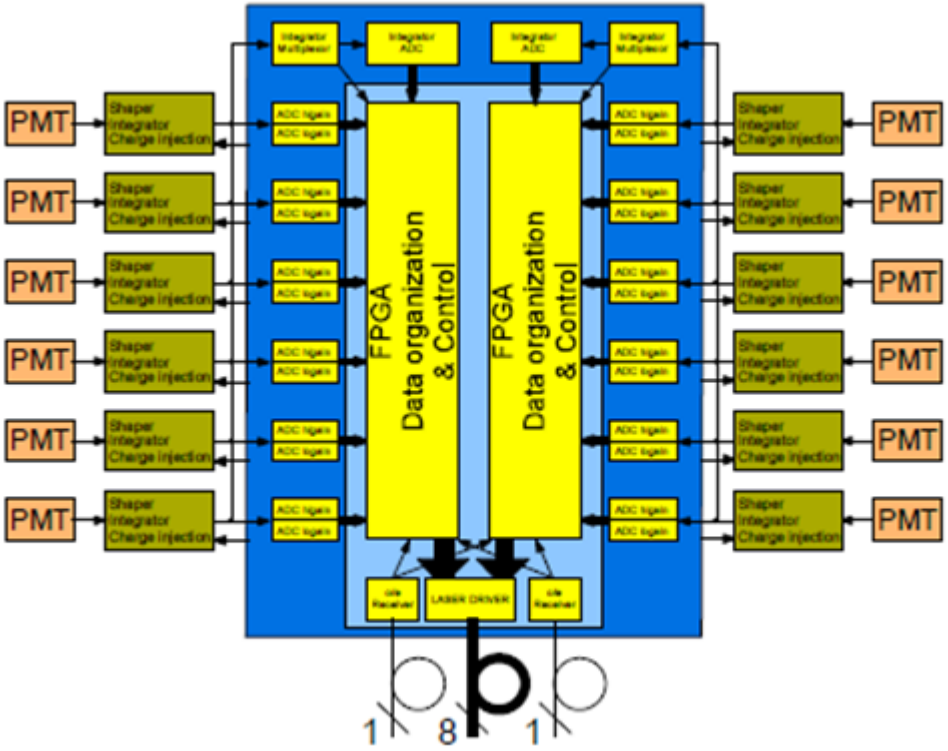


FATALIC 2 (1.7 cm)

On-detector Upgrade (Main Board)

- Data processing (12 channels) and control
- One version for each FEB
  - MB-1 (Modified 3-in-1) (Chicago-Stockholm)
    - Contains ADCs (12-bit at 40 MHz operation)
    - Contains preliminary data processing
    - Early prototype digitizes signals from 4 modified 3-in-1
  - MB-2 (QIE) (ANL)
    - Minor modification from MB-1
    - No ADCs; different data formatting
  - MB-3 (FATALIC) (Clermont)
    - Minor modification from MB-1
    - No ADCs; different data formatting

On-detector Upgrade (MB-1)



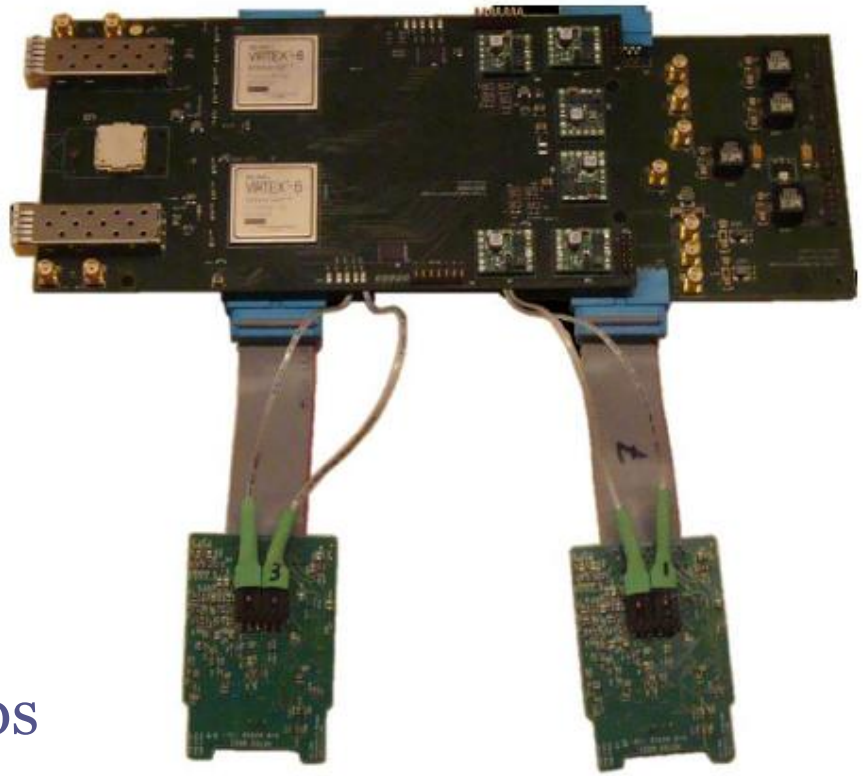
Scheme for 12-PMT MainBoard

On-detector Upgrade (Daughter Board)

(Stockholm-Chicago)

- Data interface with the back-end electronics (40 MHz)
- Should be the same for all FEB
- Optical link interface
  - Two Xilinx Kintex-7 FPGA
  - Clock, trigger and control via GBT protocol
  - 2 optical link candidates:
    - Avago/SNAP12 – 4.8 Gbps
    - Luxtera modulators – 10 Gbps

early prototype



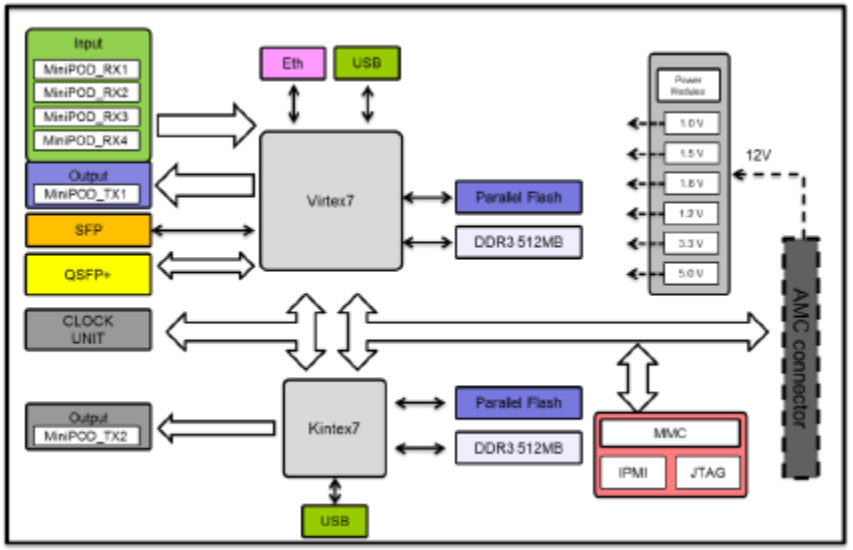
Off-detector Upgrade (sROD)

(LIP-Stockholm-Valencia-Rio)

- Requirements for sROD Demonstrator:
  - Data reception for the new drawers (48 PMTs)
  - Data Processing
    - Pipeline memories
    - Derandomizer memories
    - Data reconstruction
  - TTC and DCS management
  - L0/L1 calo functionalities
  - Compilant with ATCA standard

Off-detector Upgrade (sROD)

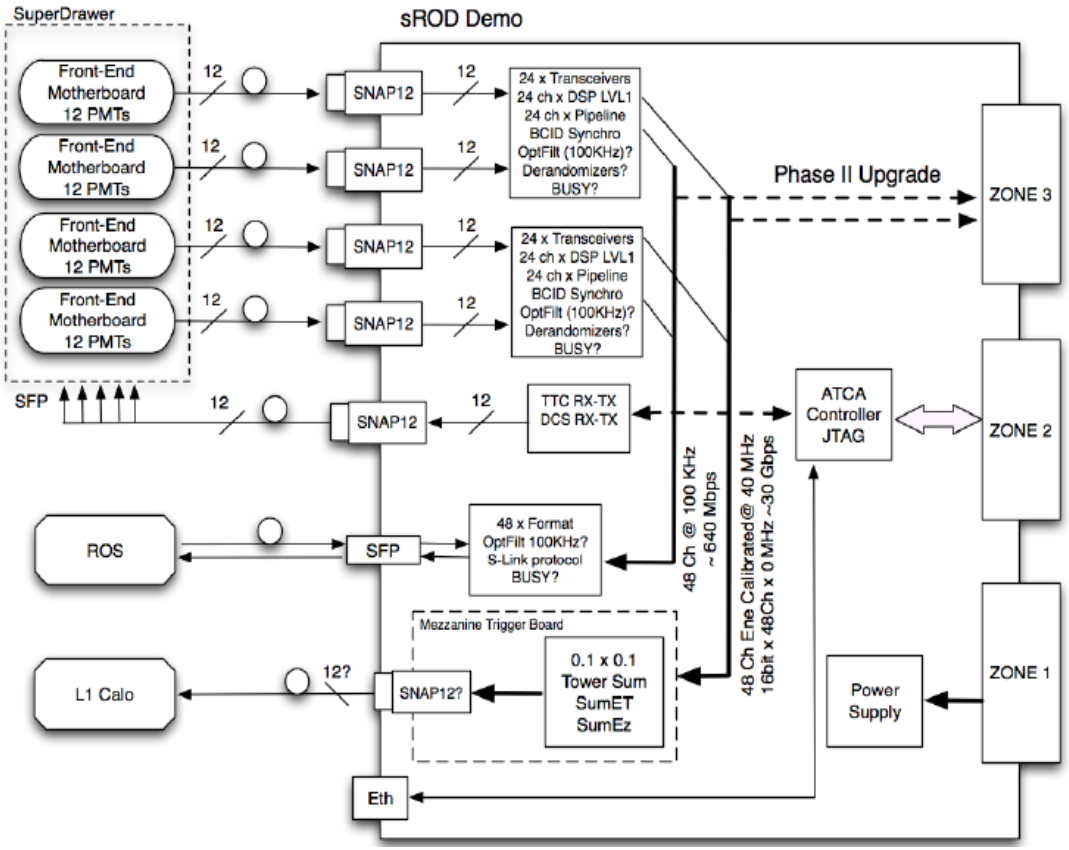
- sROD demonstrator design:
  - AMC standard compliant:
    - Double mid-size AMC (180.6 x 148.5 mm)
  - Processing Units:
    - 1 Xilinx Virtex 7 FPGA
    - 1 Xilinx Kintex 7 FPGA
  - Parallel Optics:
    - 4 x Avago RX MiniPODS (12 x 4.8 Gbps)
    - 1 x QSFP+ module (10 Gbps)
    - 2 x Avago TX MiniPODs (12 x 10GBps)
    - 1 x SFP connector



sROD diagram

Off-detector Upgrade (sROD)

- Super Read Out Driver (sROD) demonstrator board



sROD functional diagram

Upgrade Projects Status

Modified 3-in-1	QIE	FATALIC	Main Board	Daughter Board	sROD
Prototype tested Passed first radiation tests Now making demonstrator version	2 previous partial functional prototypes were successful 3rd version fully fucntional already sent to foundry radiation tests next	FATALIC 1 and 2 already validated Tests with FATALIC3 by April FATALIC+ TACTIC by November	First Prototypes already tested Schematics completed for the demonstrator version Currently under layout	Tests in progress with second prototypes High speed links partially tested	Schematics are finished First prototypes for beginning of April

Conclusions

- Different institutes are taking part in this challenging R&D period
- Three different FEB electronics approaches are being considered to cope with LHC higher data rates and radiation levels at phase II
- New boards (on-detector and off-detector) equipped with advanced devices and protocols are being employed
- Extensive tests will be performed at phase 0 (2013) using a slice of the new upgraded system (demonstrator uses discrete 3-in-1 modified boards)
- The current TileCal electronics is operating very well, therefore, the readout electronics will not be replaced until phase II