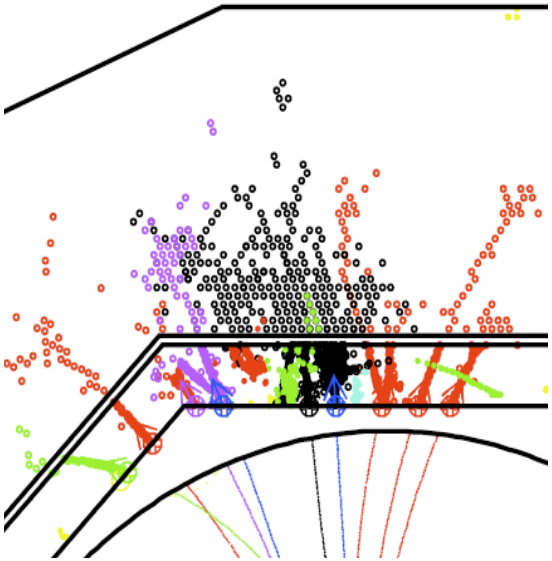
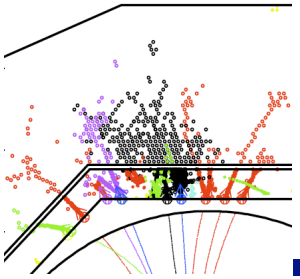
Work Package 9 Task 9.5: Granular Calorimeter Studies Infrastructure

Felix Sefkow



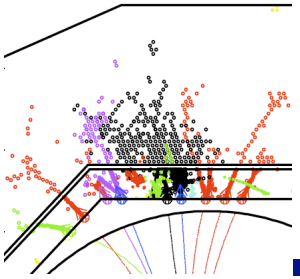
AIDA 2nd Annual Meeting
Frascati, April 10-12, 2013



Summary

- Task overview
  - Deliverables and Milestones
  - Description of work
  - New sub-task leaders

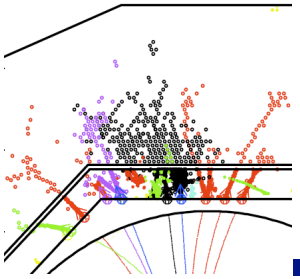
- Test beam infrastructure
- FCAL
- Electronics
- ECAL, AHCAL, DHCAL



Deliverables

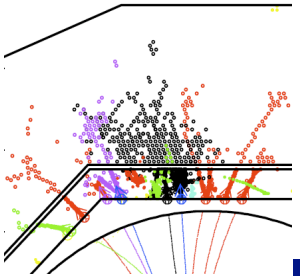
- D 9.7: Integrated **infrastructure** for highly granular calorimeters
  - Due month 40 (**May 2014**), lead DESY
- D 9.9: **Adequation of Geant 4** simulation of hadronic showers in different media (report)
  - Due month 46 (**Nov 2014**), lead DESY

- In WP 9.1, but probably requesting input:
- D 9.8: Infrastructure **performance and utilization** (report)
  - Due month 46 (**Nov 14**), lead CSIC



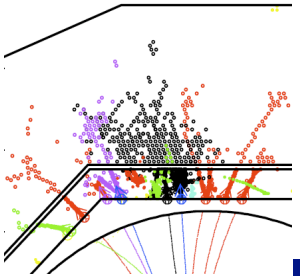
Milestones

- MS 42 **Gas** system, control and bench **structure**
  - due month 24 (**Jan 2013**), lead CNRS-LAPP
- MS 43 3rd generation fast **read-out chips**
  - due month 30 (**Jul 2013**), lead CNRS-LAL
- MS 44 Multilayer **tungsten** structure with position control and monitoring for **forward** calorimeters
  - due month 30 (**Jul 2013**), lead DESY-Z
- MS 45 Calibration and **power** supply system
  - due month 36 (**Jan 2014**), lead UIB
- MS 46 **El.magn**. **calorimeter** of at least 18x18cm^2 area
  - due month 36 (**Jan 2014**), lead CNRS-LLR
- MS 47 Multichannel readout ASICs for luminosity detector
  - due month 40 (**May 2014**), lead AGH-UST



Description of Work

- Mechanical structure to place and move elements
  - CERN, DESY, UCL, CIEMAT **MS42**
- Lumical structure, W radiator and ASICs
  - DESY, TAU, AGH-UST, IFJPAN **MS44, 47**
- ECAL extension of the EUDET module
  - IPASCR, CNRS-LAL, -LPSC, -LLR **MS43, 46**
- Hadronic structure with tungsten radiator and services
  - CERN, DESY, Wuppertal, MPG-MPP, IPASCR, CNRS-LAL, -IPNL, -LAPP, -LPC, UIB, UCL, CIEMAT **MS43, 45**



Sub-tasks

- ECAL: D. Jeans → **Roman Poeschl**
  - LLR, LPSC, IPASCR
- AHCAL: E. Garutti → **Katja Krüger**
  - CERN, DESY, MPG-MPP, IPASCR, UIB, Wuppertal
- DHCAL: Imad Laktineh
  - LAPP, IPNL, LPC, CIEMAT, UCL
- FCAL: Wolfgang Lohmann
  - CERN, DESY, AGH-UST, IFJPAN, TAU
- FEE: Nathalie Seguin-Moreau
  - LAL, UHEI
- TBM: Erik van der Kraaij
  - CERN, DESY, UCL, CIEMAT

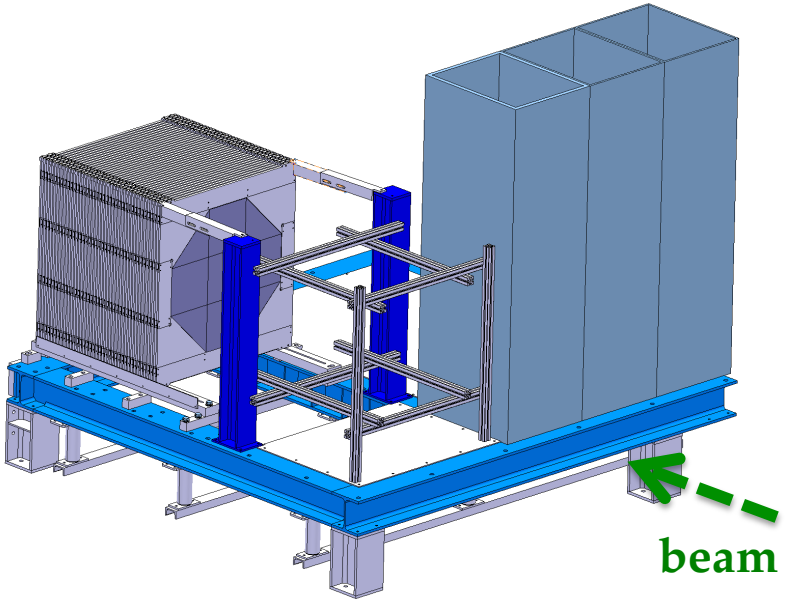
CALICE Calorimeter for ILC

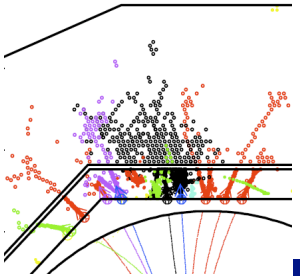
FCAL Collaboration *High precision design*

Test beam infrastructure, Mechanics

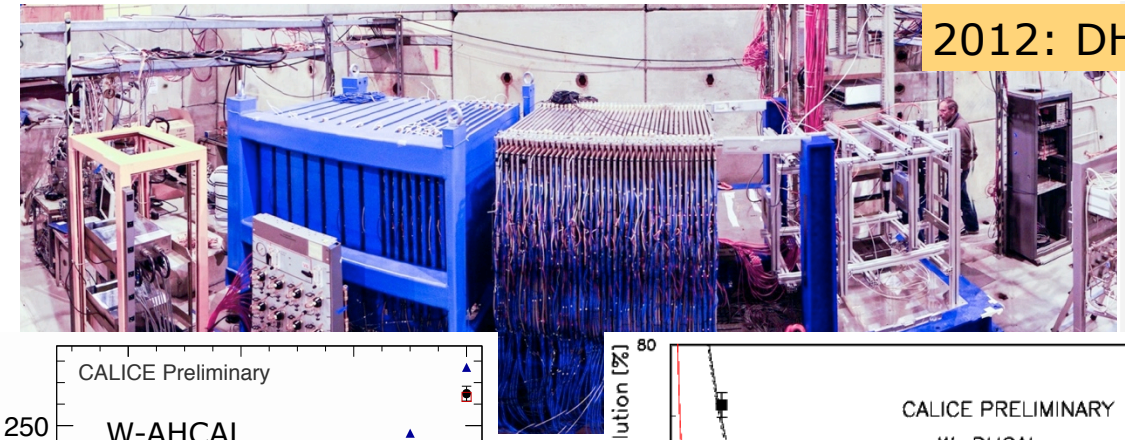
Improvements of infrastructure

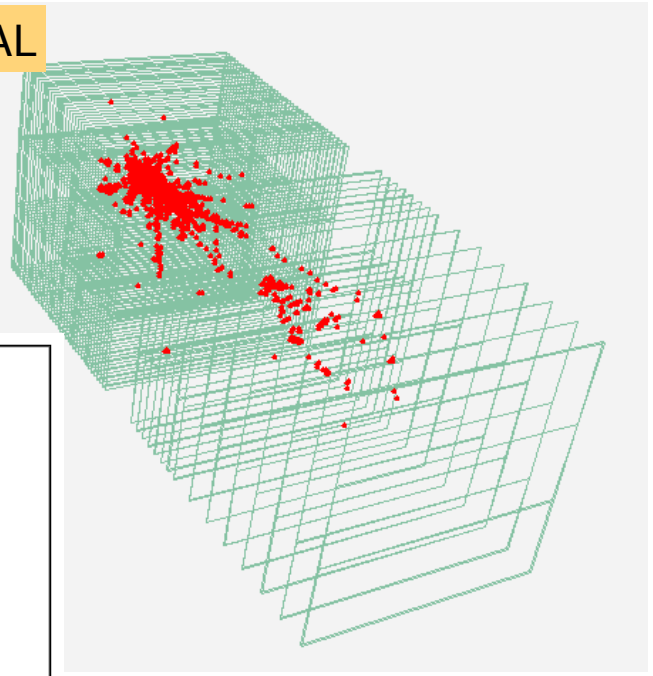
Made such that it can be transported fully equipped

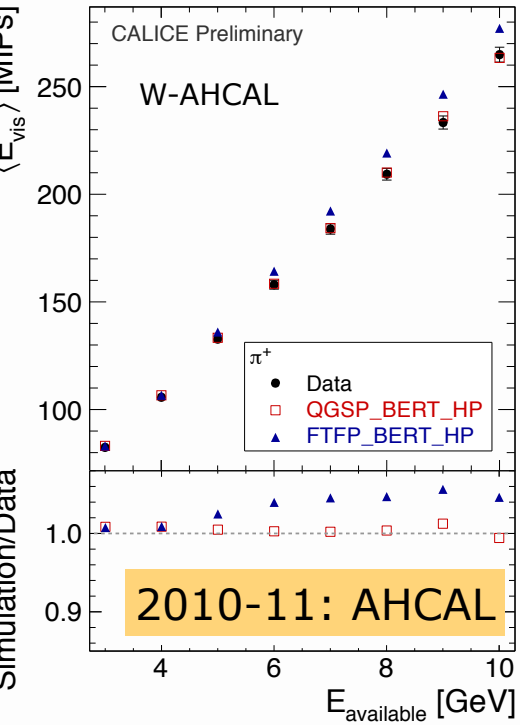


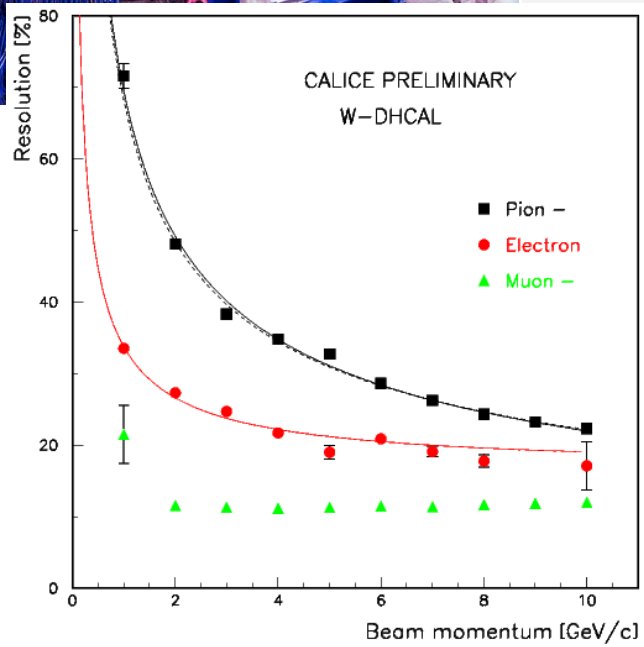


Tungsten usage, results









Test beams in 2012:

- PS T9: 2 weeks in May
- SPS H8: 2 + 1 + 1 weeks in June, August & November.

- Gas system: Micromegas and RPCs have their own

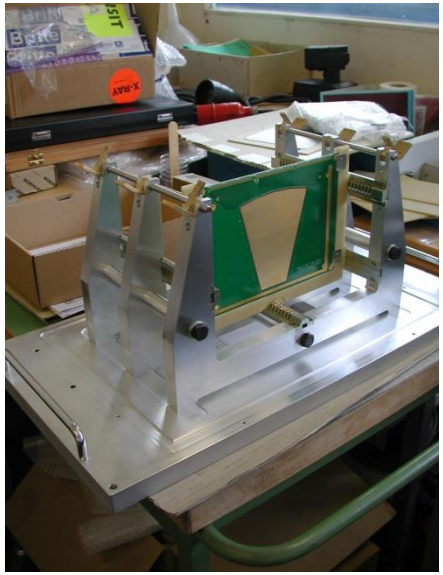
FCAL

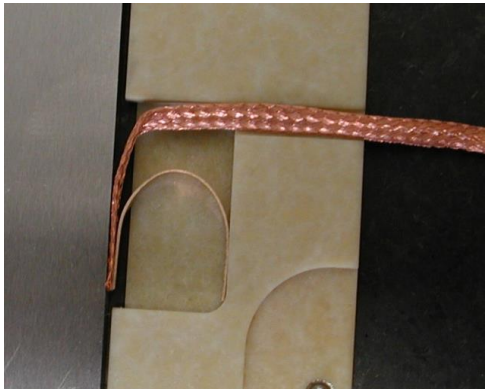
AIDA calorimeter : towards the test beam measurements

Leszek Zawiejski
Institute of Nuclear Physics PAN, Cracow

On behalf of FCAL Collaboration

The mechanical structure is ready





Grounding connection tests have been performed

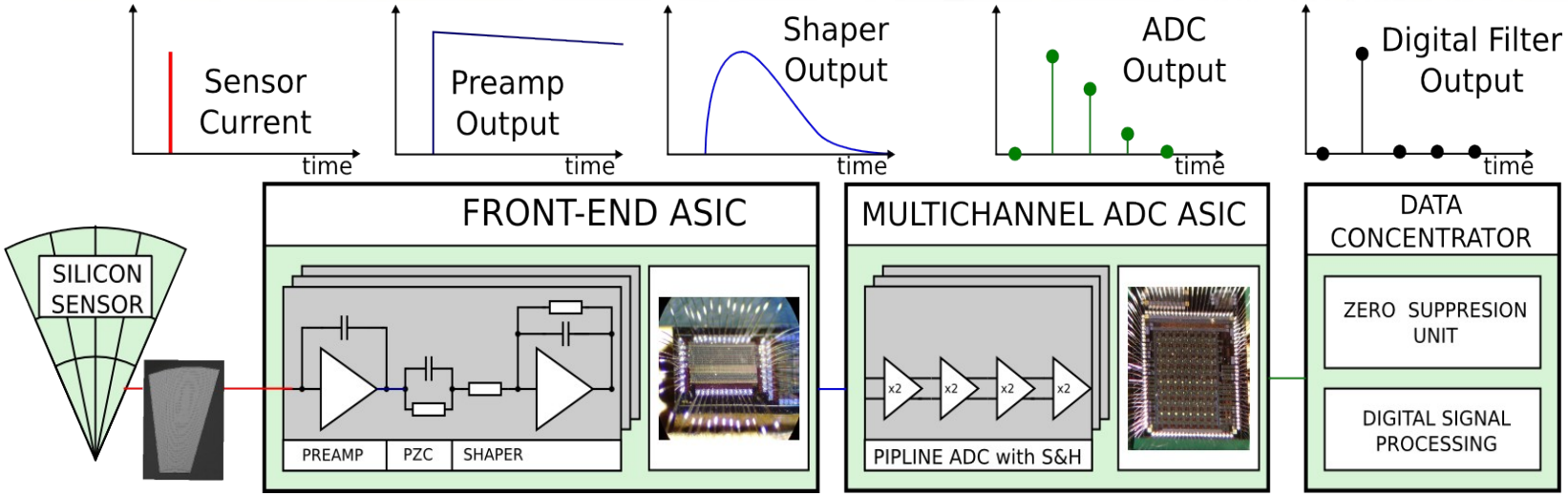
In preparation to test beam measurements:

- Four perfectly machined tungsten plates, which meet the requirements for flatness and thickness from Plansee are available now. and glued to permaglass frames. Six other "less perfect" tungsten plates (1 Plansee + 5 MG Sanders) will be also used provided resize the distance between adjacent plates of tungsten

- Also "spare sensor" (Si, GaAs) boards are glued to permaglass frames

- In the next year the readout electronics for 10 sensor layers can be available. It will contain elements of the previous front-end ASIC, (0.35 μm technology) , together with a new front-end ASIC (130 nm technology).

LumiCal detector readout chain

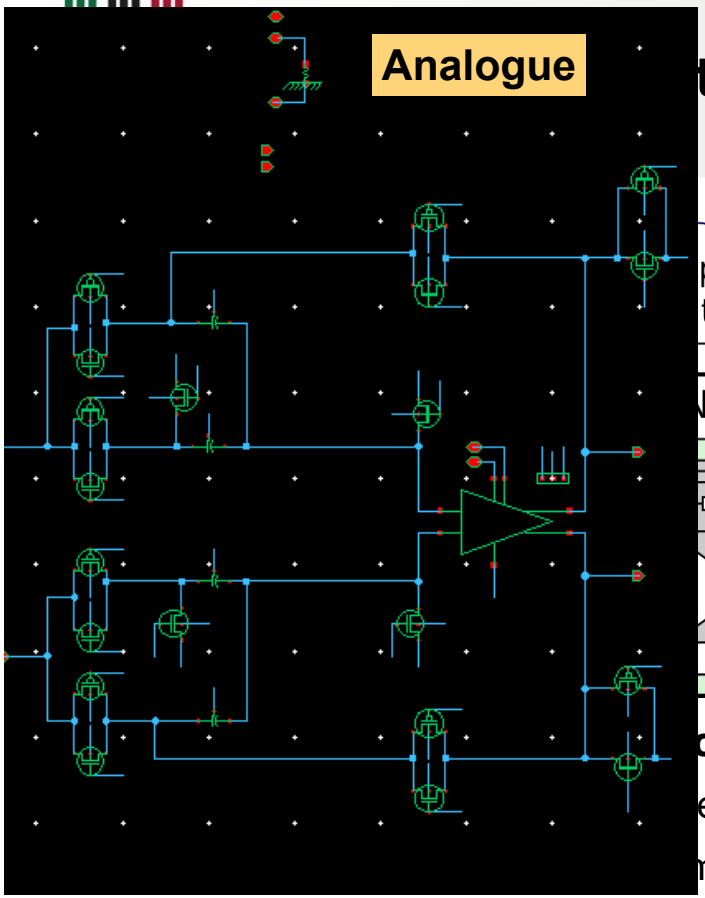


Existing LumiCal detector readout comprises:

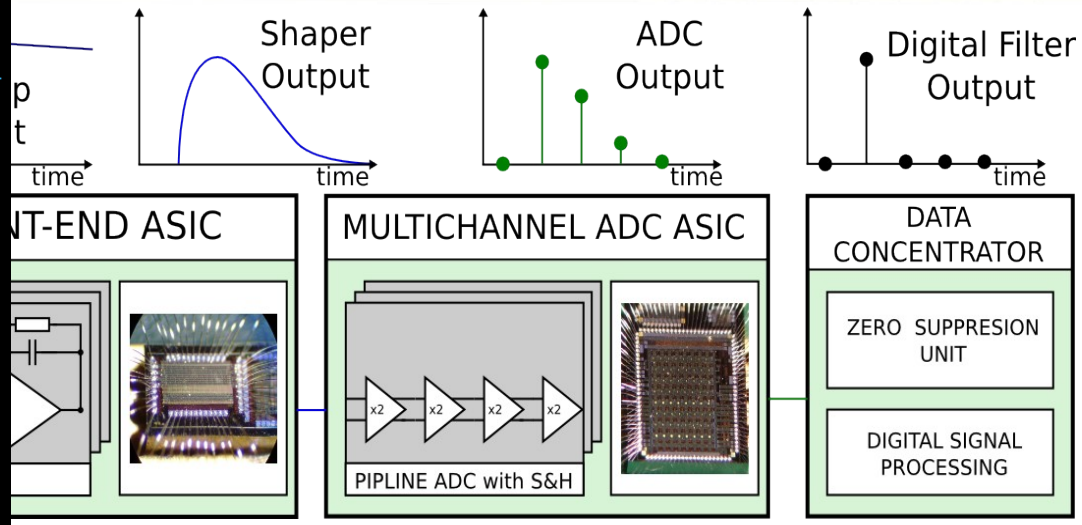
- 8 channel front-end ASIC with preamp & CR-RC shaper Tpeak~60ns, ~9mW (**AMS 0.35um**)
- 8 channel pipeline ADC ASIC, Tsmp<=25MS/s, ~1.2mW/MHz (**AMS 0.35um**)
- FPGA based data concentrator and further readout

New developments for LumiCal detector readout:

- Prototype front-end ASIC **in IBM 130 nm under development…**
- Prototype SAR ADC ASIC **in IBM 130 nm under development…**



tor readout chain



out comprises:

eamp & CR-RC shaper Tpeak~60ns, ~9mW (**AMS 0.35um**)

mp<=25MS/s, ~1.2mW/MHz (**AMS 0.35um**)

d further readout

submitted February 2013

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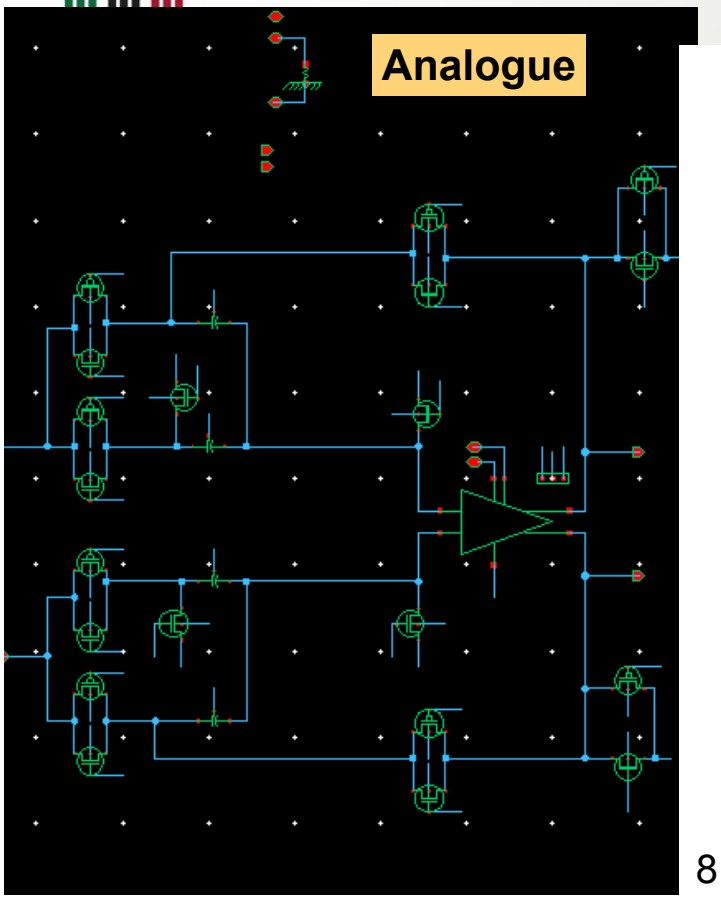

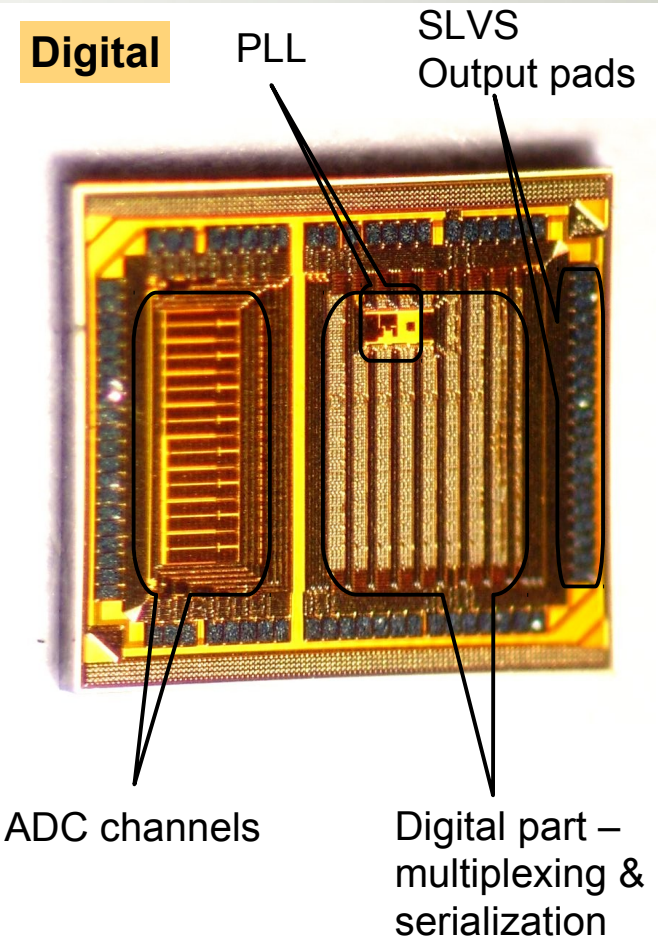

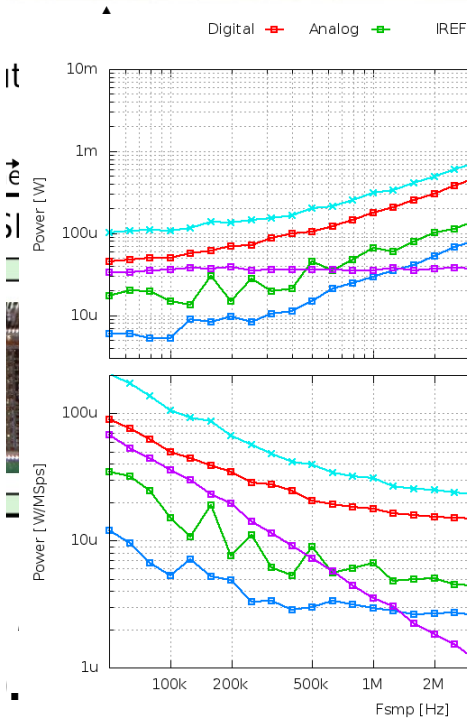

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Front end electronics

AIDA WP9.5: MILESTONES and SCHEDULE

- **Schedule presented at the AIDA Kick Off meeting**

  2011: Characterization of the 2nd generation ROC Chips
  - Dedicated run produced in **March 2010**
    - 25 wafers received in June
    - 20 000 chips packaged in the US

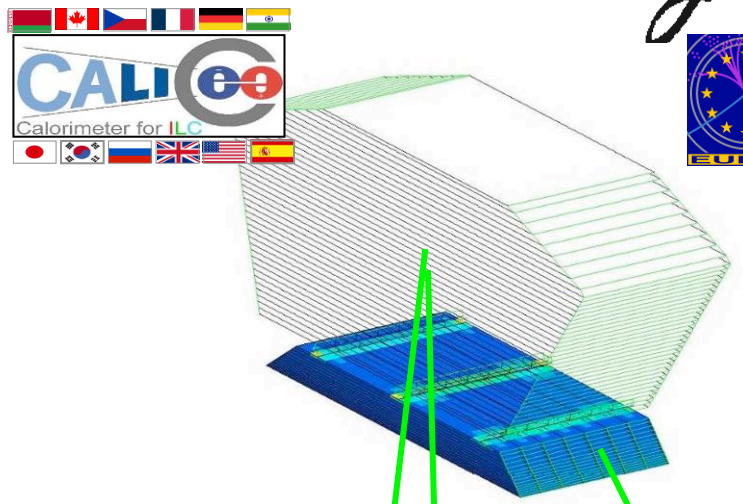
  ~~2012~~ Feb 2013: Submission and test of one of the 3rd generation chips

  ~~2013~~ 2014 ?: Submission of a second 3rd generation chip

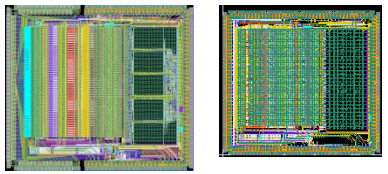
  August 2013: Report

- Budget for 3rd generation of electronics:
  - 31k€ (ECAL) + 50 k€ (Hadronic Calorimeter) => 2 chip submissions
  - 30 ppm

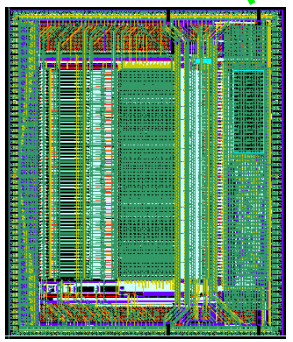
- Cost:
  - Multi Project runs (MPW): 1k€/mm2
  - Packaging: $3500
  - Testboard: 1500 €



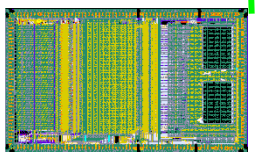
HARDROC2/MICROROC
SDHCAL RPC/µMEGAS
64 ch 20 mm$^{2/}$



SKIROC2
ECAL Si
64 ch. 65 mm^2



SPIROC2
AHCAL SiPM
36 ch 32 mm^2



0.35µm SiGe AMS technology

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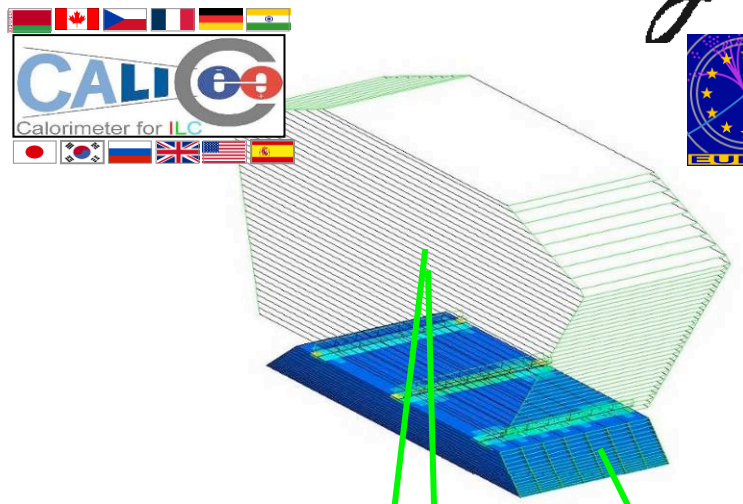

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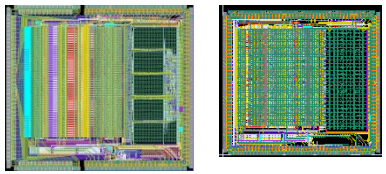

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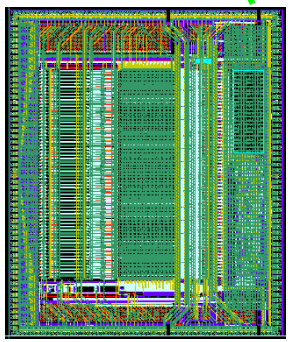

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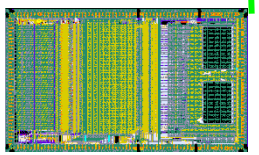
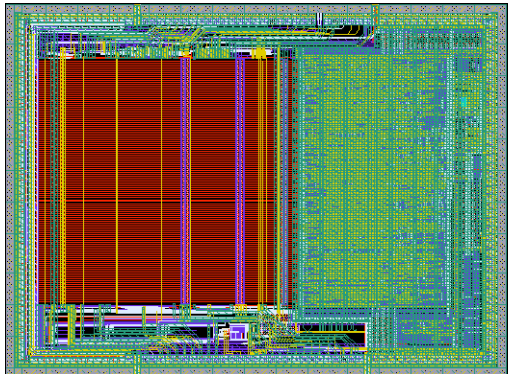


0.35µm SiGe AMS technology

HARDROC3

- HARDROC3: No major modifications needed in the FE
  - submitted at the end of Feb 2013 (SiGe 0.35µm), expected in June 2013
  - Die size ~30 mm2 (6.3 x 4.7 mm2)
  - To be packaged in a TQFP208
  - **64 independent channels**
  - **I2C link (@IPNL)**
  - PLL: integrated before in a builiding block, first measurements are very good
    - Input frequency 2.5 MHz =>output frequency: 10, 20, 40, and 80 MHz available
  - Bandgap: new one with a better temperature sensitivity, tested in a building block
  - Temperature sensor: tested in a building block, slope – 6mV/°C
  - 2013: dedicated to the test of HR3 before submitting other chips



2nd chip submission was planned to be SPIROC3 - under discussion

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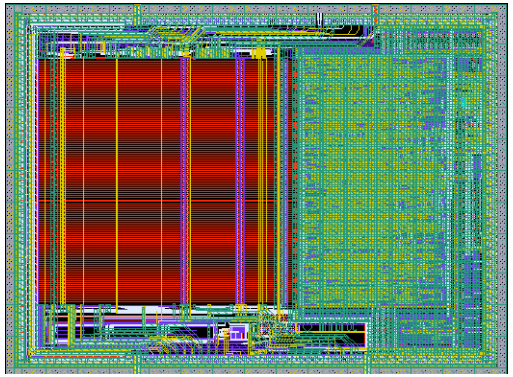

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ECAL

2013 beam tests

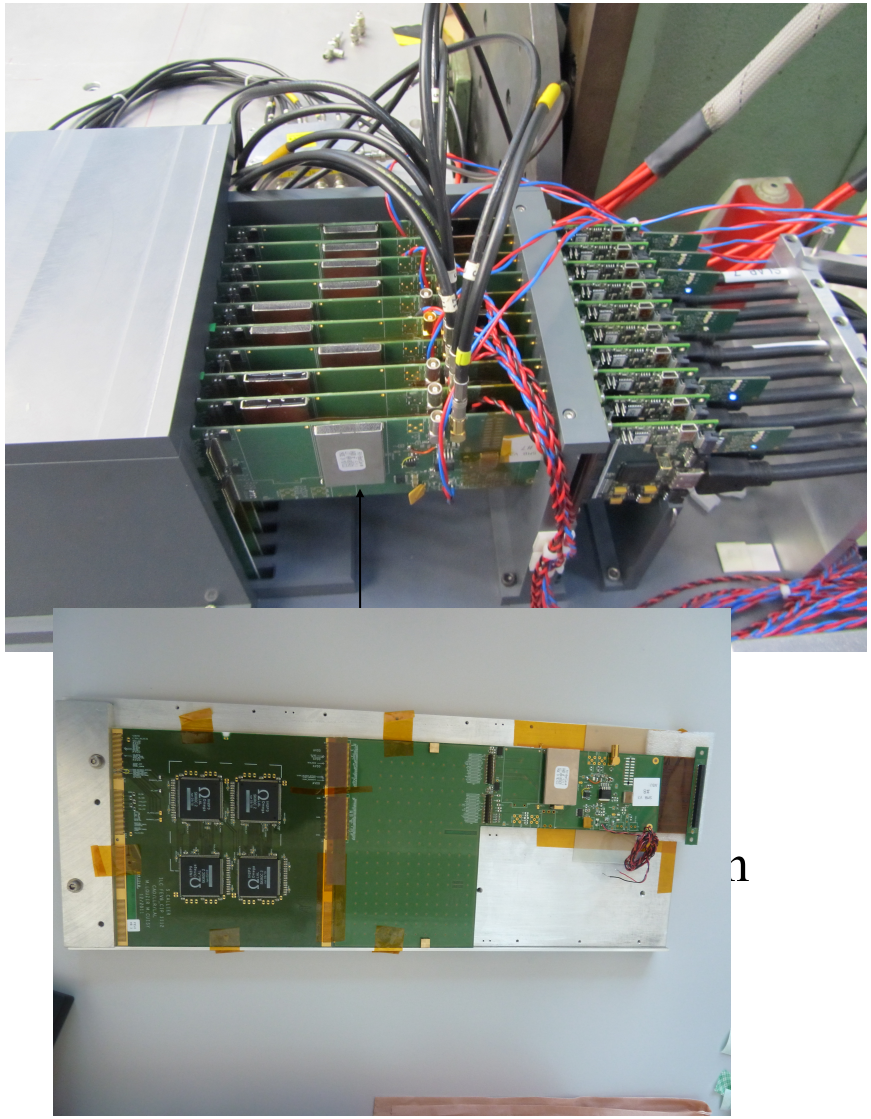
Alltogether 10 layers

- 4 continous operation
- 4 power pulsed
  Including h/w modifications see above
- 2 could not be reliably operated

DAQ: Readout by 2 LDAs

Power pulsing
Duty cycle 99%, 10Hz

Operation in power pulsing
Mode requires removal of
Decoupling capacitances
=> Do not expect as stable
performance as in continuous mode



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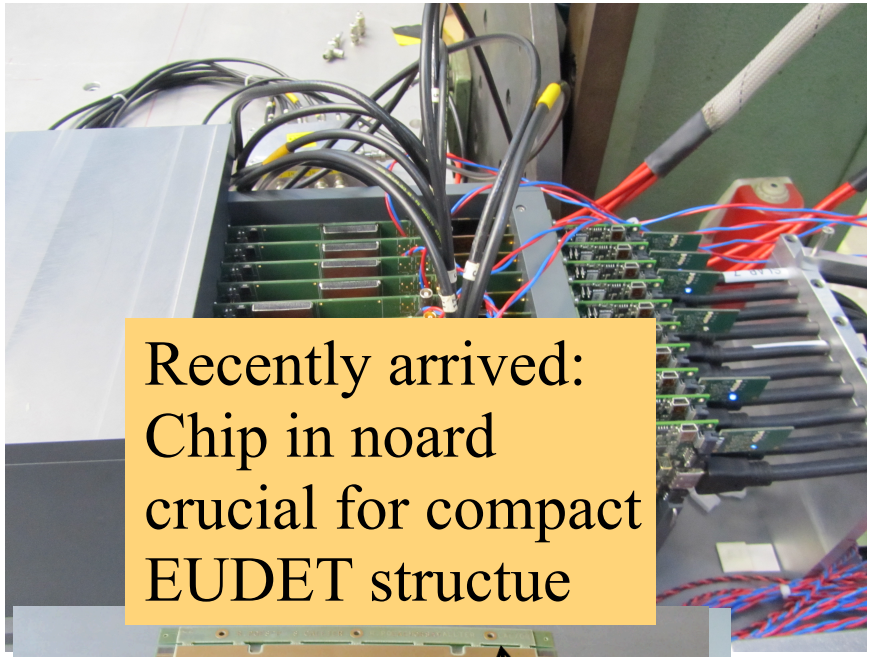
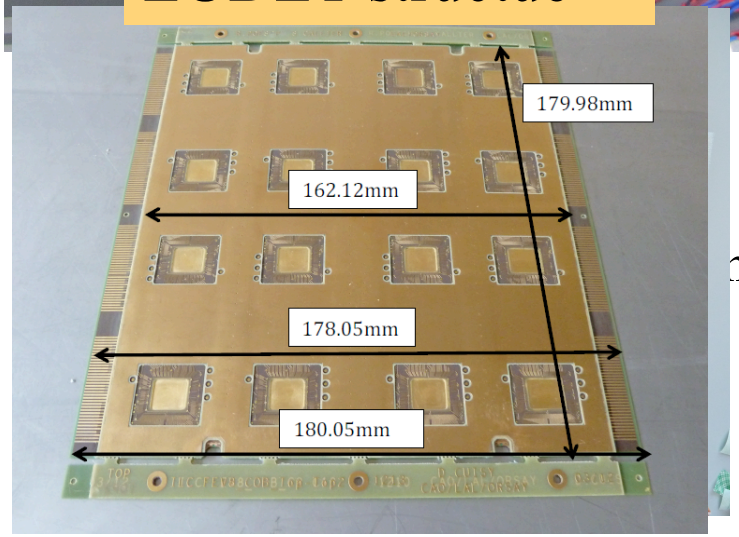
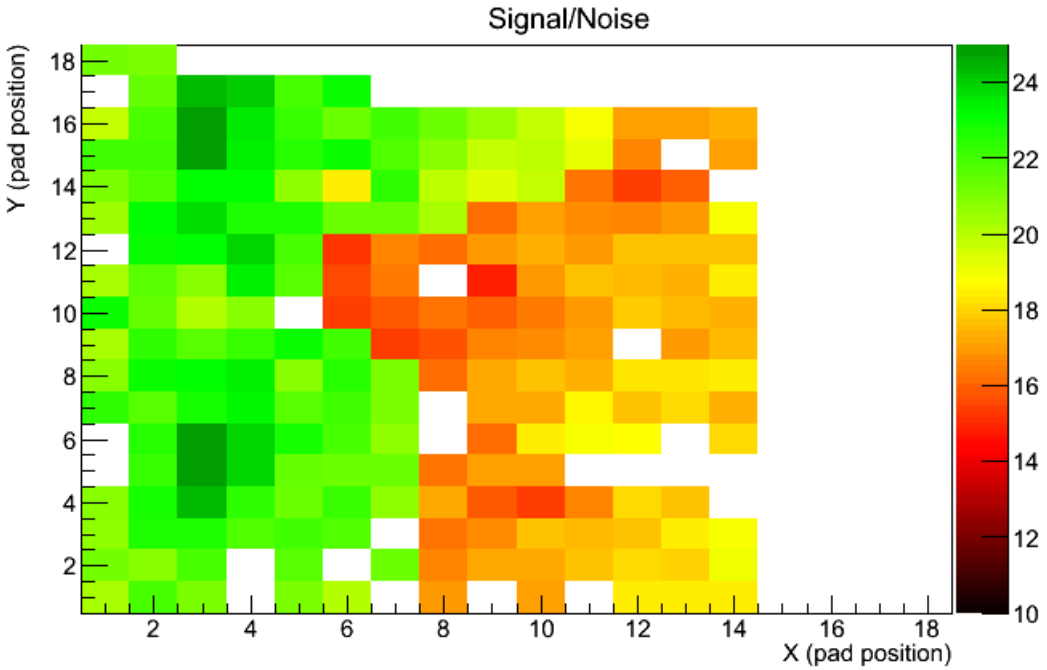


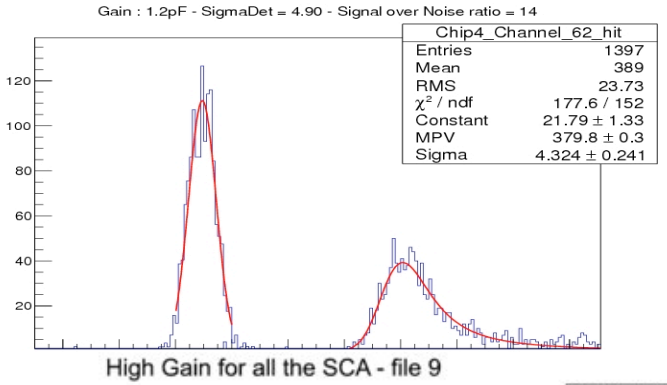
Recently arrived:
Chip in noard
crucial for compact
EUDET structue



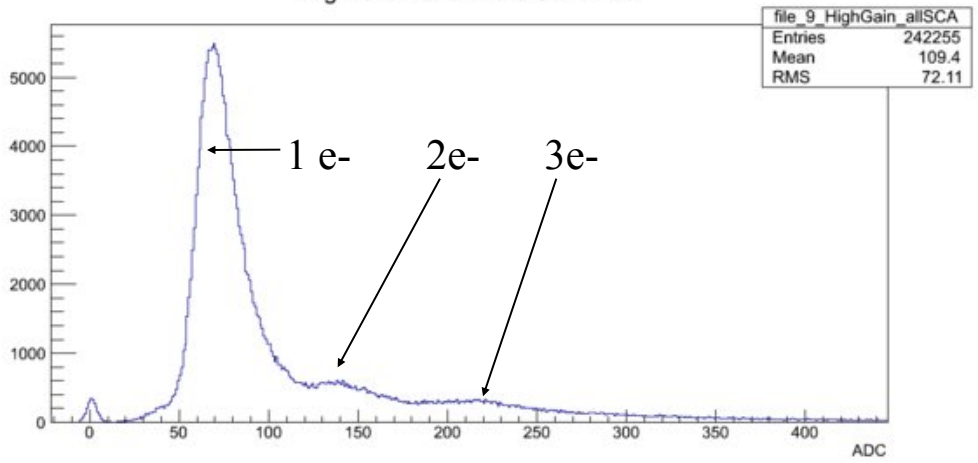
Data Analysis 2012 – Signal over noise ratio



Results after setting of trigger thresholds and event filtering (see backup slides)
White spots = Noisy cells
noice induced by PCB routing

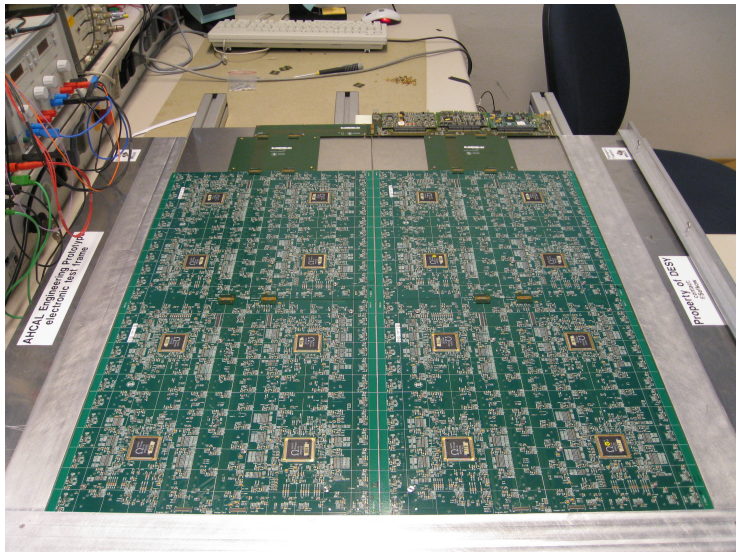


S/N > 10
(for all gains available with SKIR
R&D target is 10:1



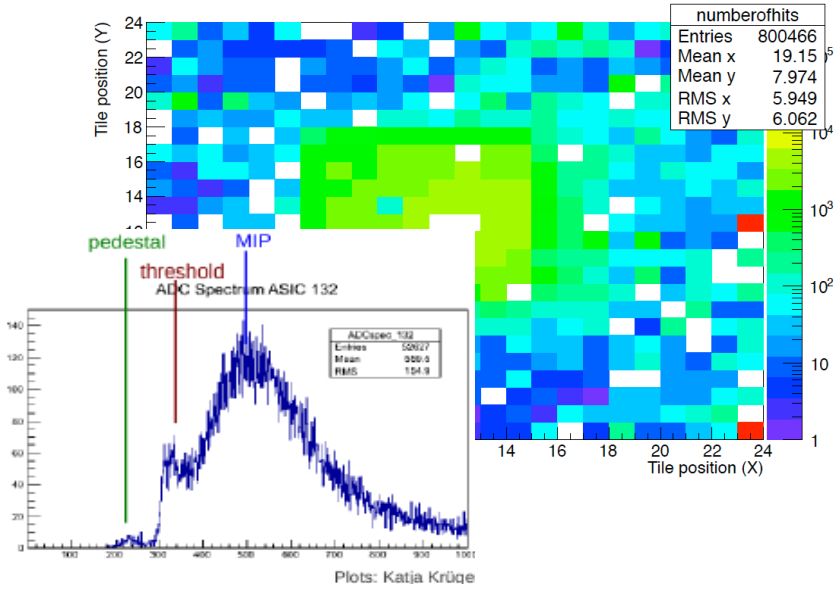
AHCAL

Current AHCAL engineering prototype

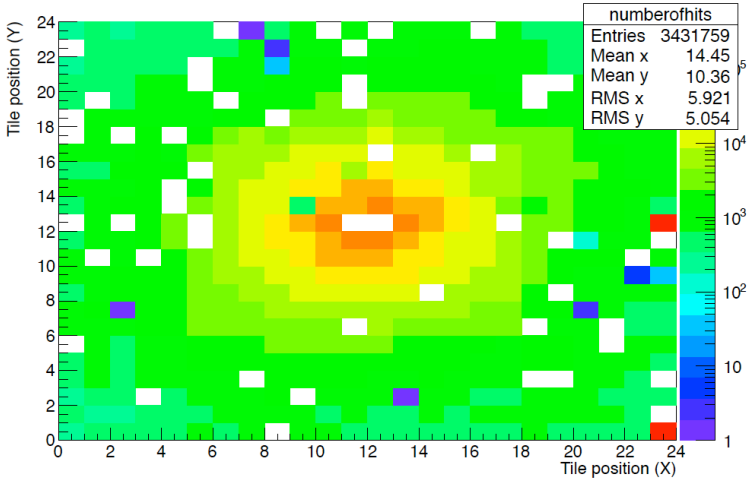


- 1 layer with 4 HBU2s fully equipped
- calibrated in the lab and in electron beam at DESY
- 10 days of muon and hadron test beam behind DHCAL at CERN in Nov. 2012
  - demonstrate feasibility of detector calibration and operation **in auto-trigger mode**
  - demonstrate time measurement capability

μ 180 GeV Number of hits

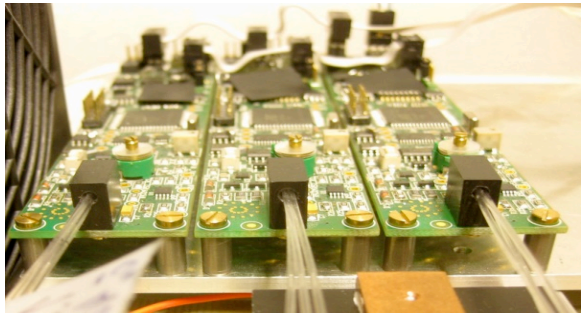


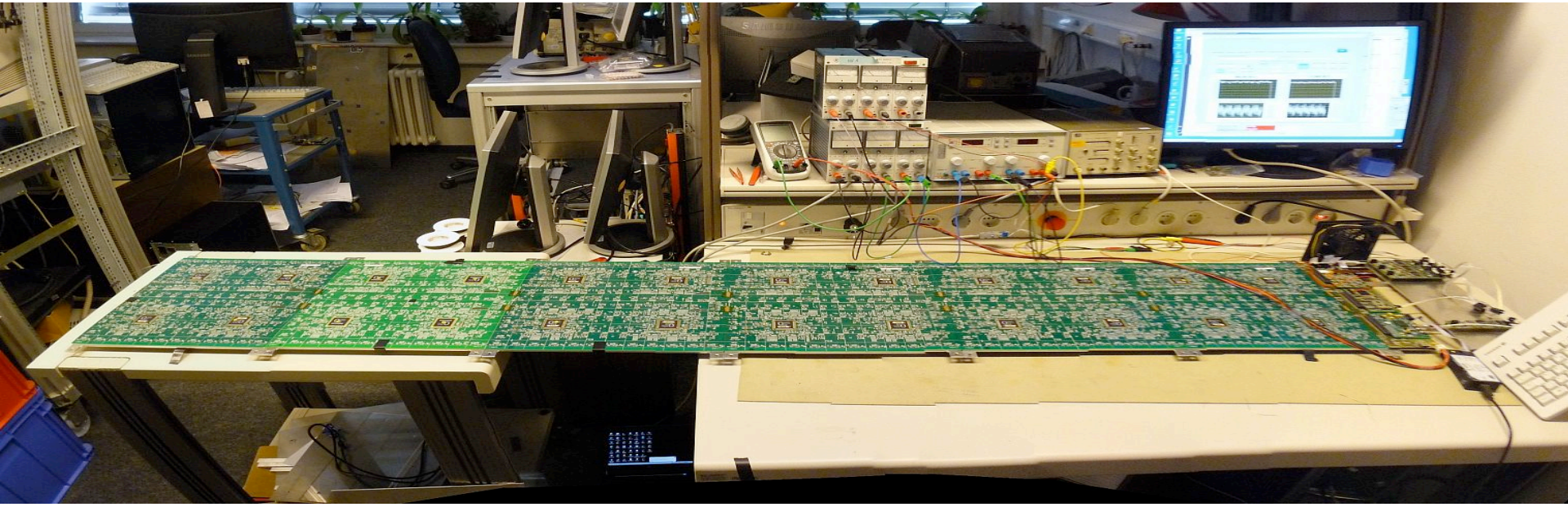
π 180 GeV Number of hits

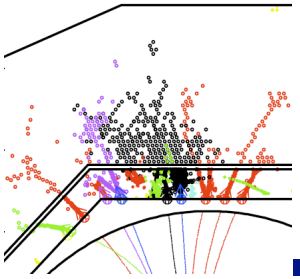


LED calibration system

- 1 LED illuminating many tiles by fibres (Prague)
  - 1 LED illuminates 3 fibres with 24 notches each (→ 72 tiles per LED)
  - new driver boards
  - tested with full slab (6 HBUs, 5 equipped with tiles)
  - successfully tested in lab, gain measured for 92% tiles in a single run







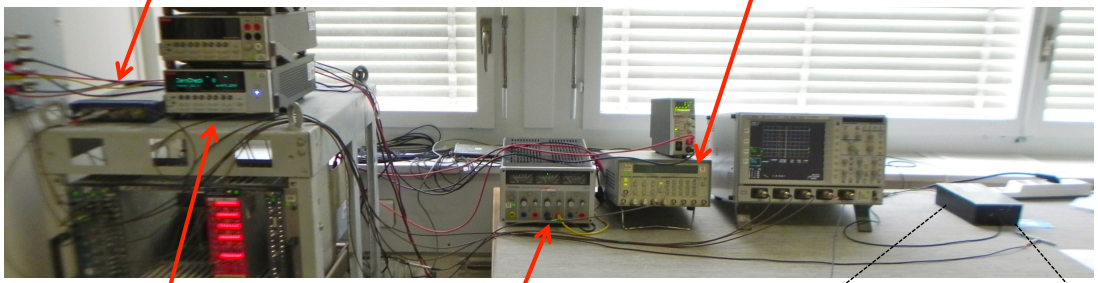
Adaptive power supply

- Started at Bergen, Prague, support from CERN, MPI-M

Setup in CERN LCD SiPM lab

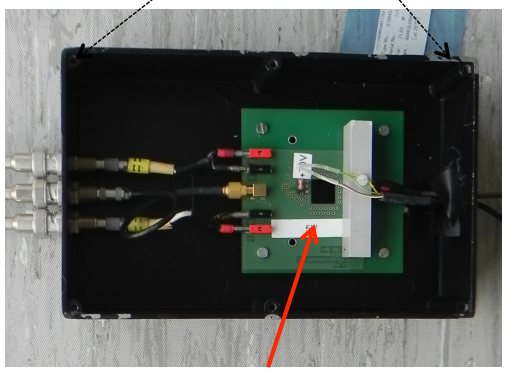
Digital oscilloscope – readout by PC with T3B DAQ

Pulse generator for LED



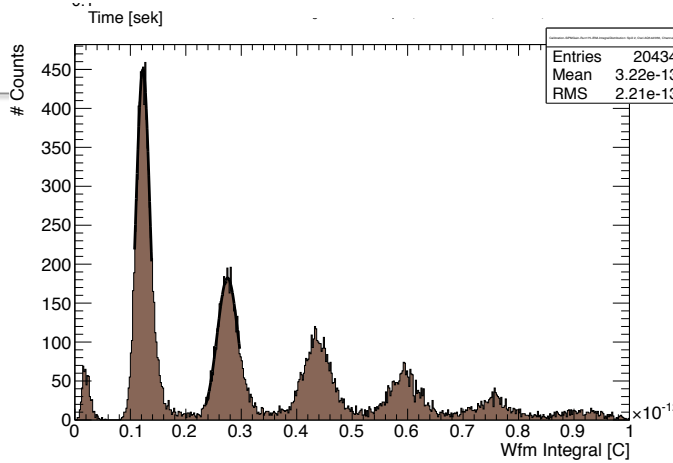
Keithley 6517B
Bias V source

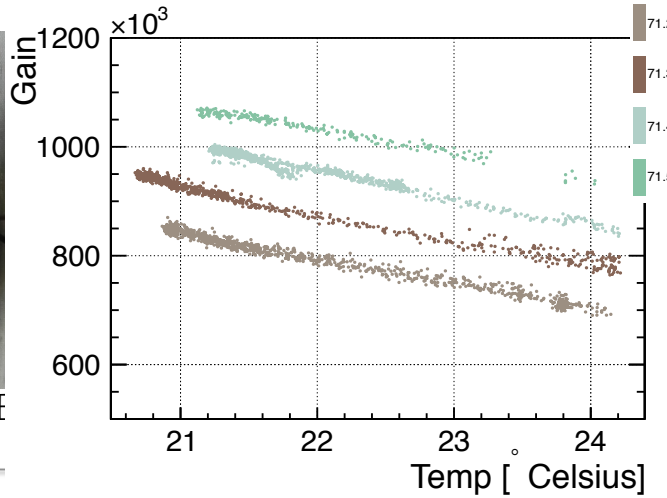
LV source



SiPM + preamp + T-sensor + LI

- Picoscope bought by CERN LCD with WP9.5 money (see other talk)
- Thanks to T3B team @MPI Munich, had a working DAQ within a day



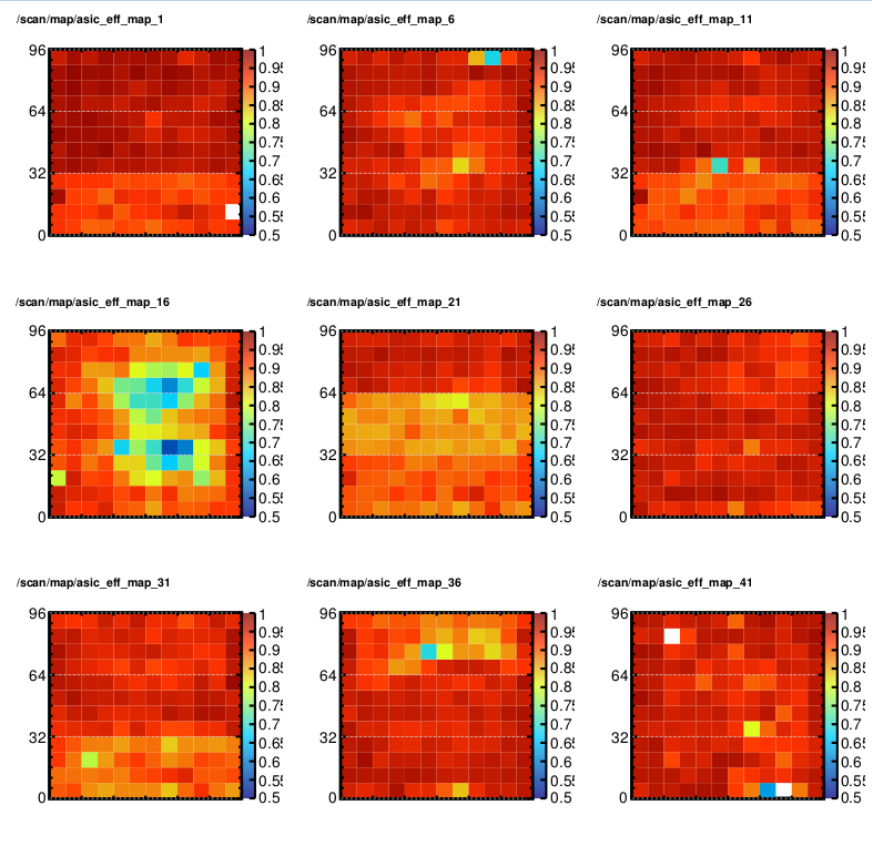


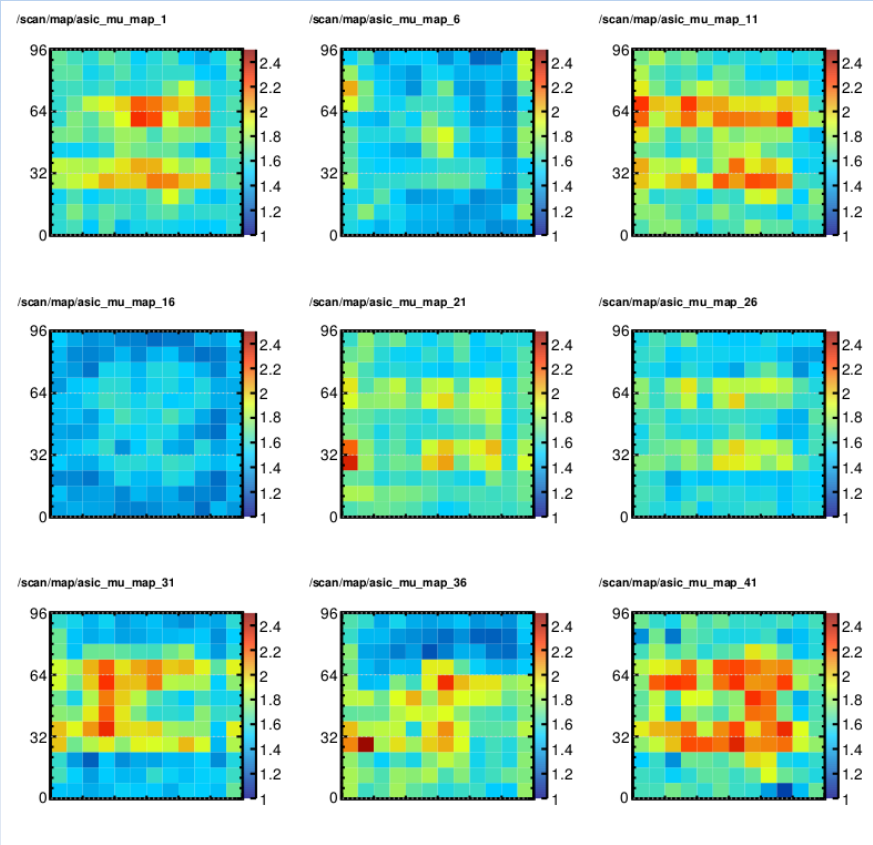
DHCAL

RPC: Efficiency & Multiplicity estimation

ASIC's efficiency & Multiplicity maps for few layers

Courtesy of Y. Haddad (LLR)



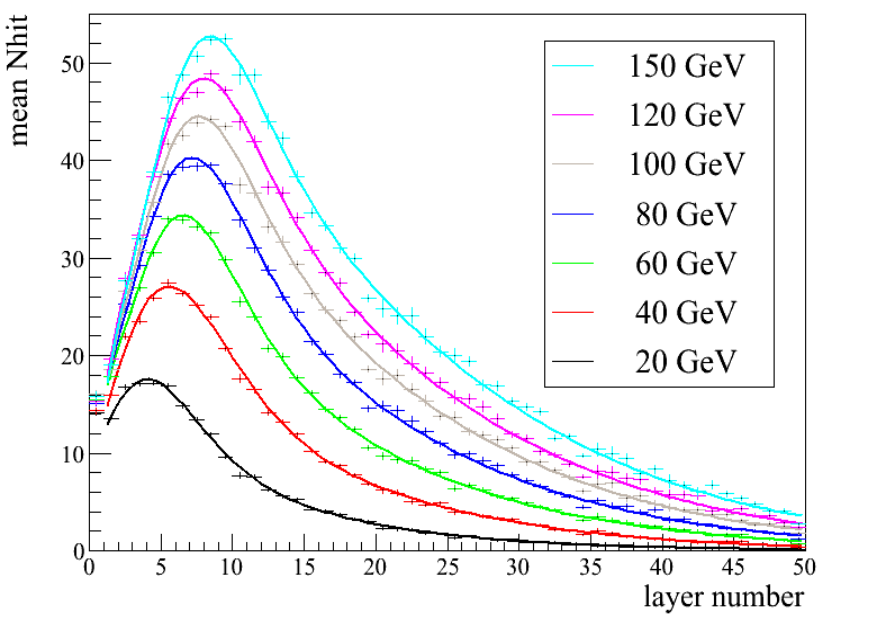


towards local calibration and optimised resolution

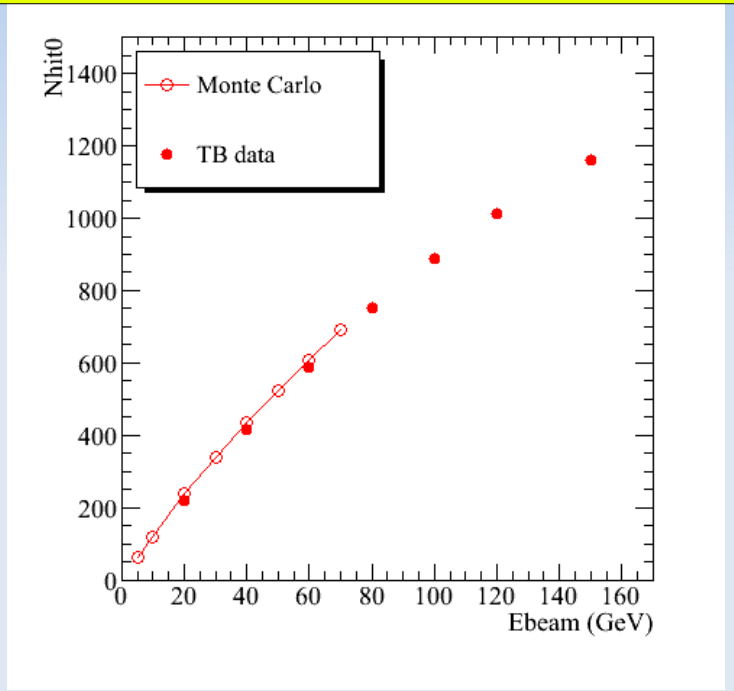
Results (2/2): calorimetry measurement in SPS/H2

Courtesy of Max. Chefdeville (LAPP)

Longitudinal profile of pions showers



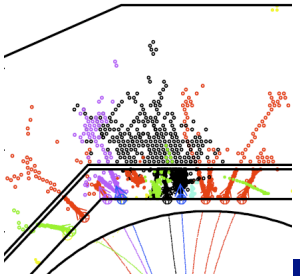
Comparison data/Monte Carlo



Inside the SDHCAL: 46 RPCs + 4 Micromegas

Use RPCs to identify the shower start and measure the number of hits in the Micromegas
→ Obtain shower profile with a virtual 50 layer Micromegas SDHCAL!

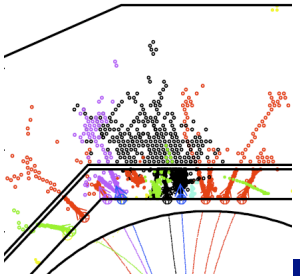
Calculate response of a virtual Micromegas calorimeter to pions by integration of the profile
→ Expected saturation is observed and compares well with Monte Carlo predictions!



Summary

- Many new nice results reported
- Milestones coming closer
- Thanks to the wisdom of proposal editors, WP 9.5 appears on track
- Overall progress is slowed down, proportional to resources
  - EUDET : AIDA = 3 : 1
- DAQ getting critical
  - AHCAL, FCAL

Back-up



Partners

- CERN
- UCL - Louvin
- IPASCR - Prague
- CNRS
  - IPNL Lyon
  - LAL Orsay
  - LAPP Annecy
  - LLR Palaiseau
  - LPC Clemront
  - LPSC Grenoble
- DESY
  - UHEI (third party)
- MPG-MPP Munich
- Wuppertal
- TAU Tel Aviv
- UIB Bergen
- AGHUST Kracow
- IFJPAN Kracow
  - CIEMAT Madrid (3rd p)

SUMMARY

- **Nice TB results obtained with all the ROC chips, in AUTOTRIGGER mode**
  - Complete system, large dynamic range, low noise
  - Tests with power pulsing mode

- **End of Feb 2013: submission of HARDROC3**
  - « Simple » chip compared to Skiroc and Spiroc: I2C, independent channels, circular memory, one register/channel, temperature sensor
  - package: TQFP208 instead of TQFP 160 for HR2
  - ⇒ **New 2-3 m RPC chamber to be built to test HR3 at the system level**
  - Die size ~30 mm2 => 30 k€ + 5K test setup (AIDA funding)
  - Tests should start at the beginning of June 2013 -> **Report for August 2013**

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  - Spiroc2b: pedestal shift
  - Spiroc2c: Very good analog performance (building block wo the digital part) BUT sensitivity to digital coupling through substrate. Pedestal shift (with large signals and external trigger) reduced but still things to be understood

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- **SPIROC3 and SKIROC3 : Complex chips**, many parts still to be tested on test bench and at the system level
  - I2C, independent channels but also new PA, TDC , SCA
  - Hardroc3 test feedback necessary before submitting Spiroc3 and Skiroc3
  - Size should be ~43 mm2 (spiroc3) and 81 mm2 (skiroc3)=> Dedicated run necessary to complete AIDA funding
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