SALTRO TPC readout system

Presented by
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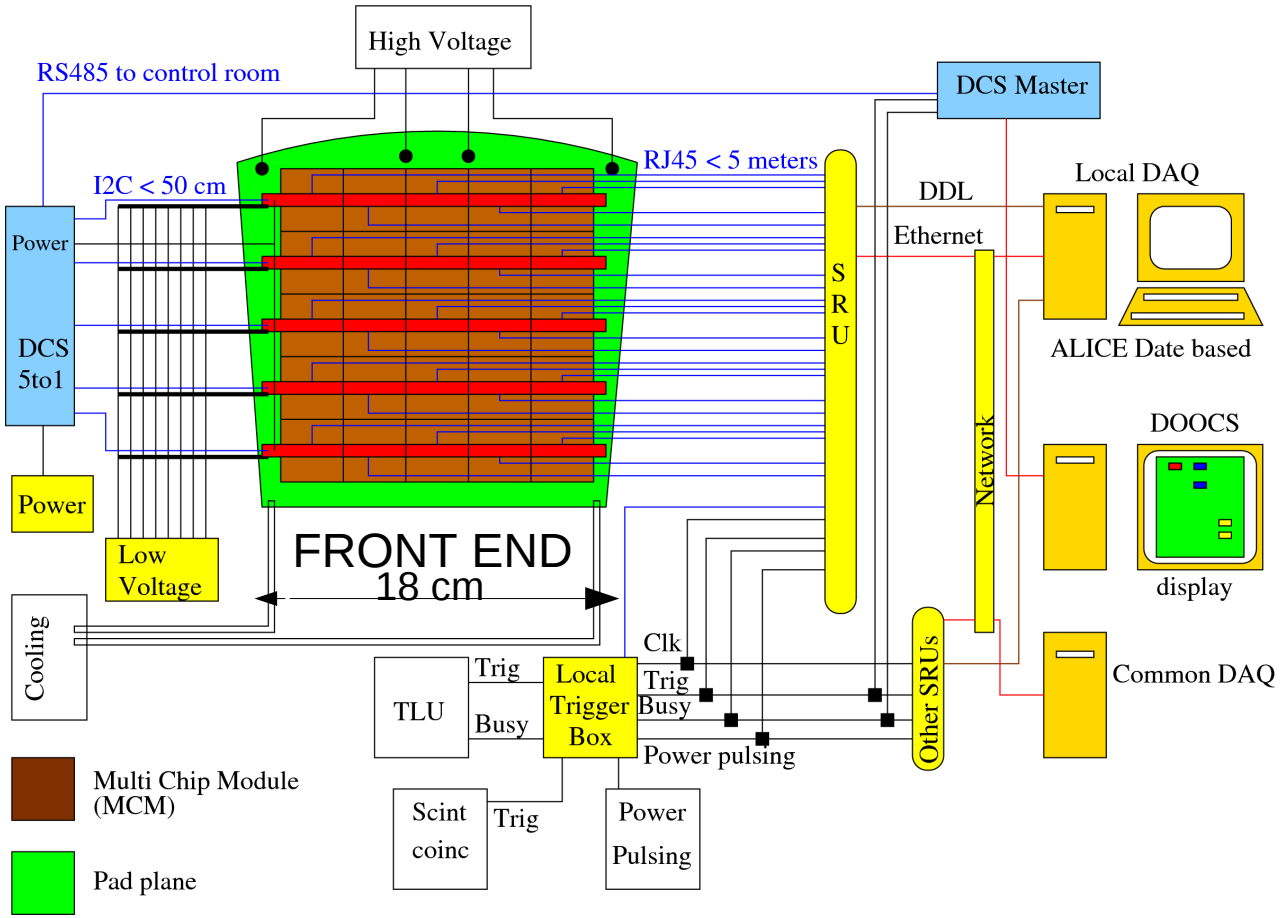
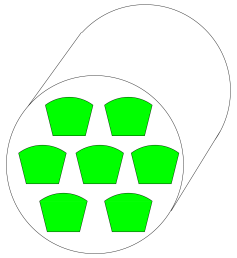
- Overview of current design
- The Front End Multi Chip Module (MCM)
- Low Voltage (LV) system
- Detector Control System (DCS)
- Serial Readout Unit (SRU) & Trigger & Power Pulsing
- DAQ system
- Status & Time scale

Overview



CONTROL TRIGGER DAQ



LCTPC ENDPLATE

7 pad plane modules

Front End = 25 MultiChipModules connected on a pad plane

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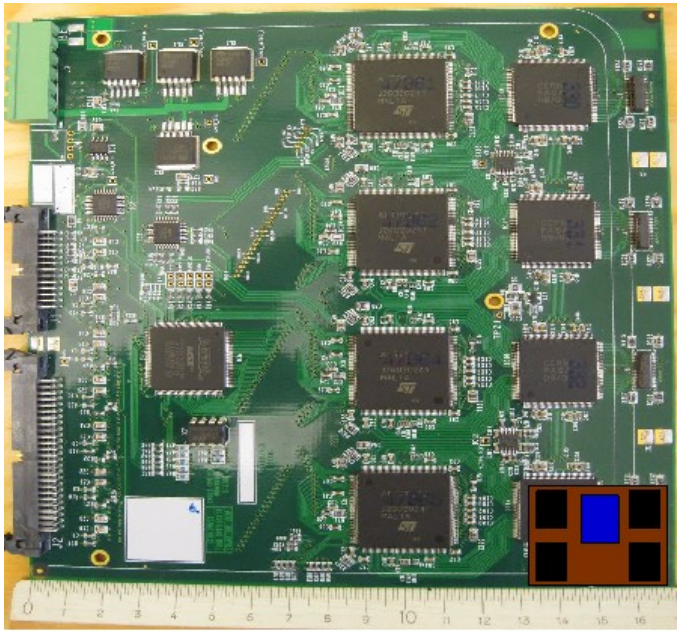
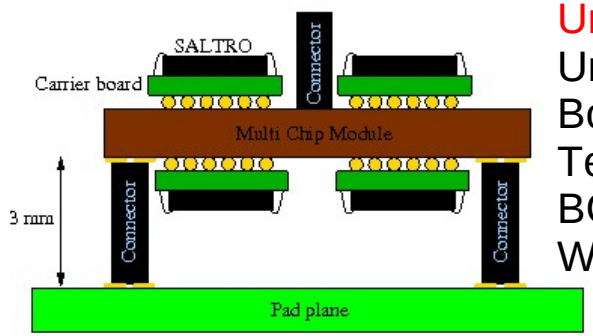
Multi Chip Module (MCM)



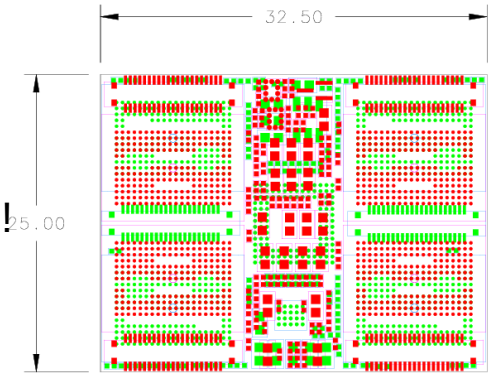
Current:
FEC = 8 ALTRO + 8 PCA16
128 channels
Parallel readout bus
17*18 cm
FPGA board controller

Multi Chip Module (MCM) = 8 SALTRO
128 channels
Serial readout
2.5*3.5 cm
CPLD (firmware Brussels)
"same" except Low Voltage



Side view NOT TO SCALE

Untested &
Unpackaged chip
Bonded on Carrier
Test (unknown yield)!
BGA on main board
With industry



Component placement

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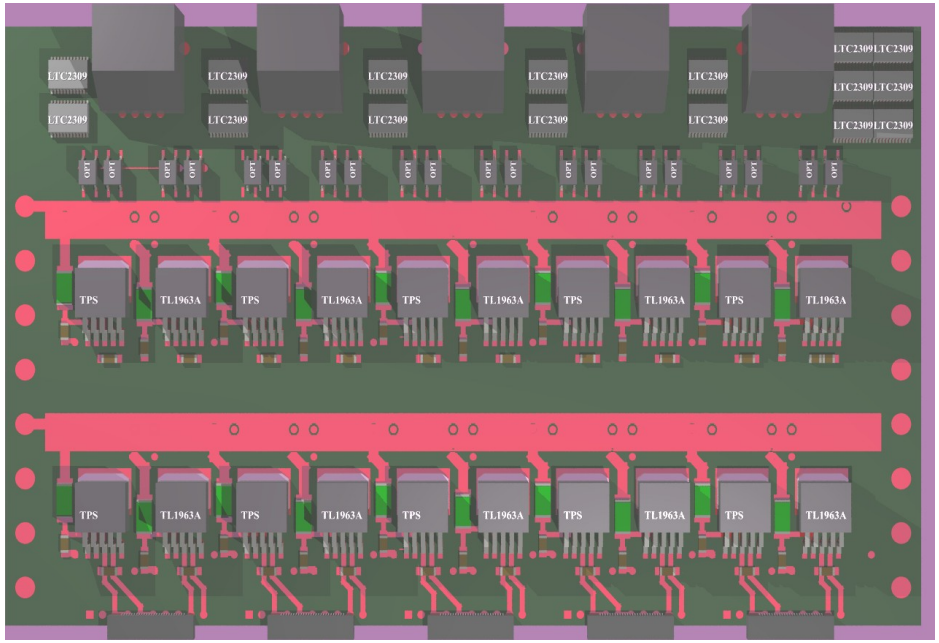
Low Voltage Card

5 MCM * 8 Voltages = 40 regulators



MCM1 MCM2 MCM3 MCM4 MCM5

Control of individual regulator
On/off

Monitor on each Low Voltage card
48 voltages
40 currents
1 temperature

On each MCM
1 temperature
1 DAC

5 low voltage cards and
~700 settings/values per pad plane

Detector
Control
System

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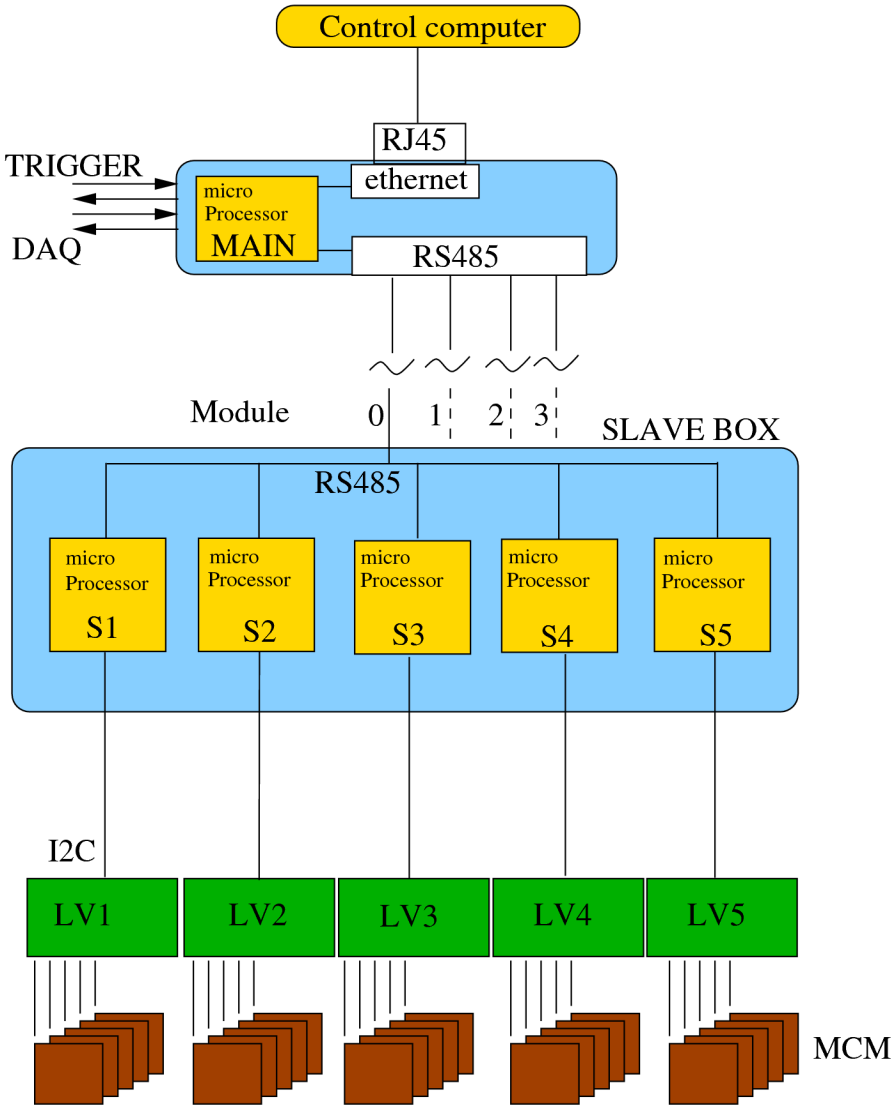
Detector Control System



In control room

Display/Logging/Control:
DOOCS (used at DESY)
(Distributed Object Oriented Control System)

STOP TRIGGER/DAQ/ALARM
How?

Near electronics

Standalone Monitoring
Automatic power off!

Expensive things!
Do not want to burn it all

370 W >>> power pulsing

110 W (regulators)

? cooling

260 W
CO2 cooling (Japan)

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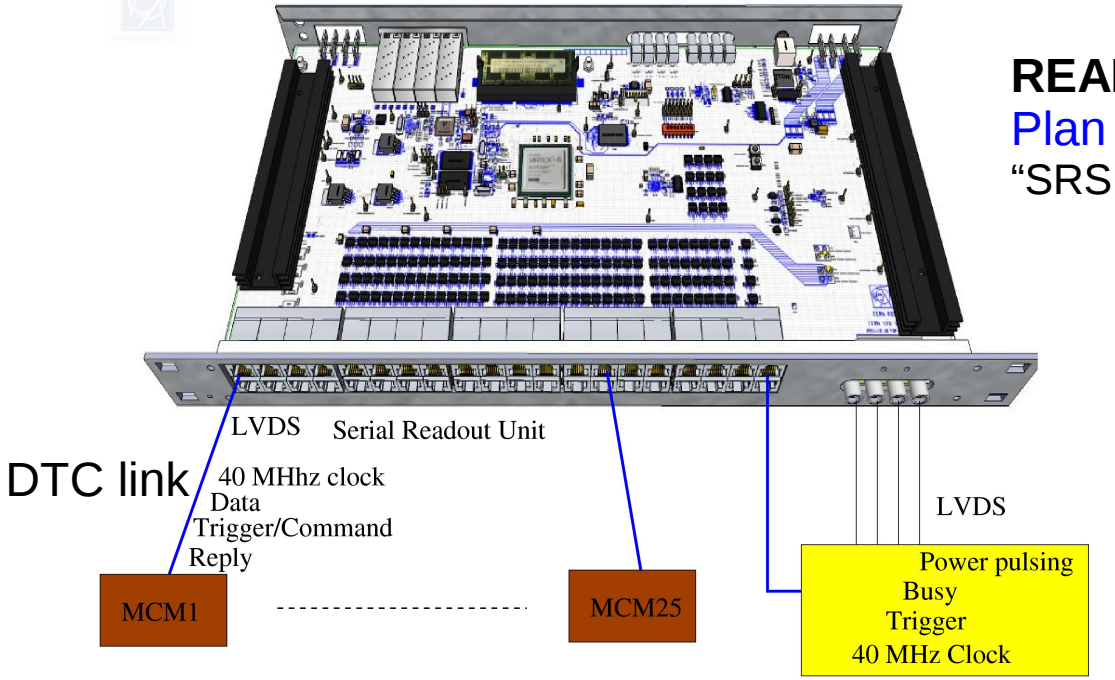
READOUT & TRIGGER

Not yet well defined



READOUT

Plan to use SRS SRU from RD51

"SRSFEC" = CPLD on MCM

Trigger

Local Trigger Box
and/or
AIDA miniTLU?

Direct DTC link with SRU?
(timestamps, clock...)

Many open questions. e.g.
How to synchronize clocks (SRUs MCMs..) < 1ns?
SRU firmware needs to be modified – by who?
…. Will go to CERN and learn how to use the SRU

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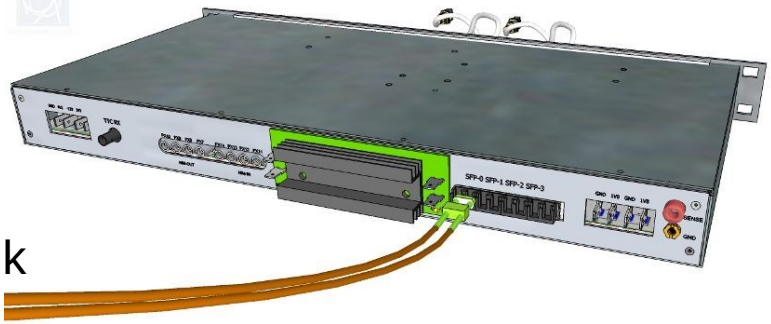
DAQ

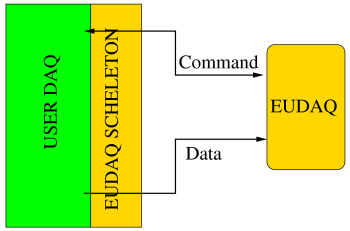
Not yet well defined

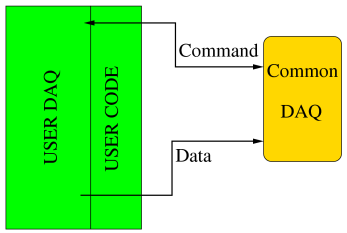


EUDET system:
Based on ALICE DATE/DDL/DRORC link
Can it be used for test setup?

AIDA system:
Plan to use ALICE DATE and 10 Gb ethernet
(DDL and 10 Gb ethernet are used in ALICE with SRU)

Common DAQ:
EUDET
problem to compile DATE routines with EUDAQ scheleton.





AIDA
instead use a well defined protocol,
to be implemented in the user code,
and no compilation with a common scheleton is needed.
(can one avoid the compilation problem with the “AIDA system”– do not know)

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STATUS

Multi Chip Module

SALTRO

- 600 untested naked chips exist

Carrier board

- design ready
- Industry collaboration to start to develop bonding/mount techniques

Bigger prototype MCM soon to be produced (with one packaged SALTRO)
Firmware started to be developed in Brussels

Low Voltage board

Design ready
Prototype board soon to be produced

Detector Control System

Hardware - design ready, soon produced
Software – in progress

DAQ

Bought one SRU – will soon go to CERN to learn
Trigger/Power pulsing/DAQ hard/software still to be defined and done

TIME SCALE

1 year - test system in beam
2 year - final system