WP3

Microelectronics and interconnection technology

Hans-Günther Moser – MPI Munich

Valerio Re - INFN

AIDA 2nd annual mmeting, Frascati, April 11, 2013

WP3 Tasks

Task 1. Coordination and Communication

- To coordinate and schedule the execution of the WP tasks
- To monitor the work progress and inform the project management and the participants within the WP
- To follow-up the WP resource utilization
- To prepare the internal and Deliverable Reports

Task 2. 3D Interconnection

- Creation and coordination of a framework to make 3D interconnection technology available for HEP detectors
- Organisation of dedicated fabrication of sensors and electronics optimized for 3D interconnection
- Construction of demonstrator detectors using 3D technology to access this technology

Task 3. Shareable IP Blocks for HEP

- Creation and coordination of a framework for the design of low and medium complexity microelectronics libraries and blocks in advanced submicron technologies to be made available to the community of users in HEP
- Organization of the design and qualification of a set of blocks using selected and qualified technologies
- Distribution and documentation of the library of functional blocks
- Organisation of regular Microelectronics Users Group meetings to exchange information, plan and coordinate actions related to the creation of a shared library of macro blocks.

3D Interconnection

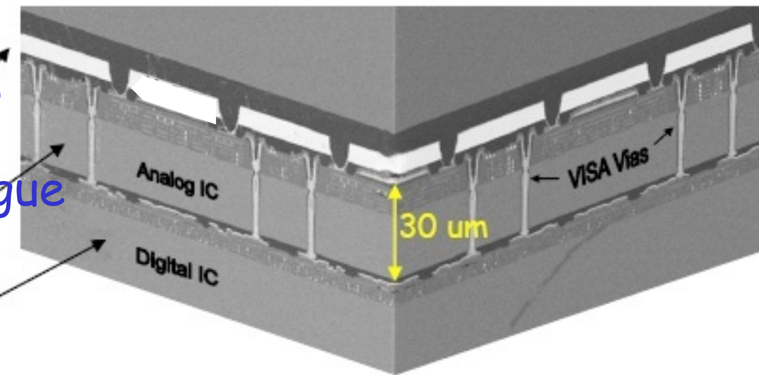
How to integrate good sensors and good electronic circuits?

3D Interconnection:

Si pixel sensor

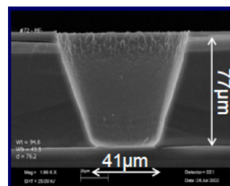
BiCMOS analogue

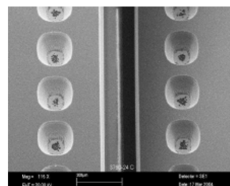
CMOS digital

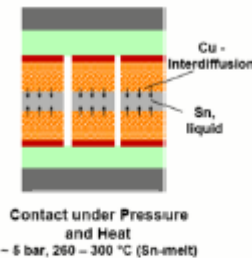


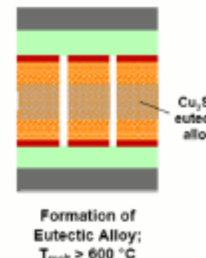
Two or more layers (="tiers") of thinned semiconductor devices vertically interconnected to form a "monolithic" circuit.

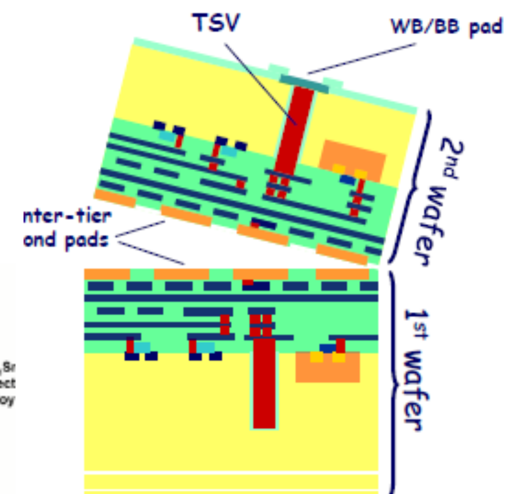
Many ways to do it











Task 2: 3D interconnection

- **Explore 3D integration of heterogeneous layers: interconnection of layers fabricated in different technologies, "via last" technique for Through-Silicon Vias.**

- Different options for the pixel sensors (high resistivity fully-depleted detectors and CMOS sensors) and for the readout electronics (130 nm and 65 nm CMOS, 3D integrated circuits)

- Different specifications for the interconnection technologies:

  relatively mature 3D processes for peripheral TSVs and for interconnection:

  high confidence level for the fabrication of demonstrators in the AIDA time span.

  more aggressive 3D processes for a low pitch (< 50 μm) for TSVs and interconnection as required to fully exploit 3D potential: higher level of risk but clear added value in view of future designs of advanced pixels (high resolution and high integration density for an intelligent pixel-level processing)

V. Re

WP3.2: 3D interconnection Sub-Projects

1) Bonn/CPPM:

Interconnection of the ATLAS FEI4 chips to sensors using bump bonding and TSVs from IZM (large diameter TSV, large interconnection pitch).

2) CERN:

Interconnection of MEDIPIX3 chips using the CEA-LETI process

3) INFN/IPHC-IRFU:

Interconnection of chips from Tezzaron/Chartered to edgeless sensors and/or CMOS sensors using an advanced interconnection process (T-MICRO or others)

4) LAL/LAPP/LPNHE/MPP:

Readout ASICs in 65nm technology interconnected using the CEA-LETI or EMFT process.

5) MPP/GLA/LAL/LIV/LPNHE:

Interconnection of ATLAS FEI4 chips to sensors using SLID interconnection and ICV (high density TSVs) from EMFT.

6) Barcelona

use a 2-tier approach to increase the fill factor of APD-sensors (based on Tezzaron/Chartered)

7) RAL/UPPSALA

Integration of a 2-Tier readout ASIC for a CZT pixel sensor using EMFT SLID technology and TSV, including redistribution of I/O connections to the backside for a 4-side buttable device.

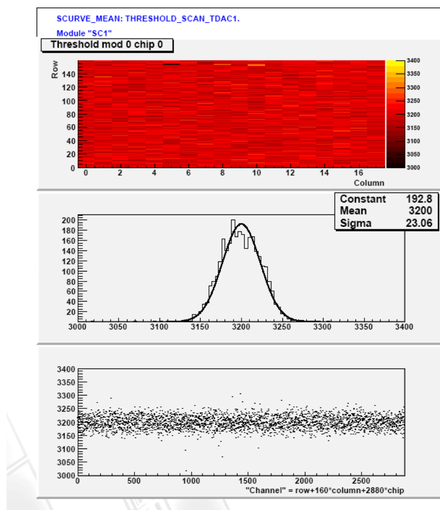
Bonn/CPPM (L. Gonella)

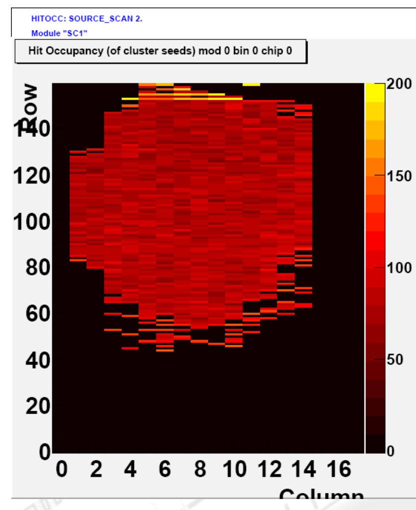
The goal of the project is to develop modules for ATLAS pixel detector at the HL-LHC using a via last TSV process

- Post-processing technology applicable on existing FE electronics
- Dead area at the chip periphery can be reduced

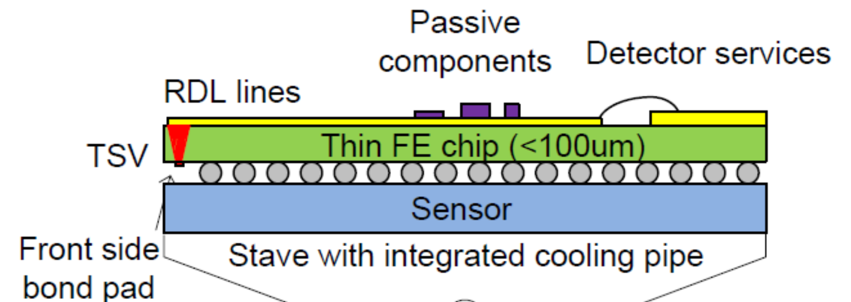
Large tapered vias by IZM, successfully tested with FEI2-based modules.

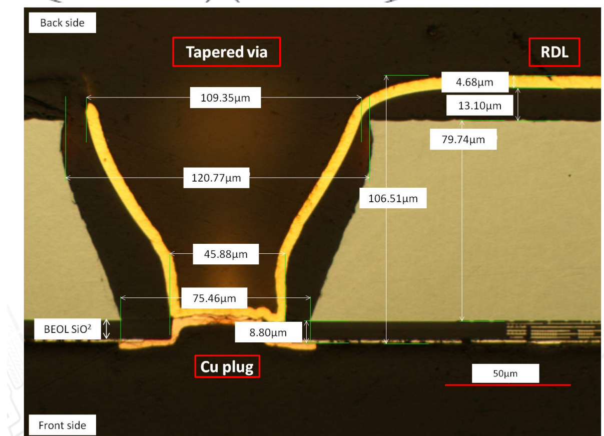
- Threshold tuning to 3200e
- Source scan with an Am-241 source





Example of TSV module

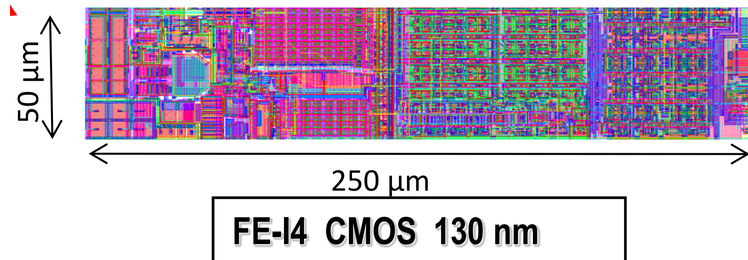




Next step: FEI4B modules with TSVs (needs handle wafer for bonding since chip is large and thin)

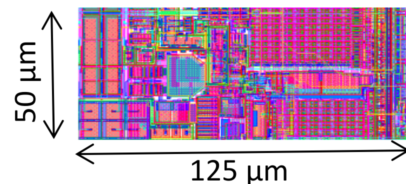
Run with IZM just started => results end of 2013

Bonn/CPPM: results on the 3D-IC run with Tezzaron GF (T. Obermann)



the analog tier : **FE-TC4-AE** : Pixel matrix of 14 x 61 pixels , pixel size 50x166 μm^2.

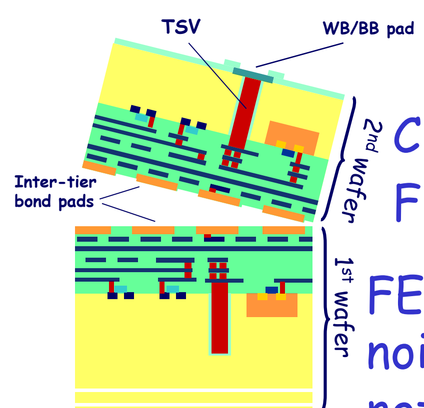
Analog tier has similar design as FE-C4-P1 (ported version of FE-I4-P1)



2 flavors of digital tier :

- **FE-TC4-DS :** digital tier with simple read-out (one-bit latch/ pixel), dedicated for studying coupling between tiers
- **FE-TC4-DC :** digital tier with complex readout "a la FE-I4" (Bonn)

130 nm 2 layers



Chip submitted in 2009/10 in the first 3D-IC MPW run

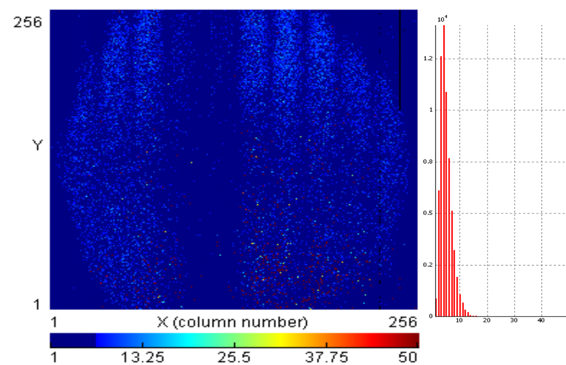
First fully functional 3D working chips in summer 2012

FE-TC4 chip samples are fully functional, with no degradation of noise performance. With appropriate shielding, digital activity does not interfere with the analog front-end.

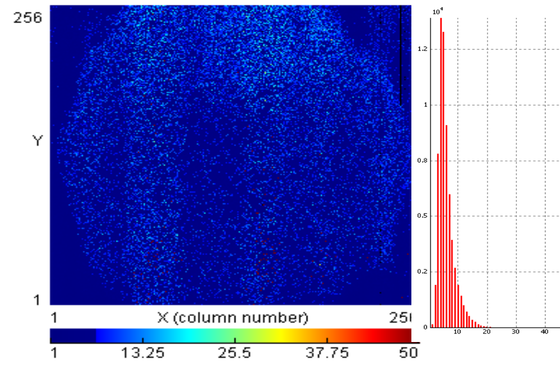
Next step: connection to a planar sensor. If hybridization on a 12 µm thinned analog tier works, a full demonstration of this 3D process will be achieved.

CERN (M. Campbell)

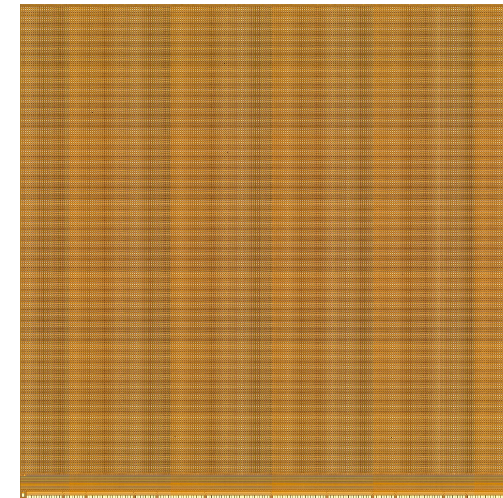
- TSVs by CEA-LETI in Medipix3 ASIC (40μm diameter, 3:1 aspect ratio
- Phase I: TSV processing on Medipix3 wafers (done , good yield and performance)



Before TSV



After TSV



All IO logic and pads contained within one strip of 800μm width

All IO´s have TSV landing pads in place

Permits 4-side butting

94% sensitive area

- Phase II; Hybridization of the TSV processed chips

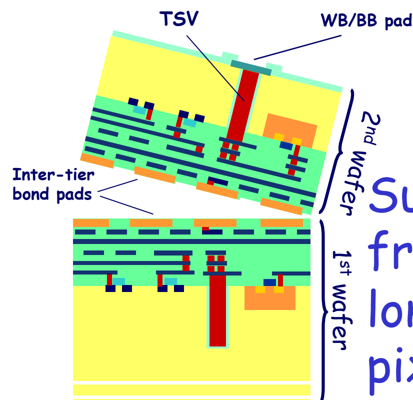
  Flip chip interconnection to sensors (first assemblies received from VTT/ADVACAM)

- Phase III: Demonstrator Module

  demonstrate multichip module operation

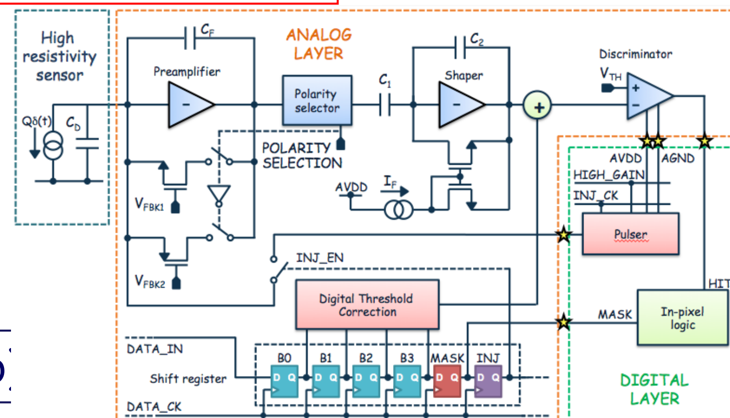
INFN (L. Ratti)

- Multi-tier pixel sensor resulting from the 3D integration of a readout chip and of a sensing layer



CMOS readout chip, based on a 130 nm vertically integrated process (Tezzaron/Globalfoundries)

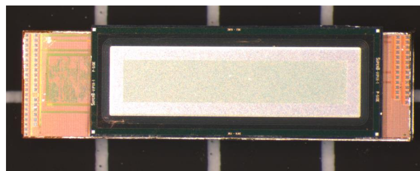
Successful tests on MAPS chips from the first MPW run (but very long turnaround time, low yield); new pixel readout chip being designed, hope to submit by end of this year



vertical interconnection process (μ-bumps by T-Micro)

Very high interconnect density (15 or 5 μm pitch)

Preliminary tests starting on 2D 130nm readout chip and planar n-on-n pixel sensors



edgeless (or 3D slim edge) fully depleted, planar silicon detector (from FBK, Trento)

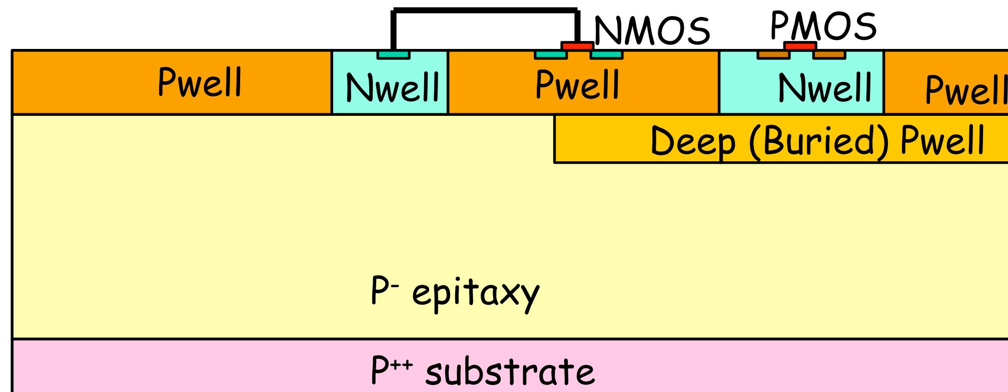
Active edge prototypes under test, nproduction of new sensors starting soon

CMOS sensing layer (XFAB, 350 nm, or an alternative process in 180 nm)

See next talk by W. Dulinski (IPHC)

IPHC (W. Dulinski)

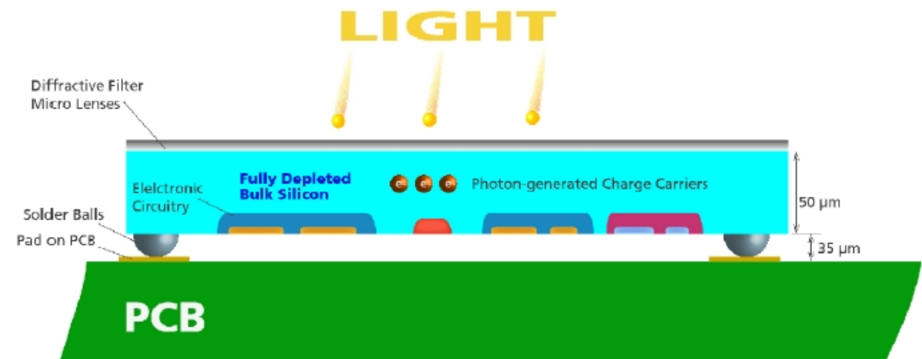
TOWERjazz® CIS 0.18 μm CMOS, 18 μm thick, > 1 kΩ cm epi layer, quadruple well process (both NMOS and PMOS allowed on pixel array)



Wafer Cross Section

Depletion of high-resistivity active layer for higher radiation hardness and thicker sensitive region possible with AC coupling between small pixel diode and front-end amplifier

Alternatives for thick high-resistivity substrate are available (ESPROS: detector grade, n-type,fully depleted 50 μm thick bulk silicon)

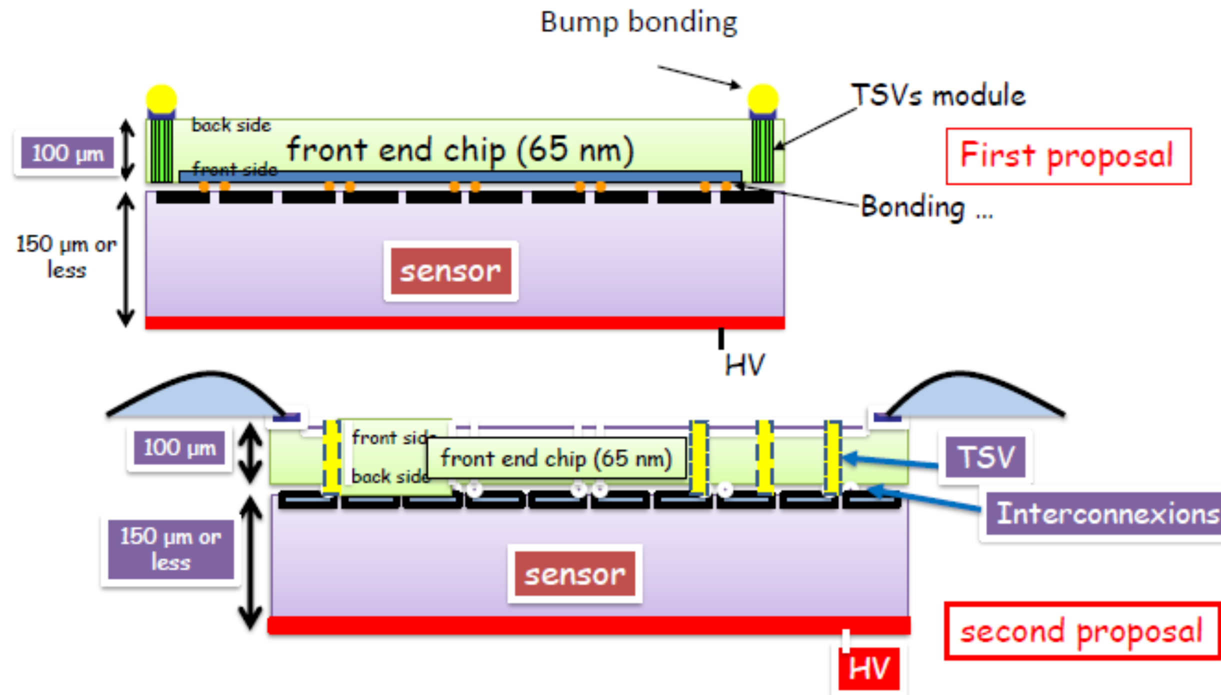


Proposal for the 3D face-to-face interconnection of 2 CMOS layers (sensor/ analog front-end + digital readout) from the 180nm TowerJazz process with SLID bonding by Fraunhofer IMS in Duisburg (submission: end of 2013)

LAL/LPNHE (A. Lounis)

Combine major technology advances and evaluate potential benefits of 3D interconnections

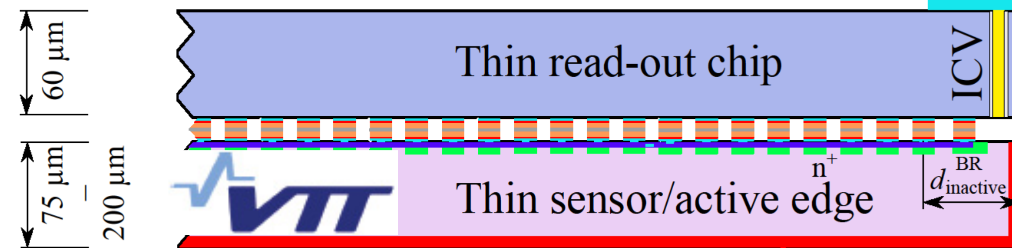
- 130 nm CMOS MPW TezzaronChartered : new version of Readout Chip Omegapix expected May 1st, 2013; afterwards, connection to pixel sensors from CiS and VTT (edgeless) (sensors are tested and functional)
- 65 nm : work in coordination with CERN, goal to design a new pixel readout chip
- Collaborative work with « open » TSV providers in Europe to demonstrate TSVs on functional chips (IPDIA, CEA LETI).



MPP/GLA/LAL/LIV/LPNHE (A. Macchiolo)

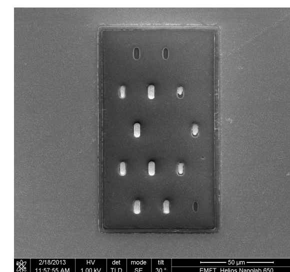
Goal: demonstrator module for SLID and TSV technologies based on ATLAS FE-I4

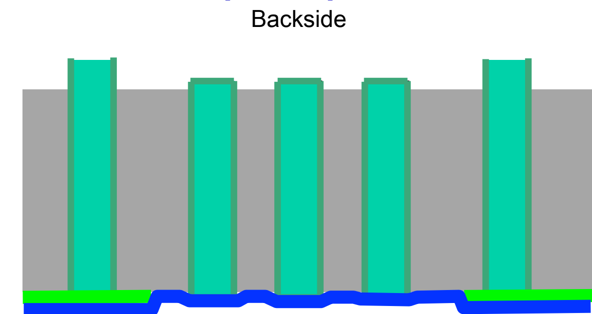
Similar to Bonn project, but more 'aggressive technology
⇒SLID ok for smaller pitch
⇒3µm 1:10 vias



75 µm thick sensors interconnected with SLID to FE-I3 chips, thinned down to 200 µm, at EMFT: interconnection is rad-hard and withstands thermal cycling
Interchip vias (ICV) are almost completed for FE-I3, with very narrow cross-section and high aspect ratio

A different technique is needed on FE-I4 because of different metal stacks and filling structures (etching from the backside).

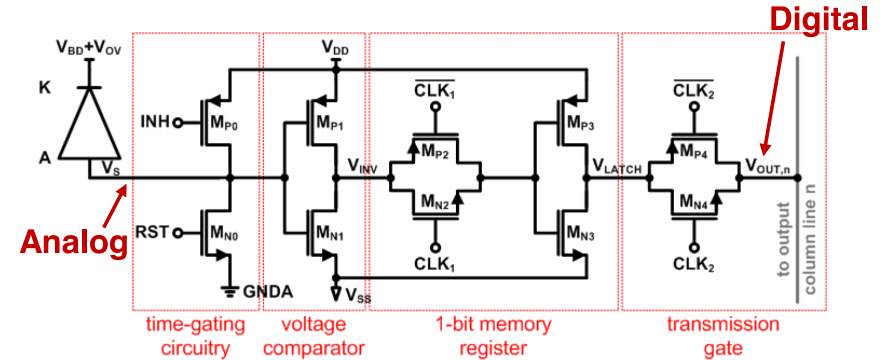




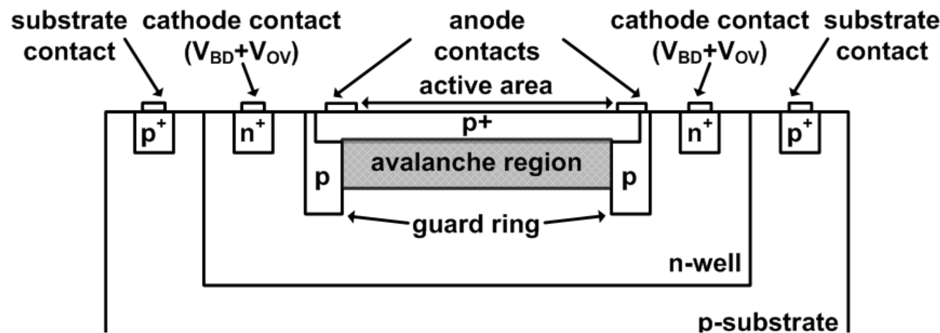
FE-I4B IBL wafers are available for TSV trials at EMFT; plan is to interconnect FE-I4 to VTT/ADVACAM active edge sensors to build a 4-side buttable demonstrator module.

Univ. Barcelona (E. Vilella)

- Tracking sensor based on Geiger APD in 3D-IC CMOS (incl. readout)
- Use 2 tier 3D to increase fill factor (up to 92%) and cure the dark count problem by time-gated operation
- Design ready, waiting for CMP/MOSIS MPW run with Tezzaron



- The GAPD is activated before the BX
- It is deactivated during the interBXs
- The GAPD's ground GNDA allows to use low V_{OV} and further reduce the noise
- The array is read row by row during the interBXs



- T1 → electronics; T2 → sensors

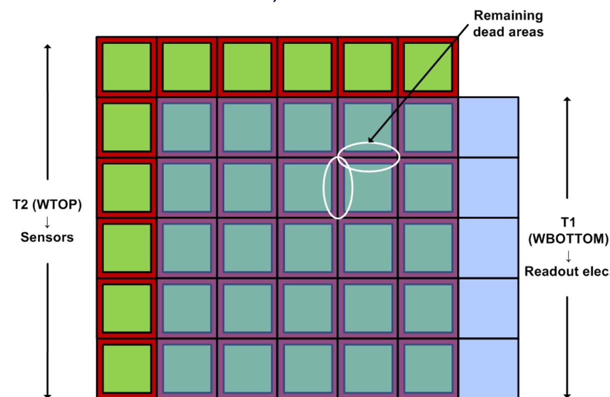
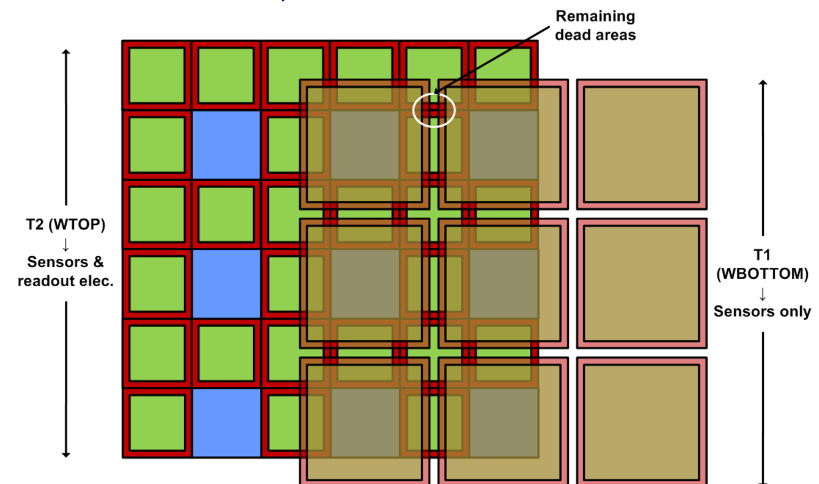


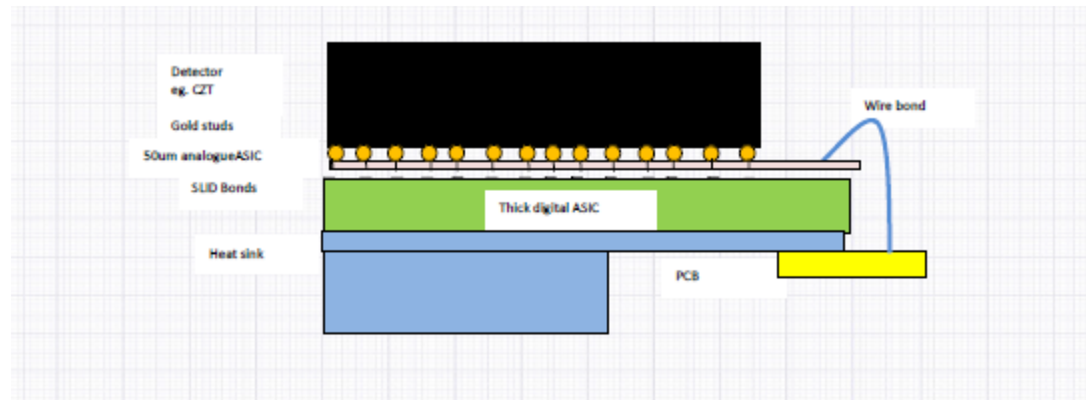
Figure legend:
GAPD active area
Readout electronics of 1 GAPD
GAPD non-active area (guard ring & poly)

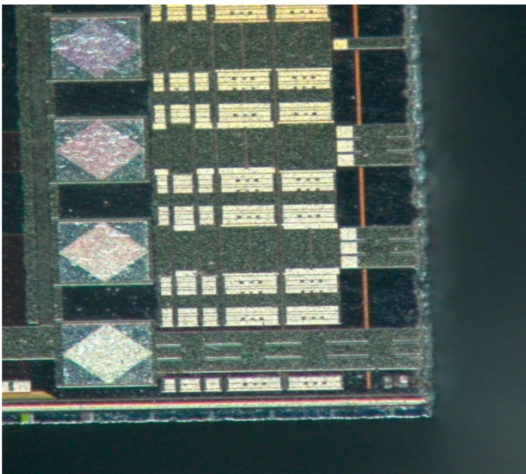
- T1 → sensors; T2 → sensors & electronics

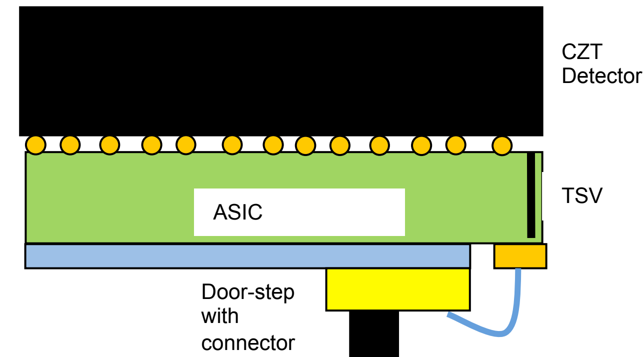


RAL/Uppsala

2 tier readout chip for CZT X-ray detector using EMFT SLID interconnection & TSVs
ASICs exist & tested







Next ASIC will reduce all the readout circuitry.

Geometry for 4-side butting and no dead region

From P. Seller's slides, June 2012

Plan:
Small readout area ASIC designed for submission Nov 2012
Probe test ASIC March 2013
TSV redistribution and test with back side wire bonding June 2013

WP3.3: Shareable IP blocks for HEP

Goal : provide IP blocks for analog and digital needs in HEP with full documentation and laboratory tests.

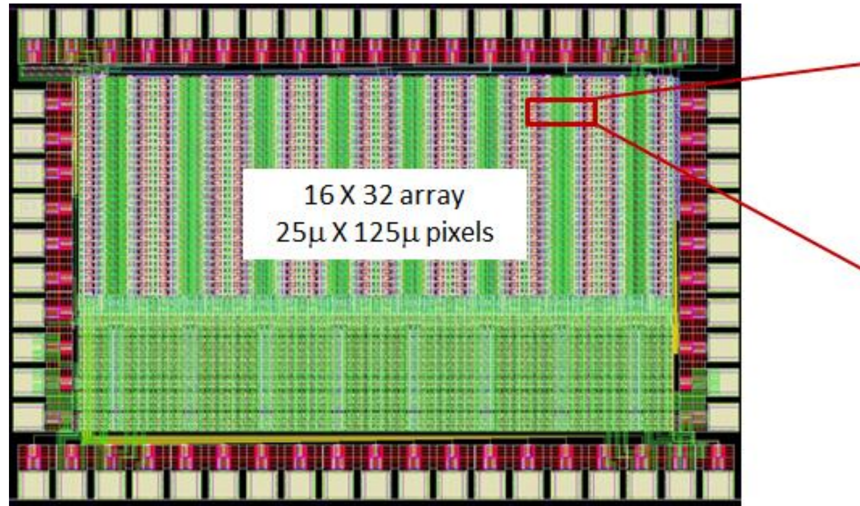
1st set organized by CERN in 65nm. Lot of interest by the community, some work has already started, triggered by the needs of new pixel systems

A 2nd set will be organized by OMEGA for needs in calorimetry, TPC,... (OMEGA/LAL → OMEGA/IN2P3)

65 nm contract status at CERN

- The CERN Finance Committee has approved in the session of March 20 the proposal for negotiating a detailed contract with IMEC for accessing a 65nm from TSMC, with a model essentially very similar to the one we had for accessing the old 130nm technology.
- **Commercial contract**
  3-4 months might be necessary for the CERN Finance Department to iron out all details of the commercial (multi-million) contract
- **Collaborative model**
  TSMC have agreed to allow us to work in a scheme similar to the old one, where essentially there was free exchange of information between users in the HEP community. Still, this requires that a special NDA be distributed by IMEC to interested Institutes.
- **Design Kit**
  CERN would like to distribute to the community a unique 65nm design kit tailored to the majority of the typical projects in the community and provide from the start a unique design flow (for both analog and digital chips), and a qualified library and methodology. We expect that the new kit will be ready for distribution by the time that the commercial contract will be ready.

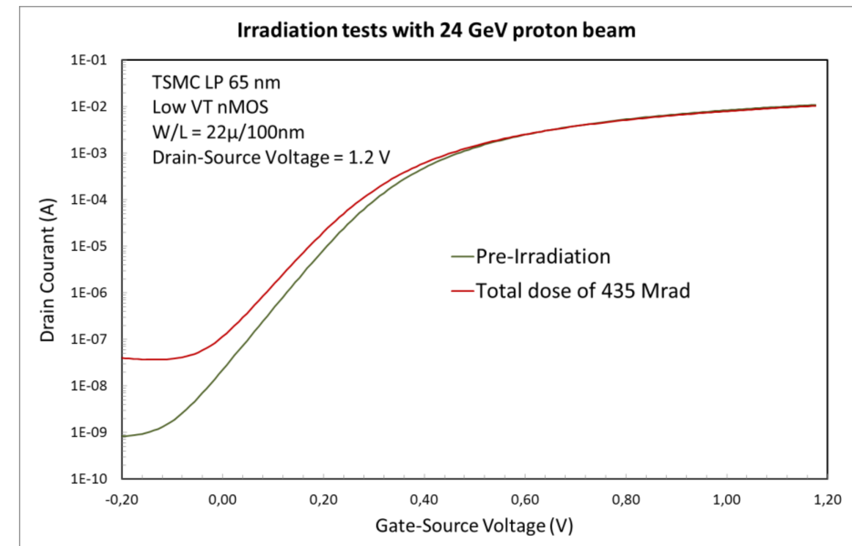
65nm work at CPPM (D. Fougeron)



Small array of 16x32 pixels designed at Berkeley, using 65 nm CMOS process.

- **Pixel area : 25 µm x 125 µm**

Irradiation tests at extreme total ionizing dose (target: 1 Grad) with 24 GeV proton beam: some degradation at very high doses, more work on technology characterization is needed



Design of IP blocks: SEU-tolerant latches, monitoring ADC, bandgap reference, temperature sensor: first submission in June or September this year

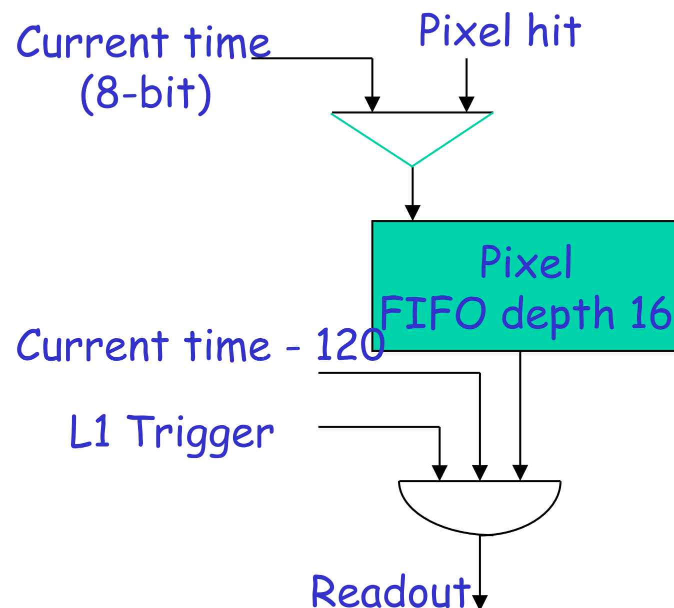
65nm work at AGH-Krakow (M. Idzik)

- At the beginning of AIDA we proposed to develop some blocks in IBM 130 nm
  - Fast (>40 MSps) SAR ADC (6 or 10 bits)
  - Variable frequency PLL
  - SLVS interface
- All these blocks were designed in IBM 130 nm and 1st prototypes were produced
- Tests are ongoing...
- We hope to move one/two blocks to 65 nm
  - 10-bit SAR ADC: first results show its functionality, the effective resolution seems to be less than simulated - quantitative measurements are still progoress
  - PLL tests are just starting
  - SLVS interface works well at least up to 700 MHz

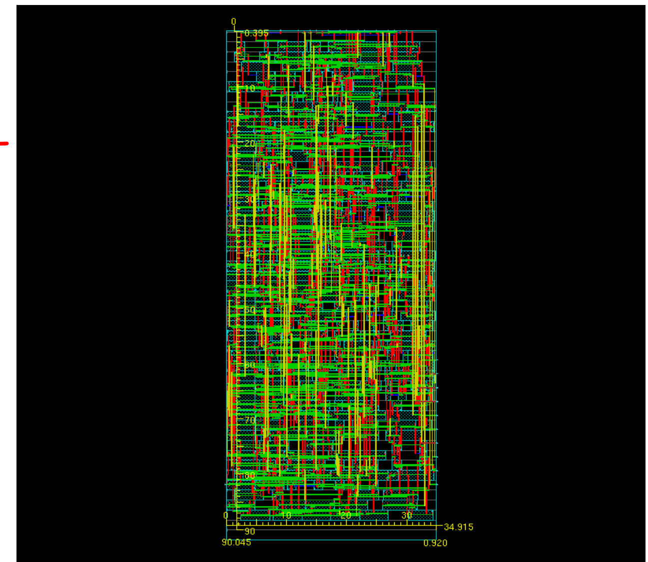
65nm work at LAL/LAPP(J.-F. Genat)

LAL -> Pixel (LAL/LPNHE)
-> OTA (Analog low noise Front-end)
-> PLLs

LAPP -> LAL Omegapix
-> DAC 12b 80 MHz -> 14b
-> Clusters centroid evaluation



Pixel readout architecture based on an in-pixel FIFO storage

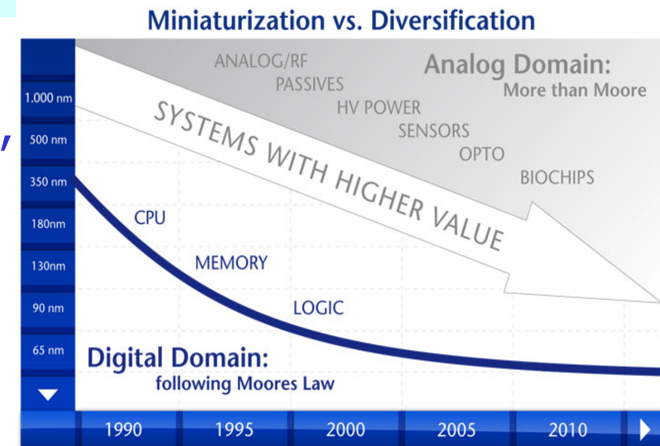


- *Selective readout scheme: Save silicon area and power at the pixel level*

SiGe IP blocks (G. Martin-Chassard)

- Electronics needs in calorimeters and TPCs :
  - large dynamic range, high speed , low noise, low offset, need of precise capacitors and resistors, …
- Blocks :

  ADC, TDC, DAC, Bandgap, OTA, Rad-tol memory, SEU resistant flipflop …

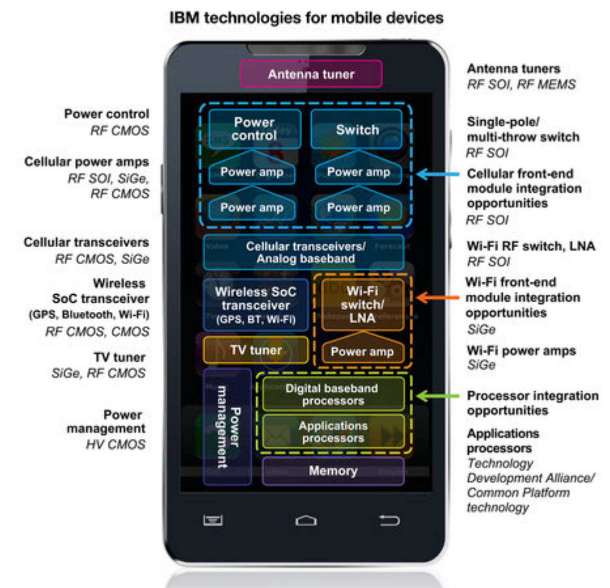


Technology choice ongoing, based upon an estimation technology availability in the future (market needs):

–SiGe or CMOS SOI, HV ….

–130 nm or 180 nm

–IBM, ST micro, AMS …



Milestones and deliverables for this 2nd set of IPs:

- blocks (SiGe) due for month 44 (September 2014)
- Characterization of these blocks before month 48 (January 2015)

Milestones

Schedule of relevant Milestones

Milestone number [59]	Milestone name	Lead beneficiary number	Delivery date from Annex I [60]	Comments
MS18	Availability of wafers with ASIC	18	17	Layout of ASICs in MPW (Task 3.2)
MS19	Submission of dedicated sensors for 3D interconnection	11	17	Layout of sensors (Task 3.2)
MS20	Qualification of ASIC and sensors for 3D interconnection	18	25	Laboratory tests (Task 3.2)
MS21	Validation of first set of IP blocks	1	26	Laboratory tests and full documentation of functional blocks (Task 3.3)
MS22	3D interconnection processing accomplished	18	36	3D integrated devices available for technology assessment (Task 3.2)
MS23	Enable access to 3D interconnection technology	12	48	Laboratory tests for validation of 3D integration processes (Task 3.2)
MS24	Validation of second set of IP blocks	8	48	Laboratory tests and full documentation of

Deliverables

List of deliverables

Delive-rable Number [61]	Deliverable Title	Lead benefi-ciary number	Estimated indicative person-months	Nature [62]	Dissemi-nation level [63]	Delivery date [64]
D3.1	Organisation of the 3D production	18	20.00	R	PU	12
D3.2	Availability of wafers of ASIC electronics	18	30.00	R	PP	17
D3.3	Production of dedicated sensors	11	25.00	R	PP	17
D3.4	1st set of macro blocks	1	22.00	R	PU	22
D3.5	Wafer post processing (thinning, TSV)	12	24.00	D	PP	25
D3.6	Component processing	18	12.00	R	PU	29
D3.7	Test interconnection and evaluation	12	24.00	R	PP	36
D3.8	Detectors in 3D available for assessment	18	24.00	D	PP	40
D3.9	2nd set of macro blocks	8	22.00	R	PU	44
D3.10	Assessment of 3D integrated sensors	11	20.00	R	PU	48

Milestones and Deliverables in 2013

Milestones:

1) MS20 Qualification of ASICs and Sensors for 3D interconnection — M25 (Feb 2013)

2) MS21 Validation of first set of IP blocks — M26 (Mar 2013)
postponed till 65nm MPW available by CERN

Deliverables:

1) D3.4 First set of macro blocks — M22 (Nov 2012)
postponed till 65nm MPW available by CERN

2) D3.5 Wafer post processing (thinning, TSV) — M25 (Feb 2013)

3) D3.6 Component processing — M29 (Jun 2013)

Conclusions

- The WP3.2 subprojects are exploring various flavors of 3D integration; the progress is largely depending on the different level of maturity of the 3D processes ("via last" vs. "via middle", high vs. low interconnection density, etc.)
- Some subprojects (e.g. CERN/MEDIPIX) are already very close to their goal of implementing 3D pixel demonstrator modules
- This task appears to be on the right track to achieve Deliverables and Milestones according to the schedule
- For WP3.3, we have some delay with respect to the original plan for 65nm CMOS, but we will quickly recover as soon as the contract negotiation phase is concluded (about 3 more months). We thank CERN for the great work they are doing to allow the community to access a technology that is strongly needed for future advanced pixel systems!

Backup slides