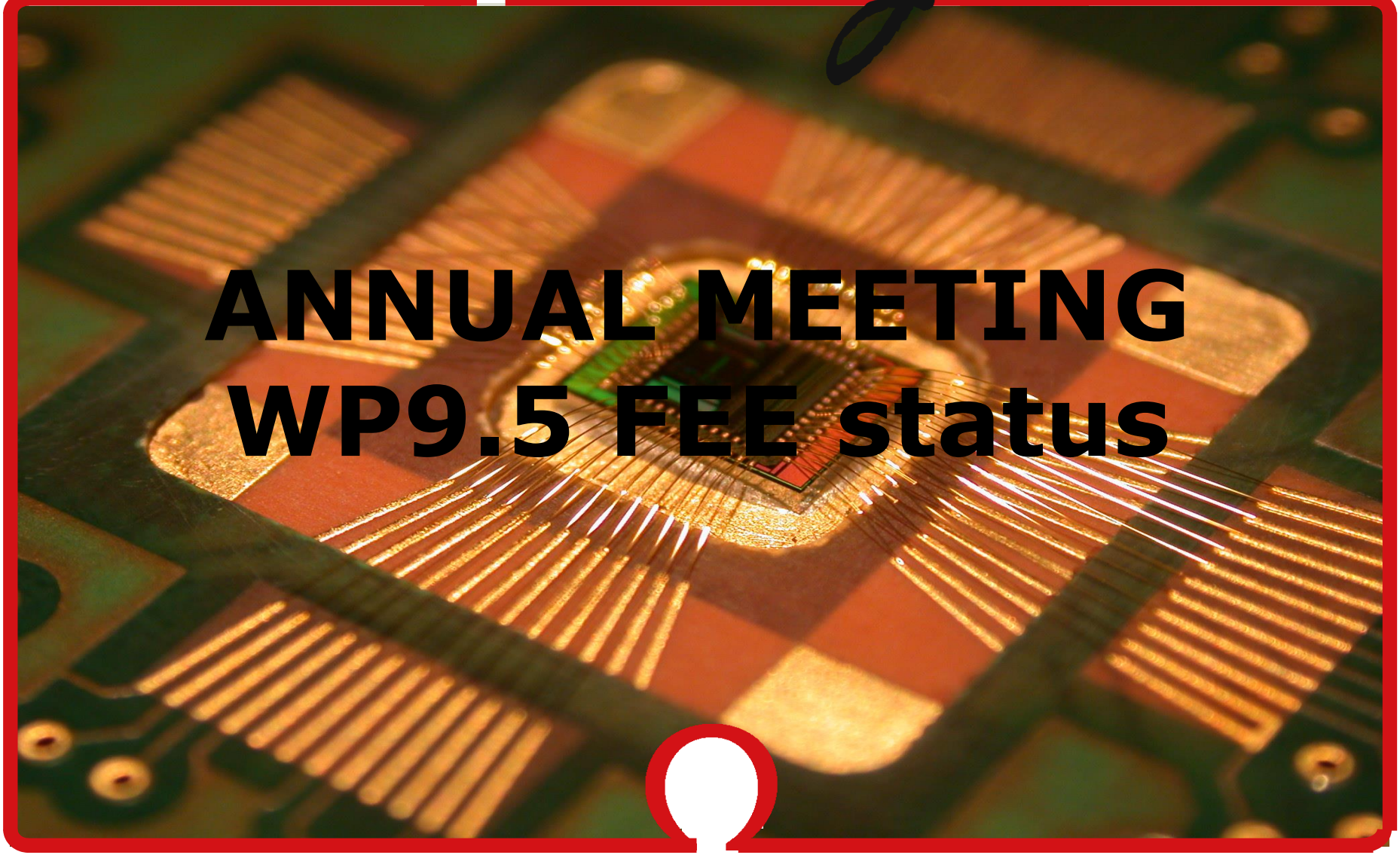


ANNUAL MEETING
WP9.5 FEE status

AIDA WP9.5: MILESTONES and SCHEDULE

- **Schedule presented at the AIDA Kick Off meeting**

  2011: Characterization of the 2nd generation ROC Chips

  - Dedicated run produced in **March 2010**
    - 25 wafers received in June
    - 20 000 chips packaged in the US

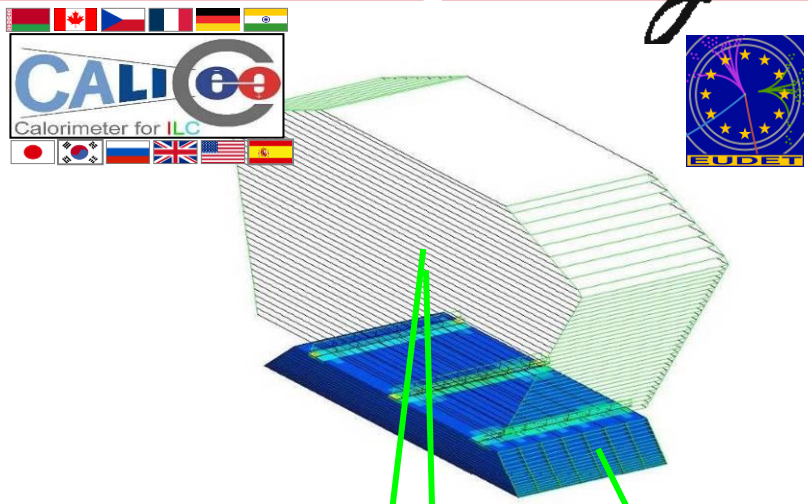
  ~~2012~~ Feb 2013: Submission and test of one of the 3rd generation chips

  ~~2013~~ 2014 ?: Submission of a second 3rd generation chip

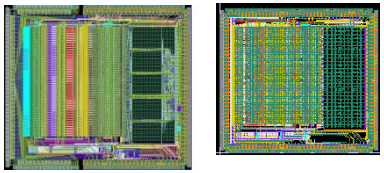
  August 2013: Report

- Budget for 3rd generation of electronics:
  - 31k€ (ECAL) + 50 k€ (Hadronic Calorimeter) => 2 chip submissions
  - 30 ppm

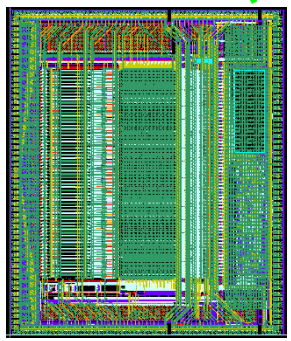
- Cost:
  - Multi Project runs (MPW): 1k€/mm2
  - Packaging: $3500
  - Testboard: 1500 €



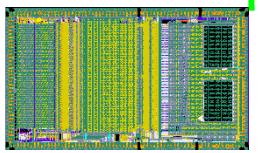
HARDROC2/MICROROC
SDHCAL RPC/µMEGAS
64 ch 20 mm2/



SKIROC2
ECAL Si
64 ch. 65 mm²



SPIROC2
AHCAL SiPM
36 ch 32 mm²

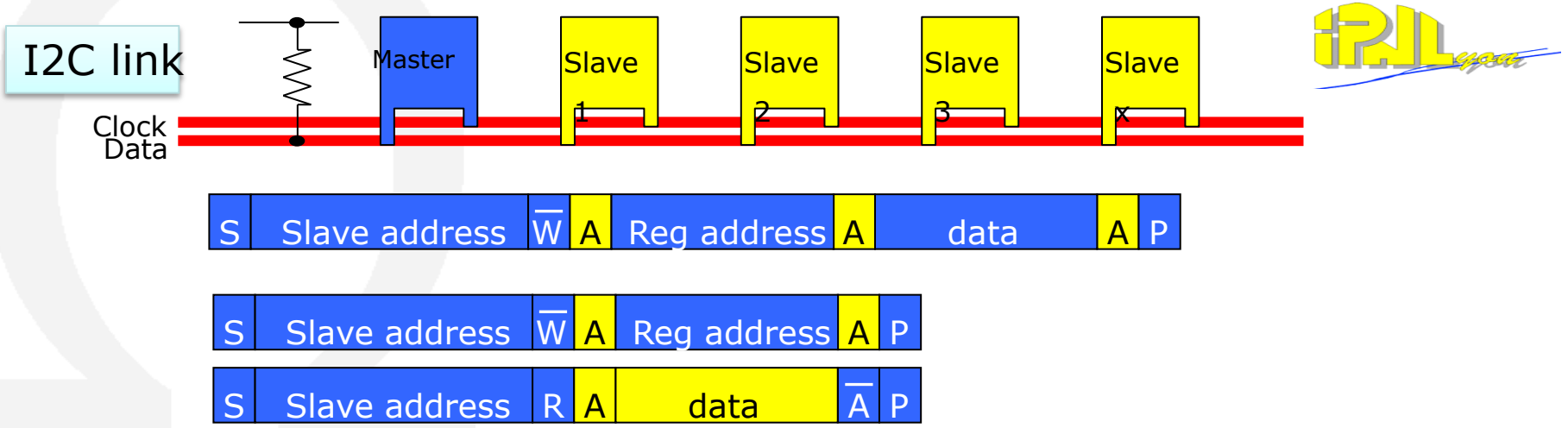


0.35µm SiGe AMS technology

AIDA WP9.5: 3rd generation of ROC cl

- 2nd generation ROC chip
  - Auto-trigger, analog storage, digitization and token-ring readout, common DAQ
  - Power pulsing : <1 % duty cycle
- 3rd generation ROC chip
  - **Independent channels (= Zero suppress)**
    - 64/36 address pointers
    - ReadOut, BCID, SCA (Spiroc and Skiroc) management

    => Digital part much more complicated
    - SCA depth: 8 instead of 16
    - Possibility to use "Roll mode" by Slow Control: circular memory very useful for Testbeam
    - New TDC with no dead time
    - **New Slow Control** (Triple voting) using **I2C link** (while keeping the « old SC » system)



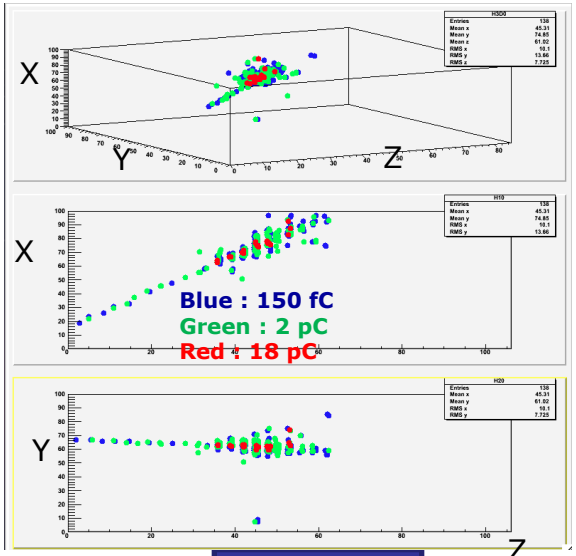
HARDROC2

- **64 channels (RPC SDHCAL)**
  - preamp + shaper+ 3 discris (semi digital readout)
  - Auto trigger on 10fC up to 20 pC
  - 5 0.5 Kbytes memories to store 127 events
  - Full power pulsing => 7.5 µW/ch
  - 2010 TB : 1 m2 (144 HR2b)
    - power pulsing in magnetic field successfully tested
  - SDHCAL technological proto with 40 layers (5760 HR2 chips) built in 2010-2011.
    - Testbeam summer 2011: pb with the DAQ2 (HDMI) + pb of cooling
    - TB November 2011: 6 detectors and USB DAQ: good performance of the electronics and detector
    - TBs 2012 with 40 detectors and intermediate DAQ (HDMI & DCC cards for synchronization and USB for config & readout)

    Very good TB results with a complete system, autotrigger mode, power pulsing

    See Vincent's Talk
  - HARDROC3 FE: No major modifications needed

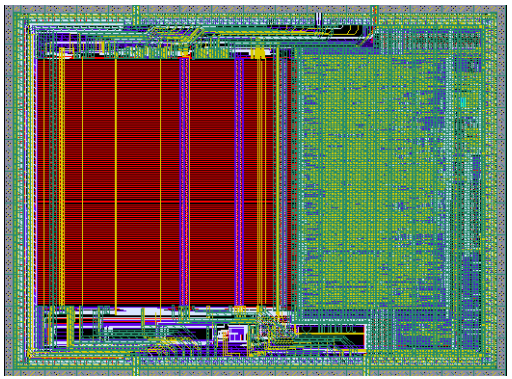
Cosmic hadronic shower



@IPNL

HARDROC3

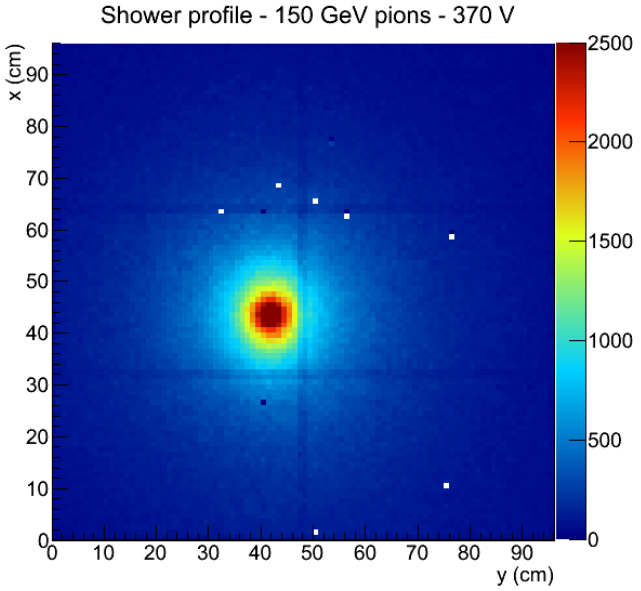
- No major modifications needed in the FE
  - submitted at the end of Feb 2013 (SiGe 0.35µm), expected in June 2013
  - Die size ~30 mm2 (6.3 x 4.7 mm2)
  - To be packaged in a TQFP208
  - **64 independent channels**
  - **I2C link (@IPNL)**
  - PLL: integrated before in a builiding block, first measurements are very good
    - Input frequency 2.5 MHz =>output frequency: 10, 20, 40, and 80 MHz available
  - Bandgap: new one with a better temperature sensitivity, tested in a building block
  - Temperature sensor: tested in a building block, slope – 6mV/°C
  - **2013: dedicated to the test of HR3 before submitting other chips**



- **64 channels for µMegas (DHCAL)**
  - Very similar to HARDROC except for the input preamp and shapers (100-150 ns)
  - Noise: 0.2fC (Cd=80 pF). Auto trigger on 1fC up to 500fC
  - Pulsed power: **10 µW/ch** (0.5 % duty cycle)
  - 4 Micromegas prototypes of 1x1 m2 were constructed in 2011-2012 and tested in particle beams inside the DHCAL steel structure in 2012
  - **Very good performance of the electronics and detector (Threshold set to 1fC)**

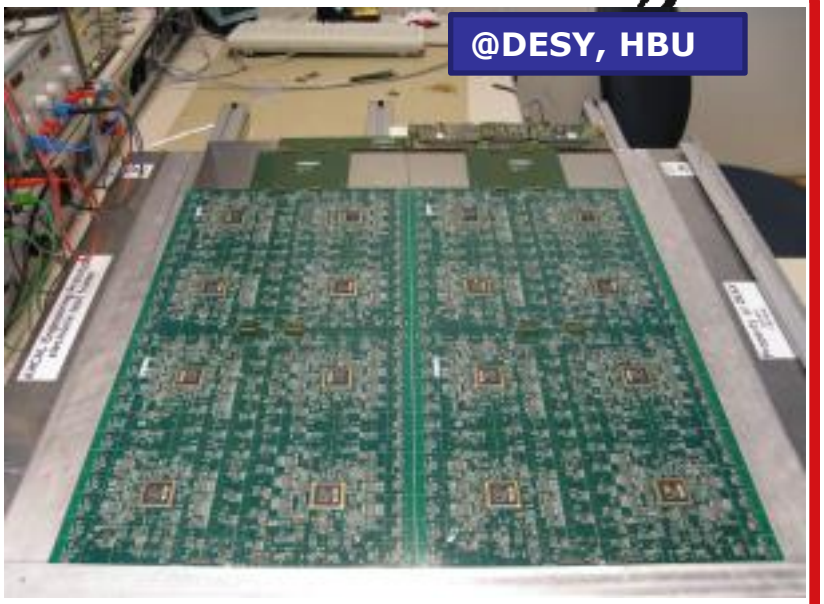
See Vincent's Talk

@LAPP



SPIROC2

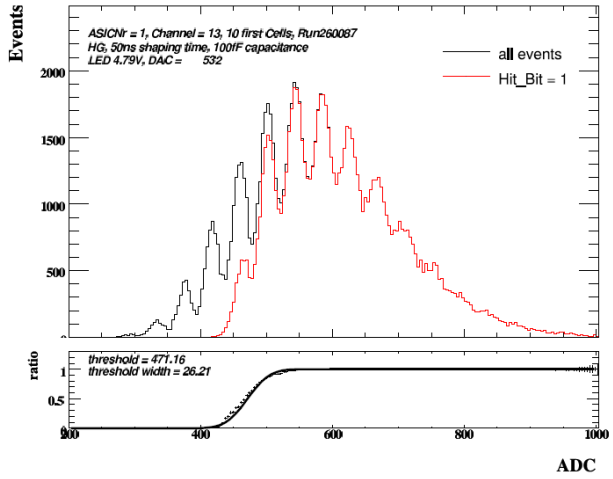
- **36 channels for AHCAL (SiPM)**
  - Autotrigger on 1 spe (150 fC), 16 depth SCA for charge measurements (up to 300 pC) and time measurement (< 1 ns)
  - 2 memories of 2K bytes to store charge and time measurements from the internal 12 bits ADC
  - Pulsed power: **25 µW/ch** (1 % duty cycle)

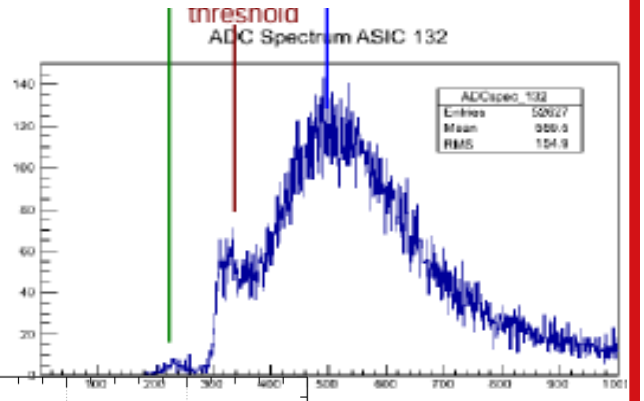


  - Testbench measurements at ORSAY and at system level at DESY in 2011 showed some fine effects in spiroc2b to be corrected
    - ✓ Building block with a new FE for spiroc tested in December 2011: new input preamp to solve rate dependency pb + coherent noise + Crosstalk (HG/LG)
    - ✓ Very good analog performance
      - ✓ HG Preamplifier + Slow shaper: Vmax= 46 mV/pe, Noise RMS = 2,3mV =>SNR ~ 20
    - ⇒ Submission of SPIROC2C (Feb 2012) with this analog FE and the digital part of spiroc2b but higher sensitiivity to digital coupling through the substrate
    - ✓ **Klaus2 chip** (Heidelberg University): also a good candidate for the FE of Spiroc => "KlausROC "

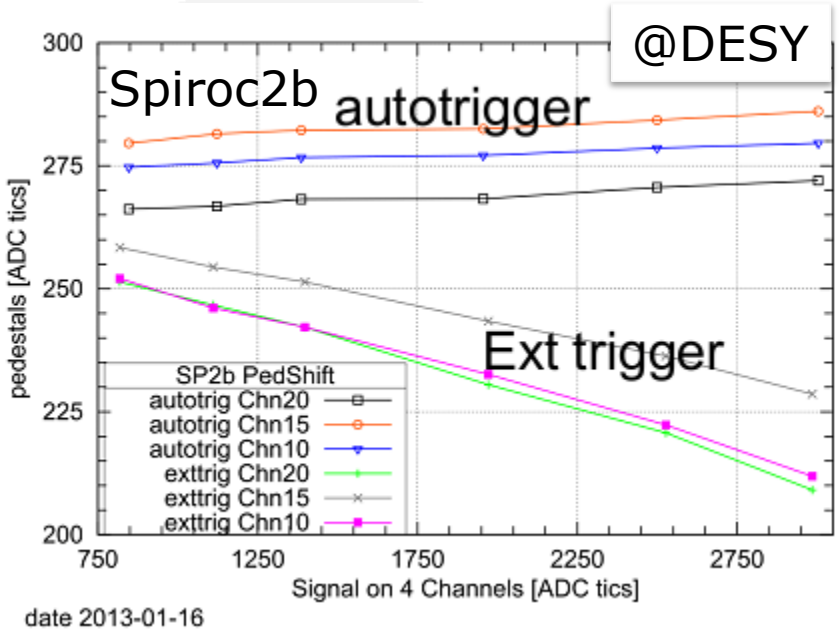
TEST BEAMs with SPIROC2b

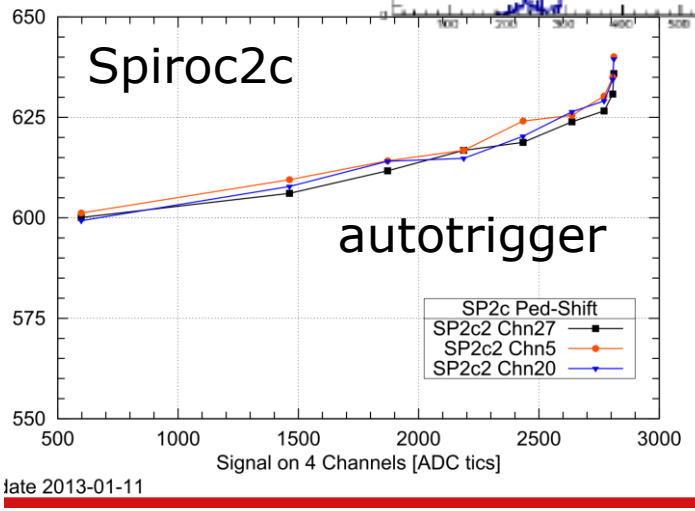
- 576 channel AHCAL layer prototype **successfully tested at CERN and at DESY** in 2012 *See Katja's Talk*
- TDC: First tests of TDC ramps in SPIROC2b show promising results
  - Many corrections needed: memory cell and channel wise offsets correction, chip wise ramp corrections
  - Electronics resolution ~2 ns
- Many measurements on testbench with 2b (referred to vdd) and 2c (referred to gnd)
  - **Pedestal shift when large pulses** (> 1000 pe-) are sent in one channel





Plots: Katja Krüger





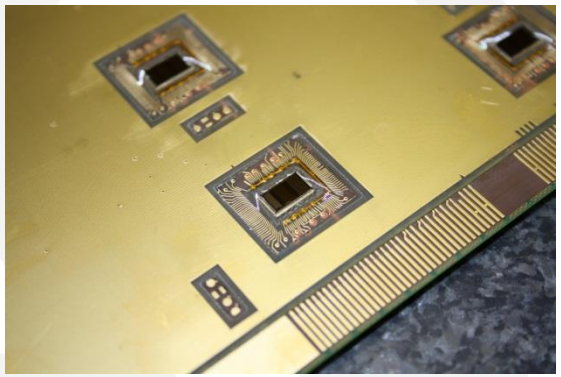
SKIROC2

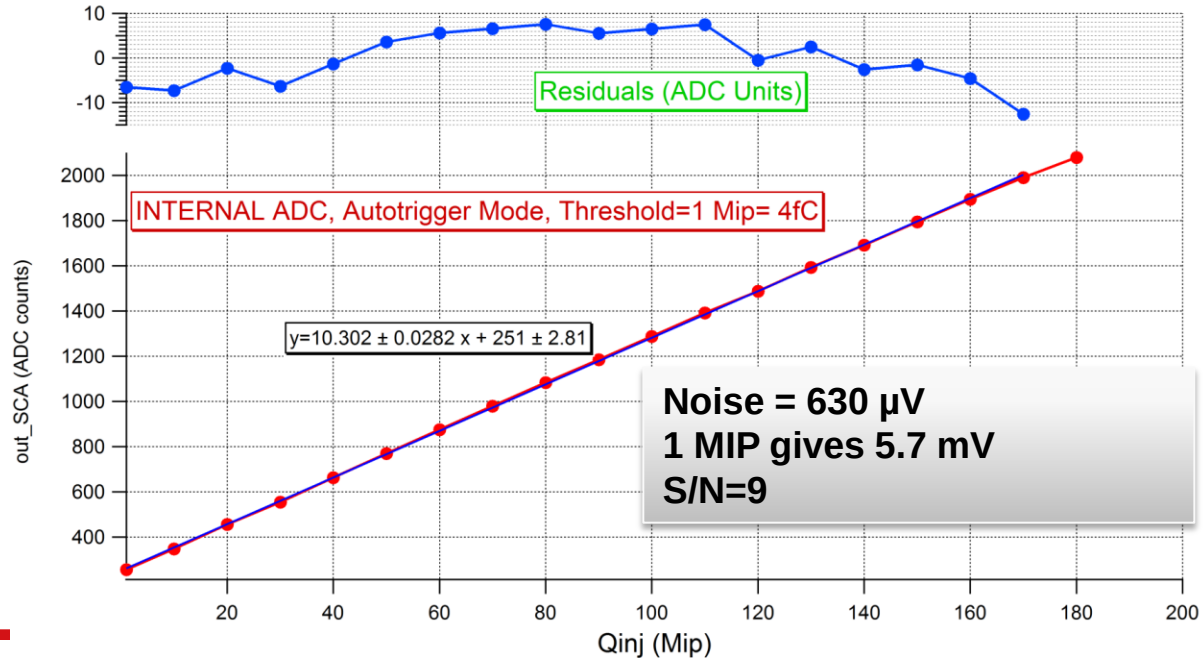
- 64 channels for ECAL (Si pin diodes)
  - ❑ Autotrigger on 0.5 MIP (2 fC), 15 depth SCA for Charge measurement (0-2500 MIPs) and Time measurement (< 1 ns)
  - ❑ 1 memory of 4K bytes to store the digitized measurements of Charge and Time by the internal 12 bits ADC
  - ❑ Pulsed power: **25 µW/ch** (1 % duty cycle)

❑ **FEV boards**

❑ Testbench measurements: very good performance, much more difficult on FEVs!

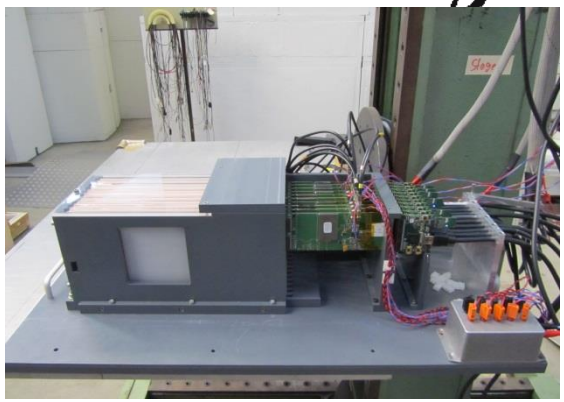
FEV board



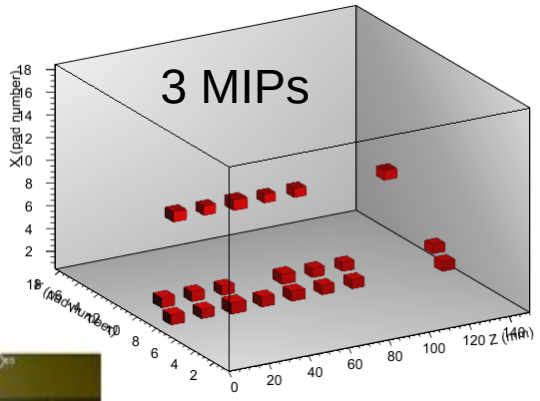


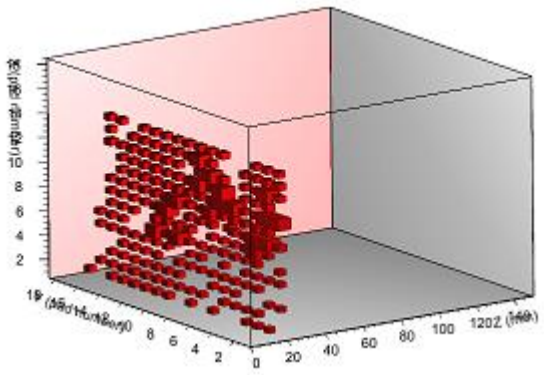
TESTBEAMs with SKIROC2

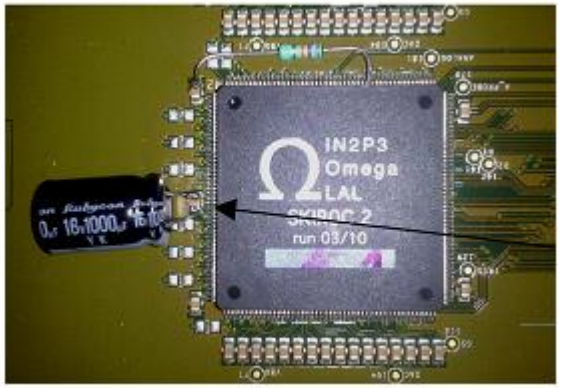
- Successful test beams @ DESY in 2012 (1 to 6 layers) and 2013 (10 layers), power pulsing mode, autotrigger mode, e- (1 to 5GeV)
  - 4 packaged skiroc2/slab *See Roman's talk*
  - Nice event displays



- **BUT**
  - BCID+1: "retriggering" of the ASIC wo hit
    - Understood and easy to correct and to cut offline
  - Plane events
    - Input PA referred to vdd (= Spiroc) and power supply common to the 4 ASICs
    - Depend of the number of ASIC with hits and of the number of channels that triggered
    - Number of plane events reduced from 80% down to 10% using decoupling capacitors and separating vdda and vddd_delay

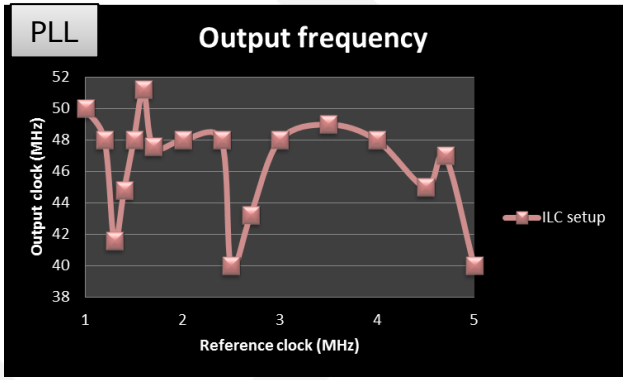


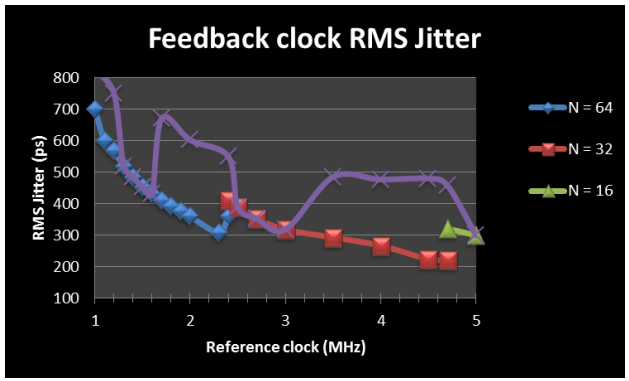




Building blocks (integrated in HR3): results

- In parallel, small building blocks were designed and submitted in 2012
- **Bandgap** (5 chips):
  - Temperature sensitivity: ~70 µV/°C (was 250 µV/°C with the previous BG)
  - Non uniformity between chips depends on the uniformity of the reference voltages which are referred to a 2.5V generated by a bandgap: Vbg Uniformity (30°C): < 14 mV (was 20 mV in hardroc2)
- **Temperature sensor:** -6mV/°C
- **PLL**: to generate clocks internally. First measurements are very good
  - Input frequency 2.5 MHz =>output frequency: 10, 20, 40, and 80 MHz available





SUMMARY

- **Nice TB results obtained with all the ROC chips, in AUTOTRIGGER mode**
  - Complete system, large dynamic range, low noise
  - Tests with power pulsing mode

- **Still some fine effects to be understood with the 2nd generation chips**
  - **SPIROC2**
    - Spiroc2b: Pedestal shift (with large signals and external trigger) under investigation
    - Spiroc2c: Very good analog performance (building block wo the digital part) , sensitivity to digital coupling through substrate.
  - **SKIROC2**
    - Plane events, digital coupling to be understood (FEV design vs chip)

- **End of Feb 2013: submission of HARDROC3**
  - Semi digital readout => « Simple » chip compared to Skiroc and Spiroc: I2C, independent channels, circular memory, one register/channel, temperature sensor
  - package: TQFP208 instead of TQFP 160 for HR2

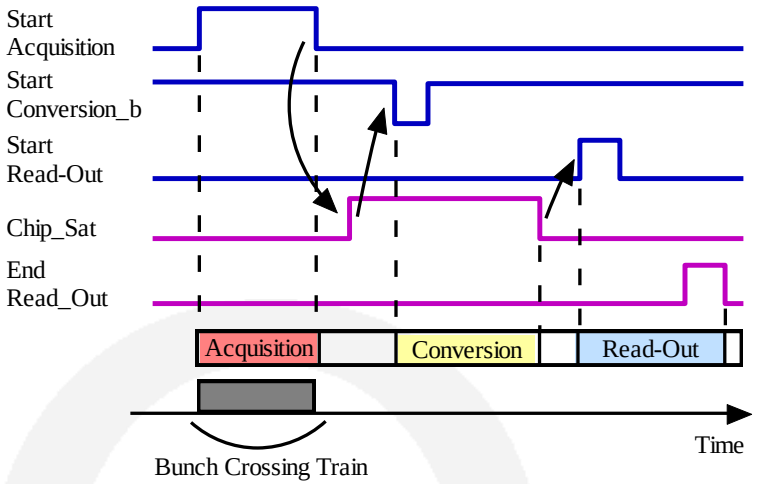
  ⇒ **New 2-3 m RPC chambers to be built to test HR3 at the system level**
  - Die size ~30 mm2 => 30 k€ + 5K test setup (AIDA funding) + 16 ppm/30 ppm used
  - Tests should start at the beginning of June 2013 -> **Report for August 2013**

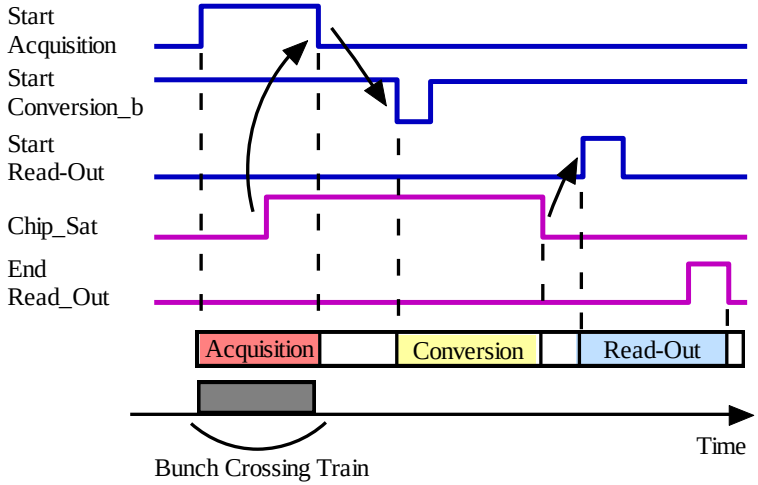
- **SPIROC3 and SKIROC3 : Complex chips**
  - I2C link, independent channels but also new PA, TDC , SCA
  - Hardroc3 test feedback necessary before submitting Spiroc3 and Skiroc3
  - Size should be ~43 mm2 (spiroc3) and 81 mm2 (skiroc3)=> Dedicated run necessary to complete AIDA funding
  - Submission: 2014?

BACK UP Slides

3Gen ROC chips: common features

- DIF sequencing (Acq, Conv and Readout):
  - Backward compatibility with 2Gen ROC chips sequencing
  - Use of ChipSat signal
  - Daisy chained chips for readout

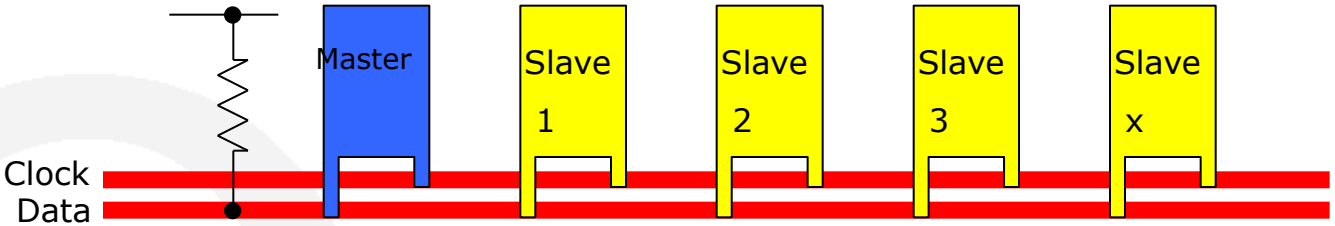




- Possibility to use Roll mode by Slow Control:
  - If RollMode = "0" ➔ Backward compatibility with 2Gen ROC chips behavior
    - Only the N first events are stored
  - If RollMode = "1" ➔ 3Gen ROC chips behaviour
    - Use the circular memory mode
    - Only the N last events are stored

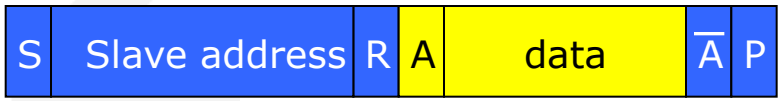
3Gen ROC chips: common features

- Slow control parameters:
  - Backward compatibility with 2Gen ROC chips slow control
    - Use of classical shift register slow control
  - Embedded I2C
    - 7-bit address + 1 general call address (127 chips can be addressed)
    - Access port doubled
    - Bidirectional data line with open collector (Driver will be the same as Dout)
  - Read back capability of SC bits (non destructive)



- Write frame:

- Read frame:



3Gen ROC chips: common features

- Extra pin needed for I2C / SC:

HARDROC 2		HARDROC 3	
ShiftReg_In	1	ShiftReg_In	1
ShiftReg_Out	1	ShiftReg_Out	1
ShiftReg_Clk	1	ShiftReg_Clk	1
ShiftReg_Rst	1	ShiftReg_Rst	1
		ShiftReg_Loadb	1
		ShiftReg_ReadBack	1
		Error_Triple_Voting	1
		7-bit I2C @	7
		2 x (SCL / SDA)	4
		Select_I2C_Port	1
		Clk_I2C_SR	1
		Rstb_I2C	1
		Select_I2C_SR	1
Total	4	Total	4+18

Standard SC

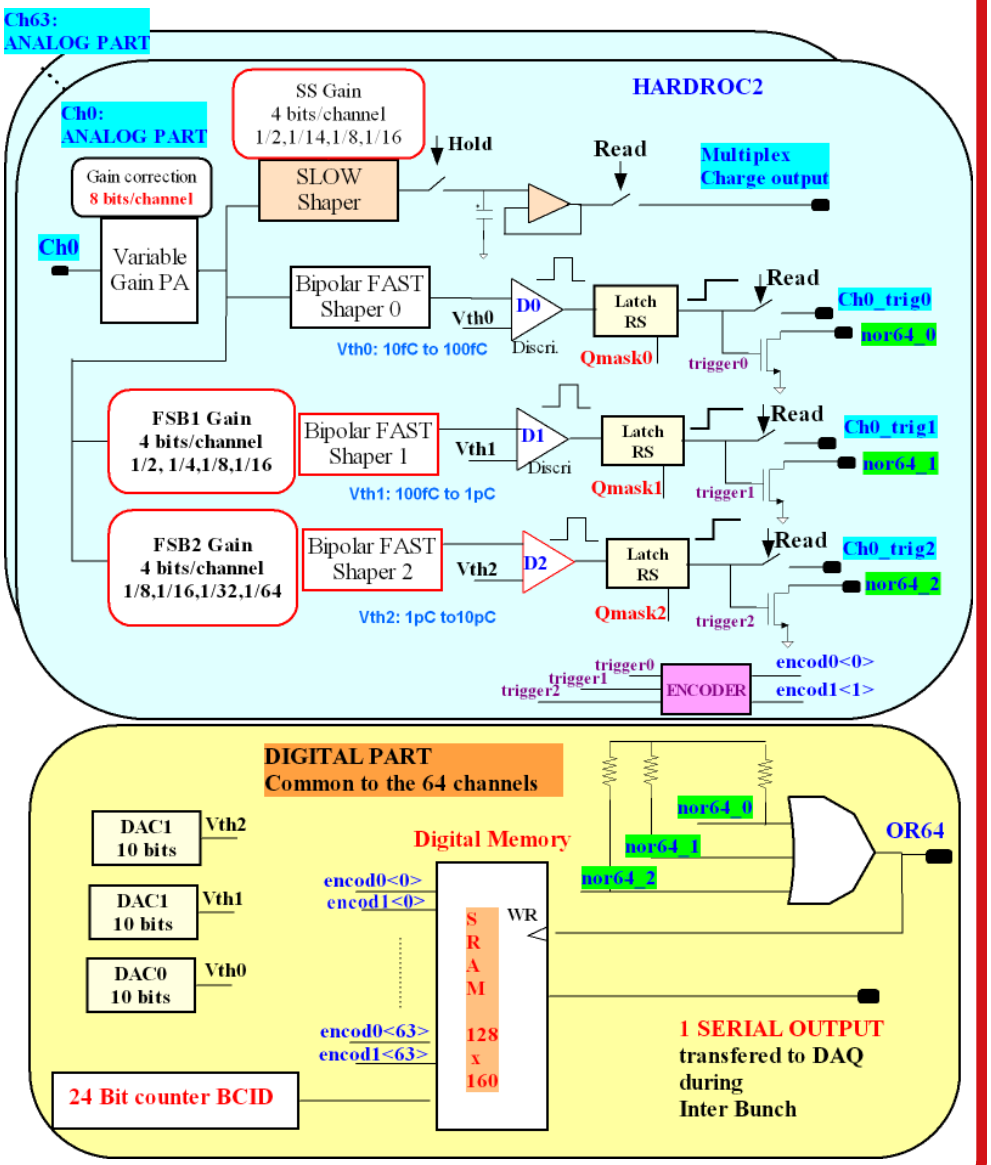
SC with triple voting

I2C

Selection I2C or std SC

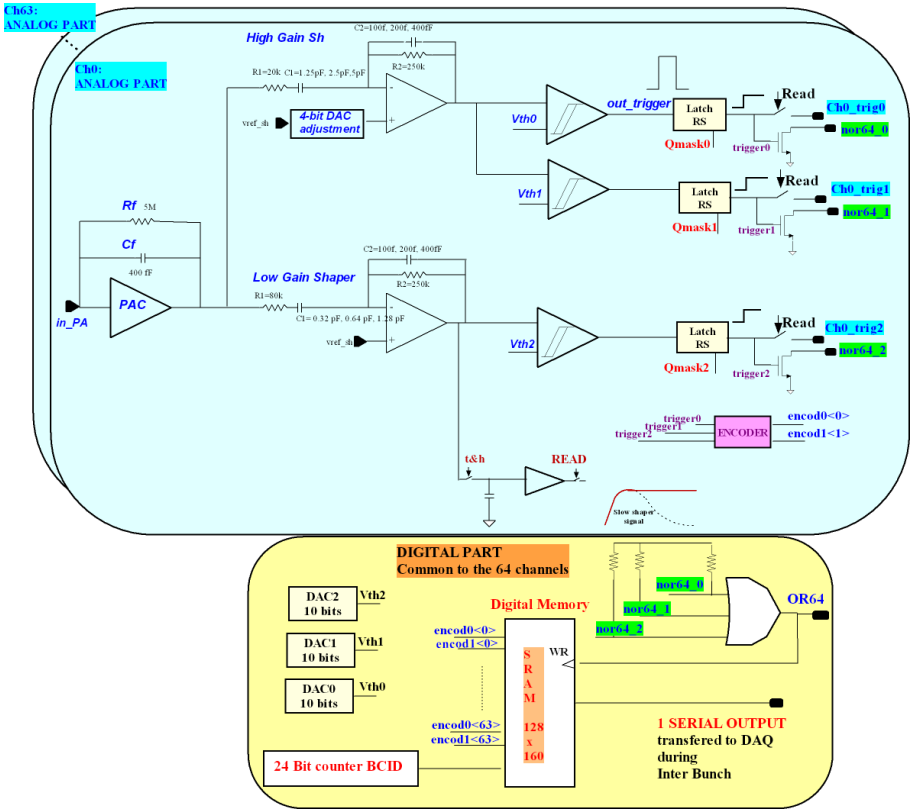
HARDROC2b

- **64 channels, 20 mm2**
- **Variable gain (8bits) current preamps (50 ohm input)**
- One multiplexed analog output (12bit)
- **3 shapers, variable Rf,Cf and gains**
- **3 thresholds** (=> 3 DACs):
  - 10 fC, 100fC, 1pC (megas)
  - 100fC, 1pC, 10pC (GRPC)
- **Auto-trigger on 10fC**
- Store all channels and BCID for every hit. Depth = 128 bits
- Data format : 128(depth)*[2bit*64ch+24bit(BCID)+8bit(Header)] = 20kbits
- **872 SC registers**, default config
- **Power pulsing**



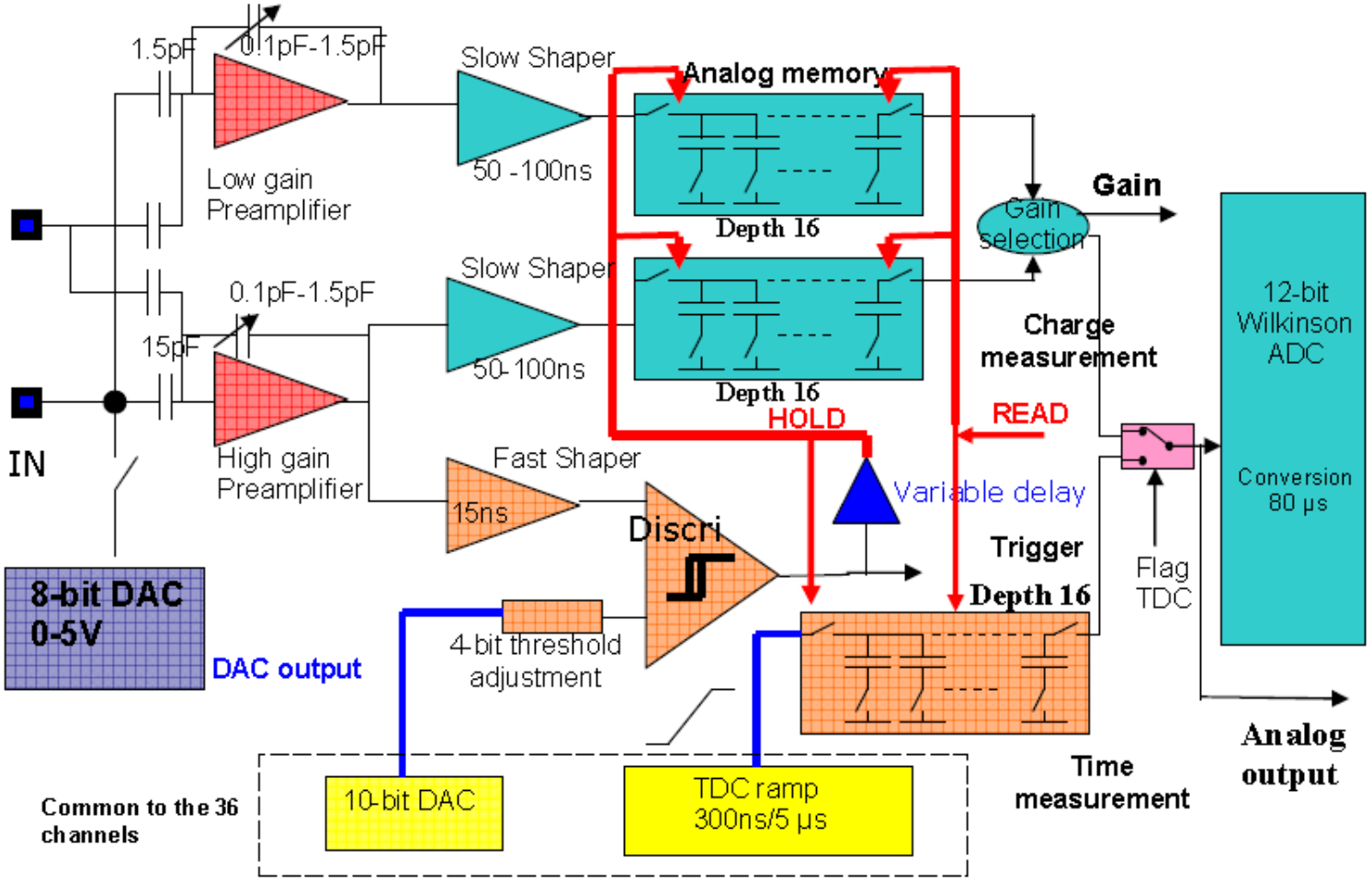
MICROROC ~ HR2B

- Collaboration with LAPP Annecy
- 64 channels, 20 mm2
- Same as HARDROC but with charge preamp input stage + HV protection and slower shaping + 4bit DAC/channel
- Preamp optimized for Cd=80 pF, noise = 0.2 fC. Cf=0.4pF Rf=5M
- Maximum input charge : 500 fC
- Bi-gain shaper (G1-G4), peaking tunable 50-200 ns (2 bits)
- 3 thresholds: Lowest threshold ~2 fC
- Pin to pin compatible with HR2
- Store all channels and BCID for every hit. Depth = 128 bits
- Data format : 128(depth)*[2bit*64ch+24bit(BCID)+8bit(Header)] = 20kbits
- **872 SC registers**, default config
- **Power pulsing**

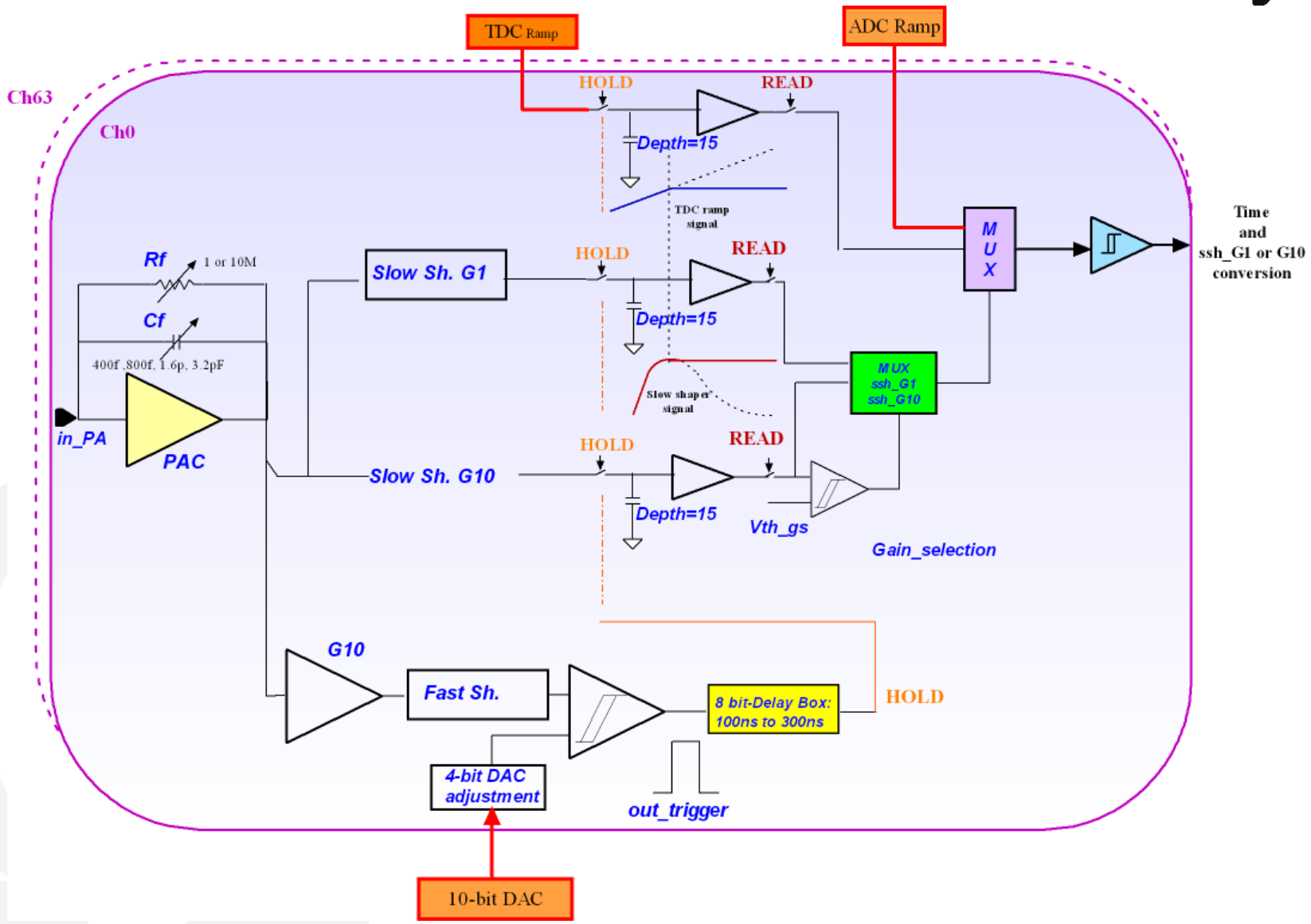


SPIROC2b

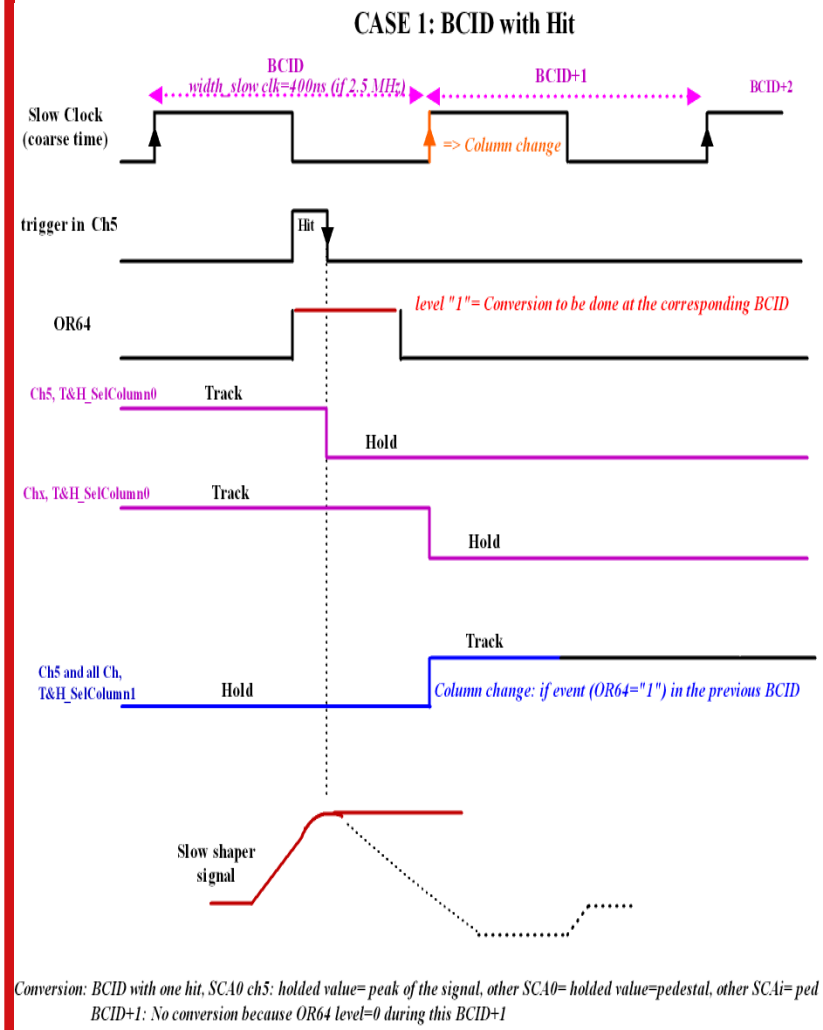
- 36 channels , 32 mm2
- Bi-gain (autogain)
- Analogue Memory depth : up to 16 events can be stored (columns)
- 2 × 36 channels (Charges/Times)



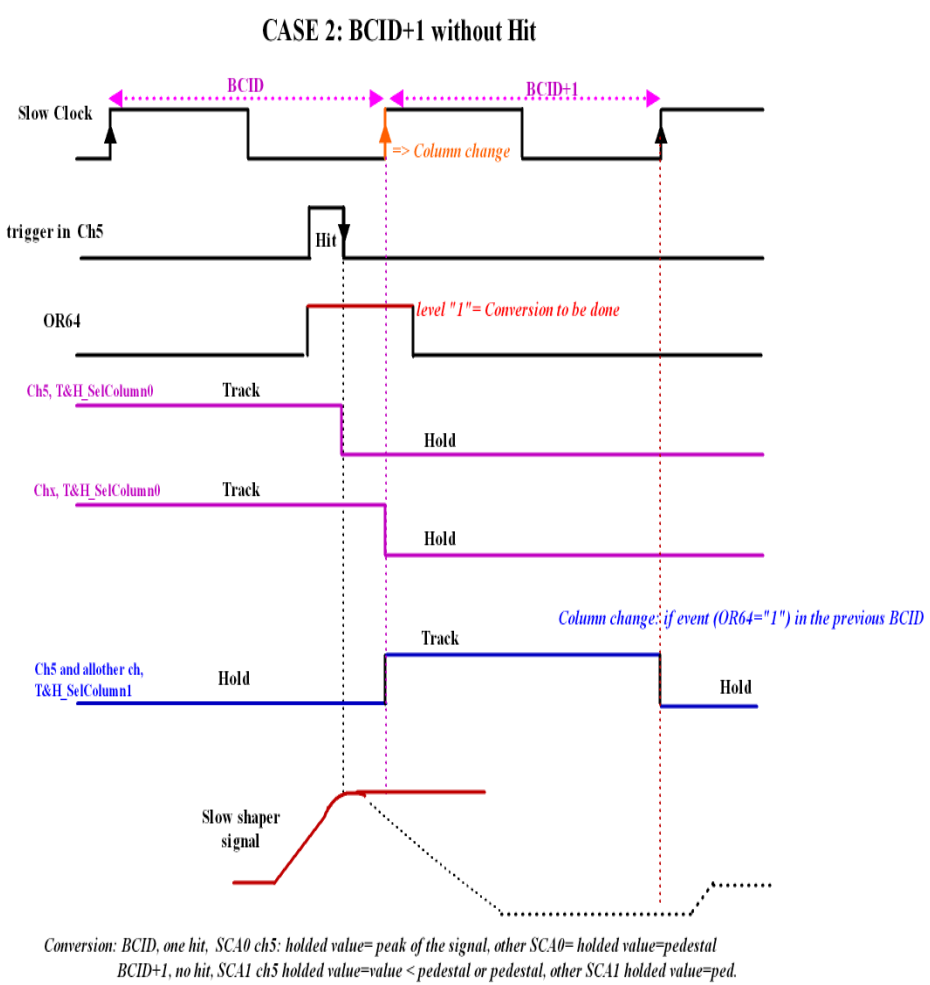
SKIROC2


TDC Ramp
ADC Ramp
Ch63
Ch0
HOLD
READ
Depth=15
TDC ramp signal
Rf
1 or 10M
Cf
400f ,800f, 1.6p, 3.2pF
in_PA
PAC
Slow Sh. G1
HOLD
READ
Depth=15
Slow shaper signal
MUX
ssh_G1
ssh_G10
Slow Sh. G10
HOLD
READ
Depth=15
Vth_gs
Gain_selection
MUX
Time and ssh_G1 or G10 conversion
G10
Fast Sh.
8 bit-Delay Box: 100ns to 300ns
HOLD
4-bit DAC adjustment
out_trigger
10-bit DAC

BCID+1 wo hit in SKIROC2



Conversion: BCID with one hit, SCA0 ch5: holded value= peak of the signal, other SCA0= holded value=pedestal, other SCAi= ped
BCID+1: No conversion because OR64 level=0 during this BCID+1



Conversion: BCID, one hit, SCA0 ch5: holded value= peak of the signal, other SCA0= holded value=pedestal
BCID+1, no hit, SCA1 ch5 holded value=value < pedestal or pedestal, other SCA1 holded value=ped.