AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

FCAL electronics and DAQ

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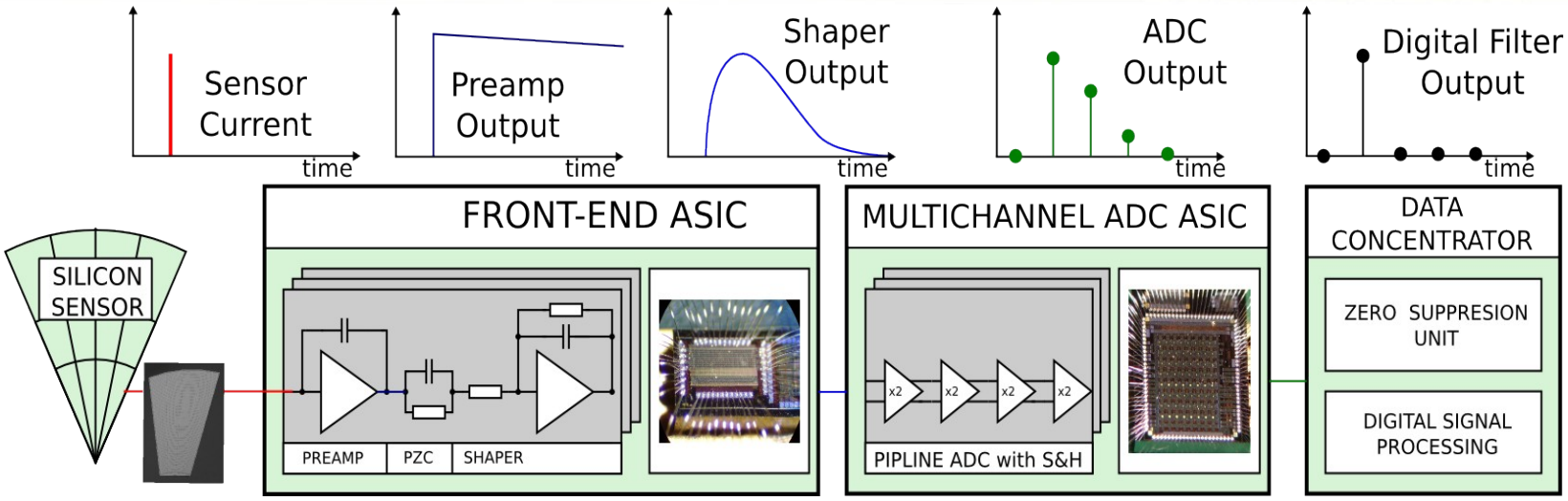
LumiCal detector readout chain



Existing LumiCal detector readout comprises:

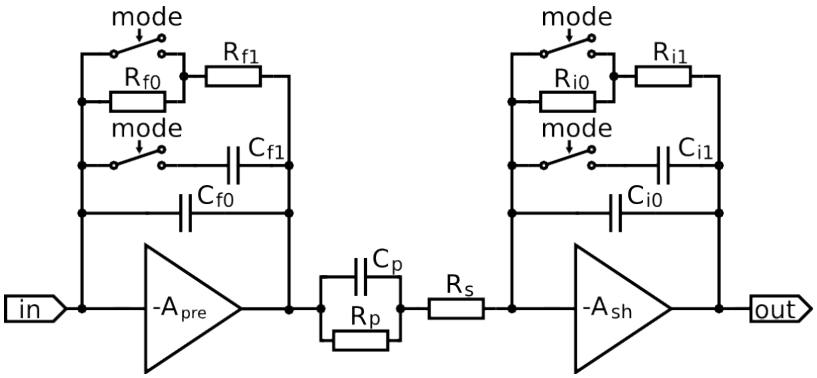
- 8 channel front-end ASIC with preamp & CR-RC shaper Tpeak~60ns, ~9mW (**AMS 0.35um**)
- 8 channel pipeline ADC ASIC, Tsmp<=25MS/s, ~1.2mW/MHz (**AMS 0.35um**)
- FPGA based data concentrator and further readout

New developments for LumiCal detector readout:

- Prototype front-end ASIC **in IBM 130 nm under development…**
- Prototype SAR ADC ASIC **in IBM 130 nm under development…**

Development of front-end in IBM 130nm Preamplifier & Shaper

Block diagram of existing ASIC (in AMS0.35um)

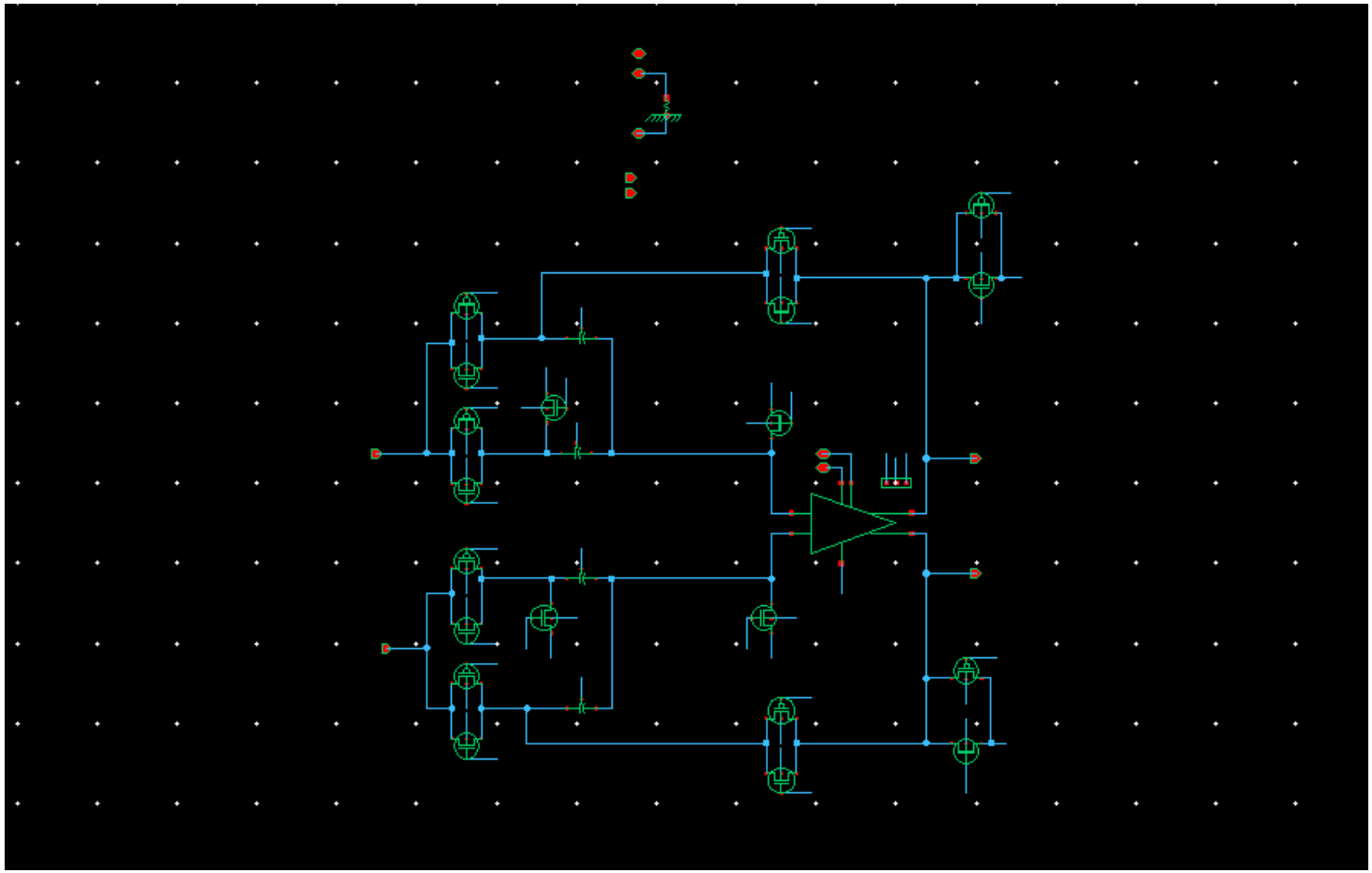


New front-end has very similar architecture ("mode" switch only in the preamplifier)

Design specs:

- 8 channels
- Cdet ≈ 5 ÷ 50pF
- 1st order shaper (Tpeak ≈ 50 ns)
- Variable gain:
  - calibration mode - MIP sensitivity
  - physics mode - input charge up to ~6 pC
- Power pulsing implemented
- Simulated power consumption ~1.5 mW/channel
- ***Design submitted in February 2013***

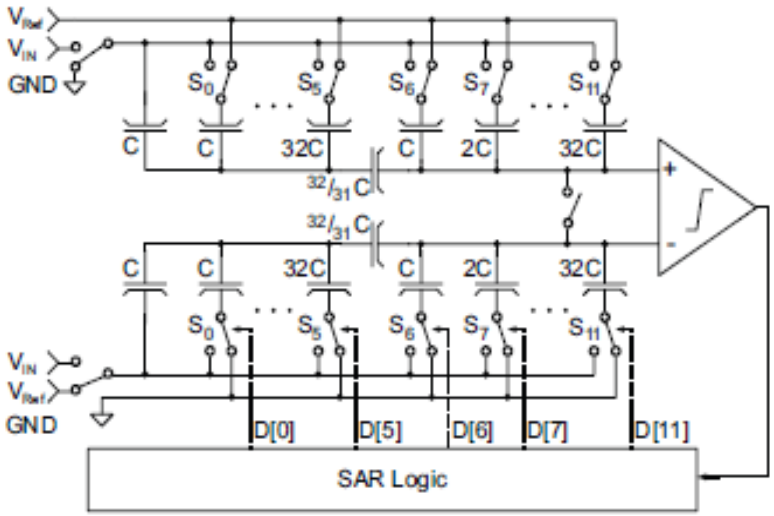
Development of front-end in IBM 130nm SingleEnded-to-Differential converter



Converter has gain of 2

Design submitted February 2013

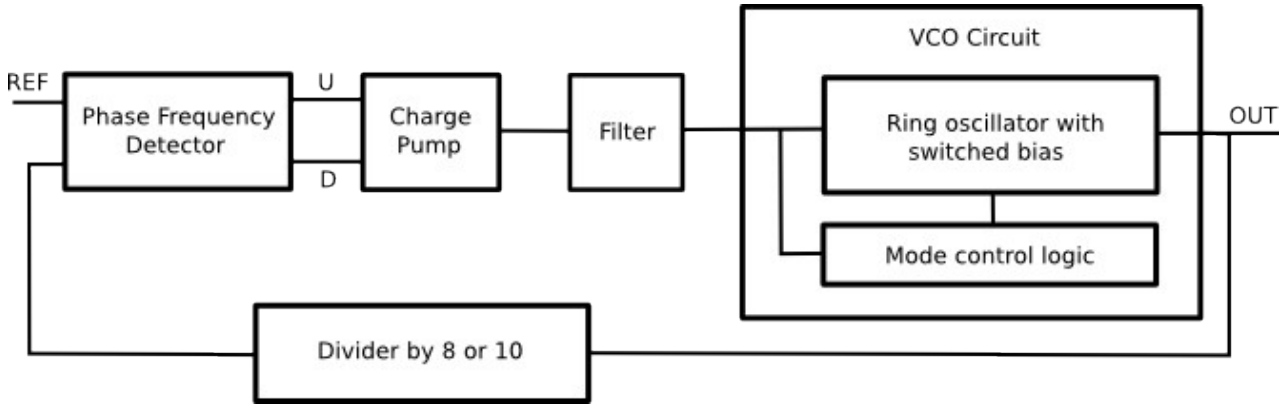
Development of SAR ADC in IBM 130 nm



Designs specs:

- 10-bit ADC
- Architecture: SAR ADC with segmented/split DAC
- Asynchronous SAR logic – Only sampling clk, No fast bit clk
- Scalable frequency (up to ~50 MS/s) and power consumption
- 1-2mW at 40MS/s
- ~150um pitch
- ***Submitted and fabricated in 2012, presently under test…***

Design of PLL for data serialization in IBM 130nm



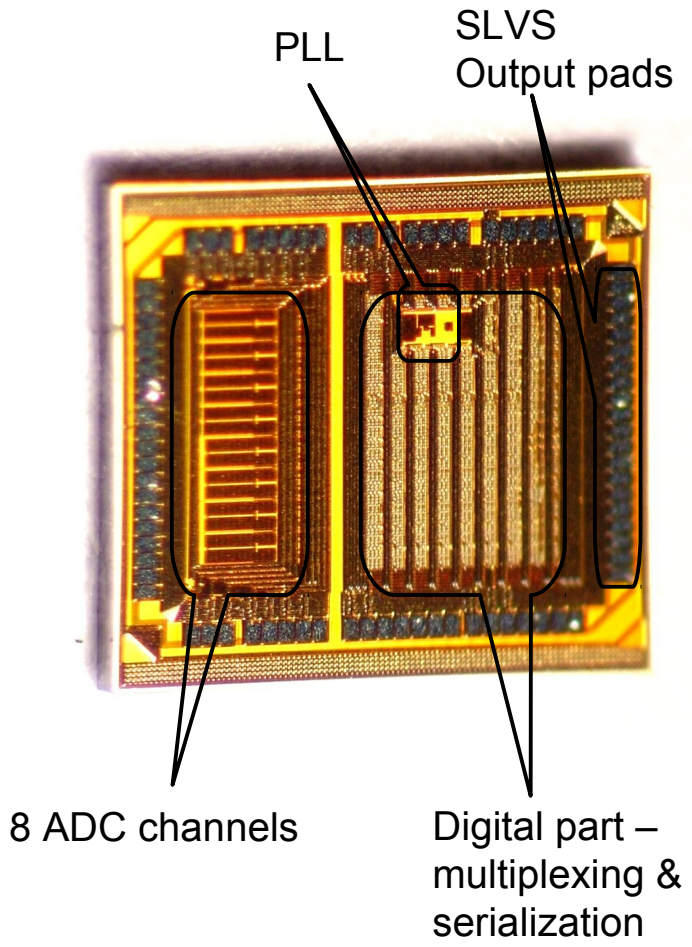
Design specs:

- Architecture: type II PLL with 2nd order filter
- Scalable frequency&power
- Automatically switched VCO freq. range
- VCO frequency range 8MHz – 3GHz,
- VCO frequency division by 6, 8, 10 or 16
- Power consumption <2mW at 3GHz
- ***Submitted and fabricated in 2012, the tests have just started…***

First Pprototypes in IBM 130 nm under tests 10-bit ADC, PLL, SLVS

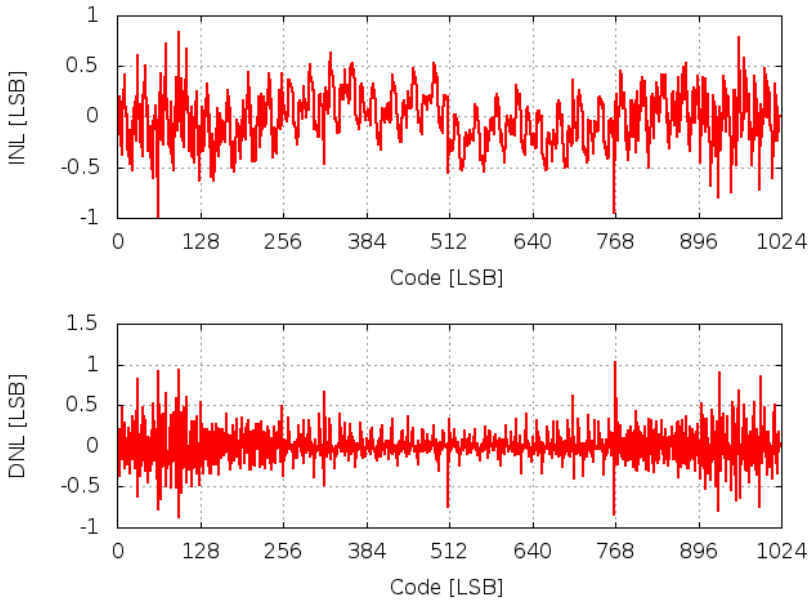
Prototype ASIC contains:

- 10-bit SAR ADC
- PLL
  - Systematic tests are just starting. PLL output clock signal was observed with scope.
- SLVS interface
  - No dedicated tests of SLVS interface were done, but looking at ADC and PLL differential outputs it was veryfied that SLVS driver operates at least up to 700 MHz.

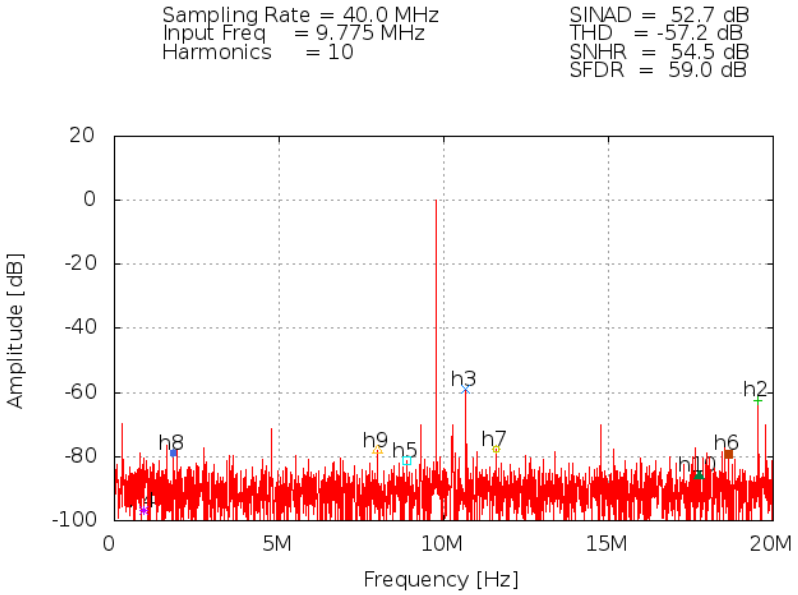


Preliminary measurements of 10-bit ADC
Example measurements at 40Ms/S

Static measurements



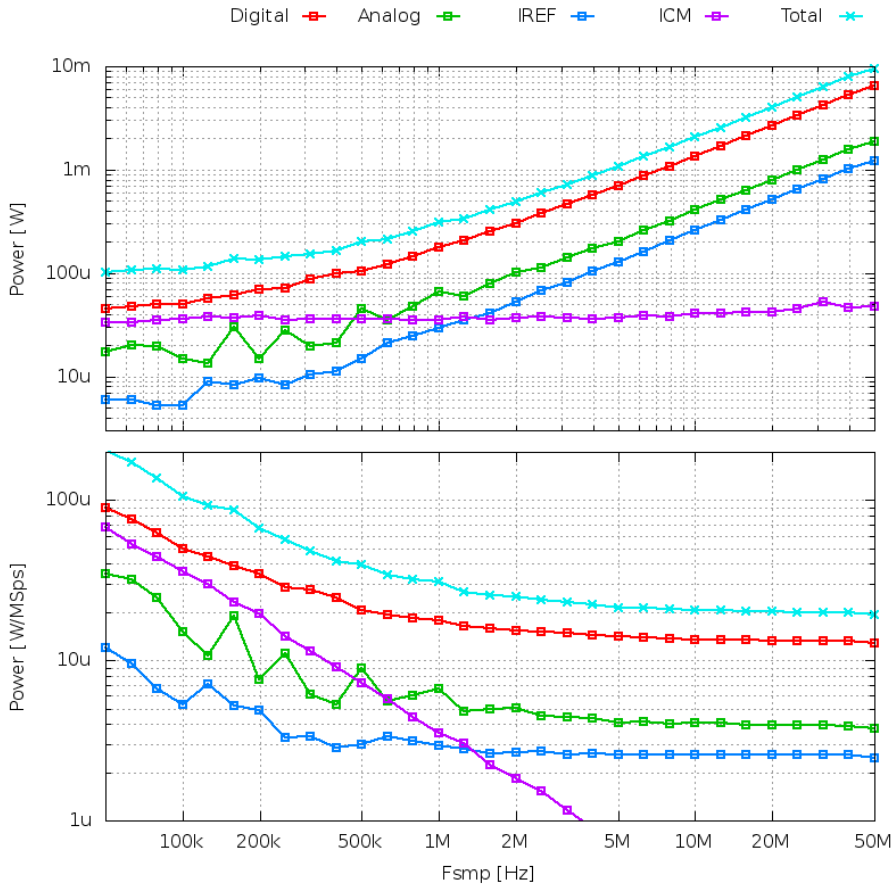
Dynamic measurements



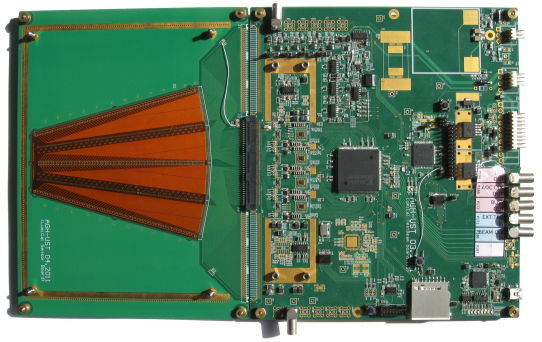
- First conclusion is that ADC works in the whole simulated frequency range, at least up to 50MHz
- Quantitive results will be probably worse than simulated (ENOB 8-9 bits ?)
- Test are in progress...

Preliminary measurements of 10-bit ADC
Power consumption vs sampling frequency

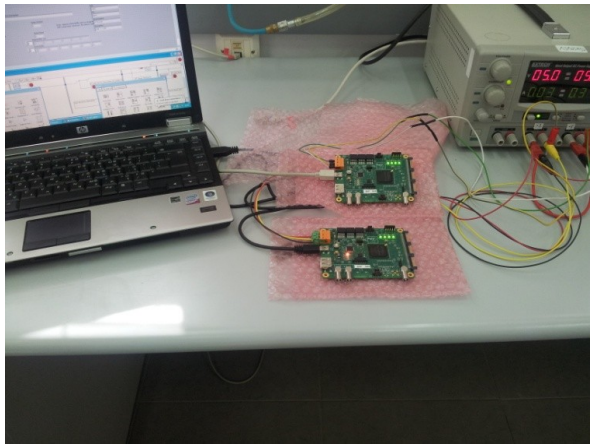
- Power measured for 8 ADC channels
- At 40Ms/S the consumption is about 1 mW per channel – in agreement with simulations



FCAL DAQ status



- By now FCAL uses in test beams the DAQ system based on FPGA readout developed by AGH-UST and EUDET spectrometer system from DESY.
- In the future FCAL wants to use CALICE DAQ2, some work was done in this direction :
  - 4 DIFS (AHCAL) were distributed between Tel Aviv, DESY Zeuthen, IFJ Cracow, and Tel Aviv start to communicate with it,
  - 1 LDA was borrowed from AHCAL to IFJPAN and the works on its implementation have started
  - Key element still missing: FCAL-DIF



Summary and Plans

- New LumiCal readout in IBM 130 nm under development
- First prototype of front-end electronics submitted and should be available in May/June 2013
- First prototypes of 10-bit SAR ADC, PLL, SLVS already produced and presently under test:
  - 10-bit SAR ADC: first results show its functionality, the effective resolution seems to be less than simulated - quantitative measurements are still progoress
  - PLL tests are just starting
  - SLVS interface works well at least up to 700 MHz
- Depending on test progress and results we plan next submission at the turn of 2013/2014