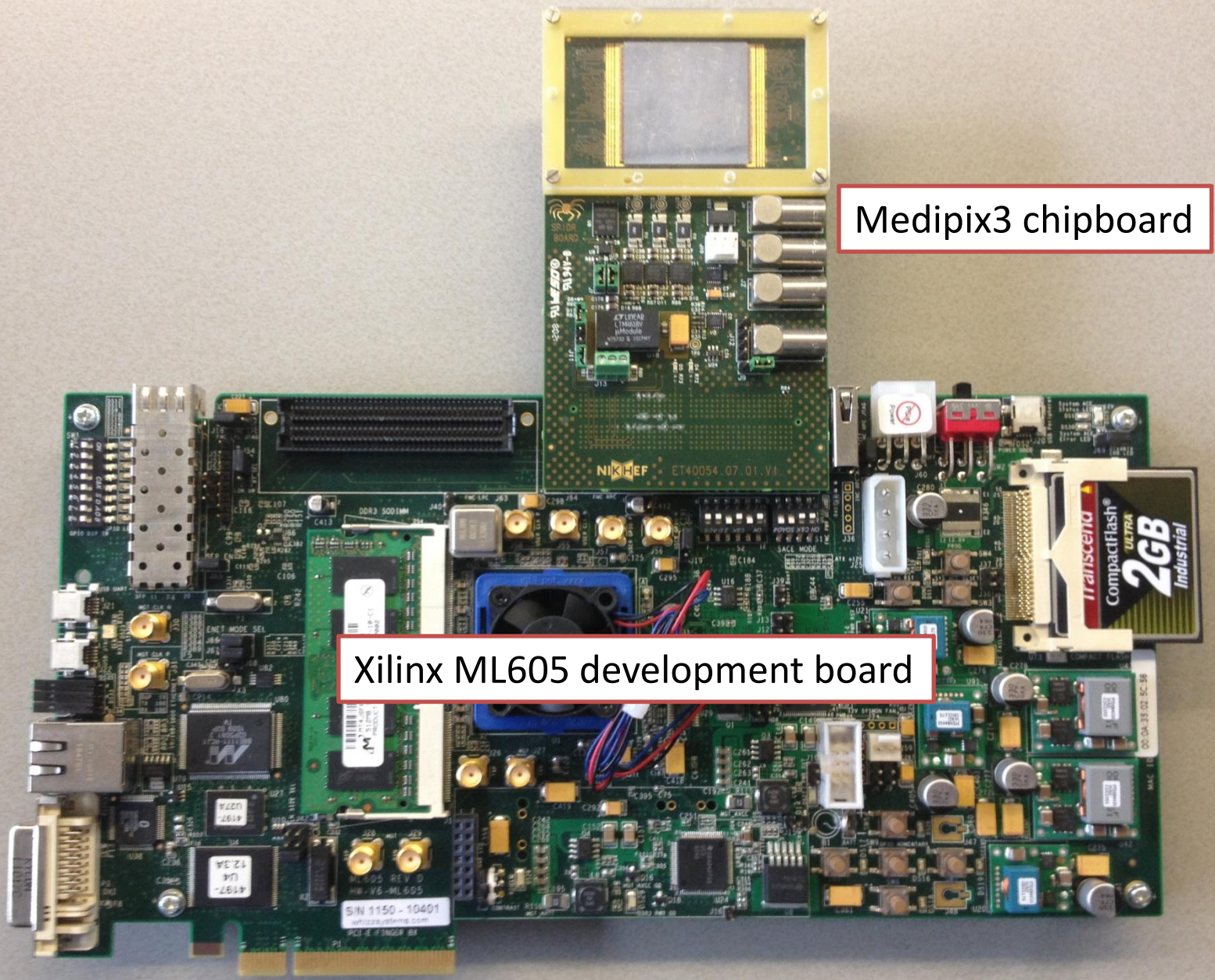
Timepix3 Readout

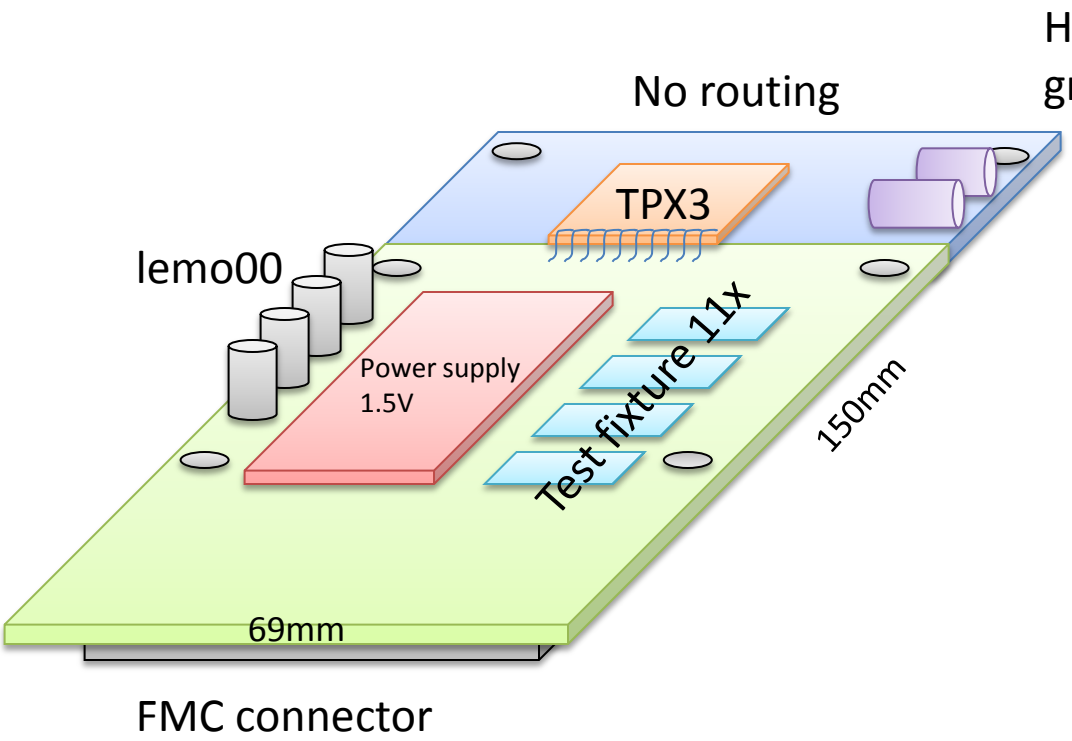
By: Bas van der Heijden & Martin van Beuzekom

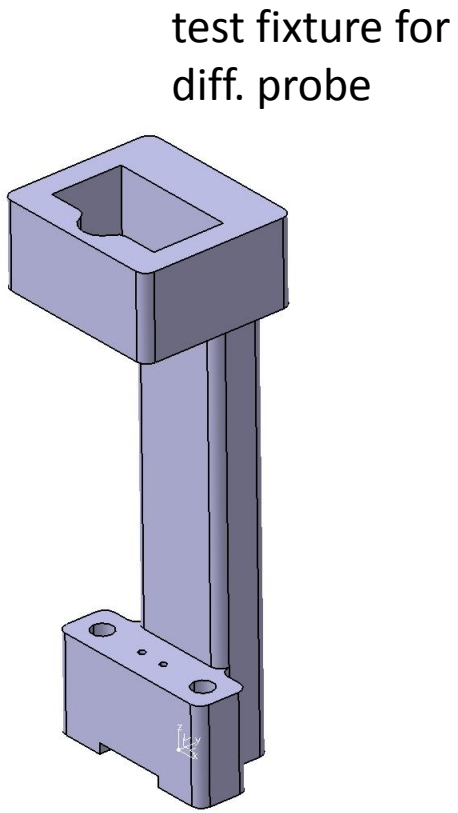
MPX3 and TPX3 readout -> SPIDR

- Speedy PIxel Detector Readout
- Development on a Xilinx evaluation board
  - design a custom (small form factor) FPGA board at a later time
- Aim to read out 1 Timepix3 at full (80 Mhits/s) speed, or multiple Timepix3 chips at lower speed (less links per TPX3)
- Readout bandwidth at least 5 Gbits/s -> use 10 Gigabit ethernet
  - currently using 1 Gigabit ethernet
  - 10 Gbe VHDL code development started
- MPX3.1 and RX readout up and running (low DAQ speed)
- Re-use 'back-end' code for TPX3 readout


Medipix3 chipboard
Xilinx ML605 development board

Timepix3 chipboard

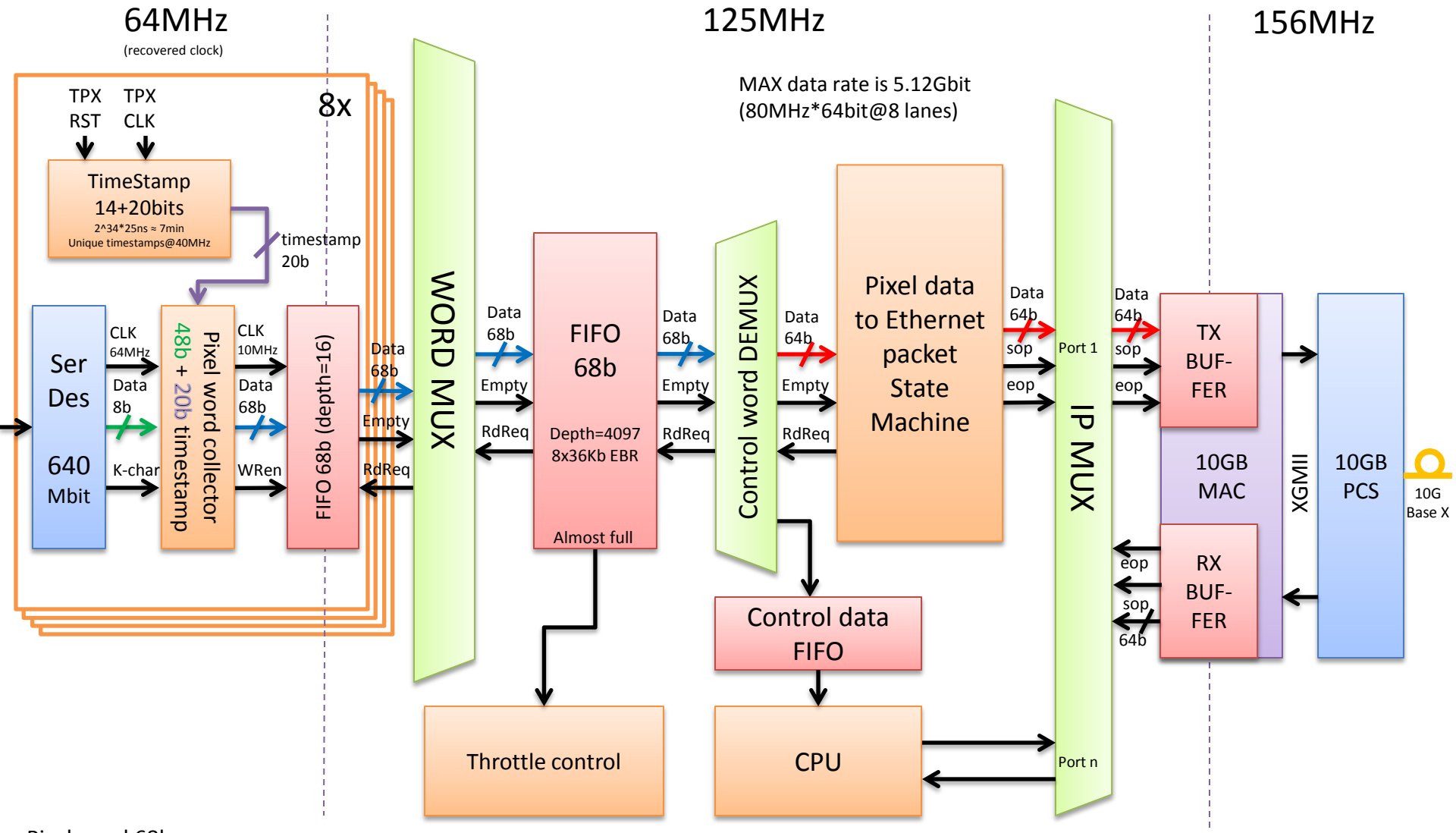




Timepix3 chipboard

- FMC (high pincount 8gbt's)
- Mux for selecting between gbt and regular IO pins on fpga (PI2PCIE2412ZHE)
- ADC & DAC for timepix I^2C
- Lemo's (trig/clk/busy/?)
- VDD(1.5V) VDDA(1.5V) VDDPLL(1.5) (from one DC/DC? CERN sm01c)
- VDDA(3.3 efuse from FMC)
- U&I monitor (ina219)
- CERN rad-hard powersupply's?
- Flash for storing pixel mask (mp25p32 32Mb)
- Simple bias supply for Si sensor? (max668) (12-100V)
- Extra pad and connector/pad for HV bias (1000V) (thick sensor/grid+cathode)
- Probing fixtures for 8x data_out/data_in/clk_in/enable_in
- No routing behind chip (allows removing/thinning of PCB for beamtest)
- Chip cooling?

Fast data transmission path

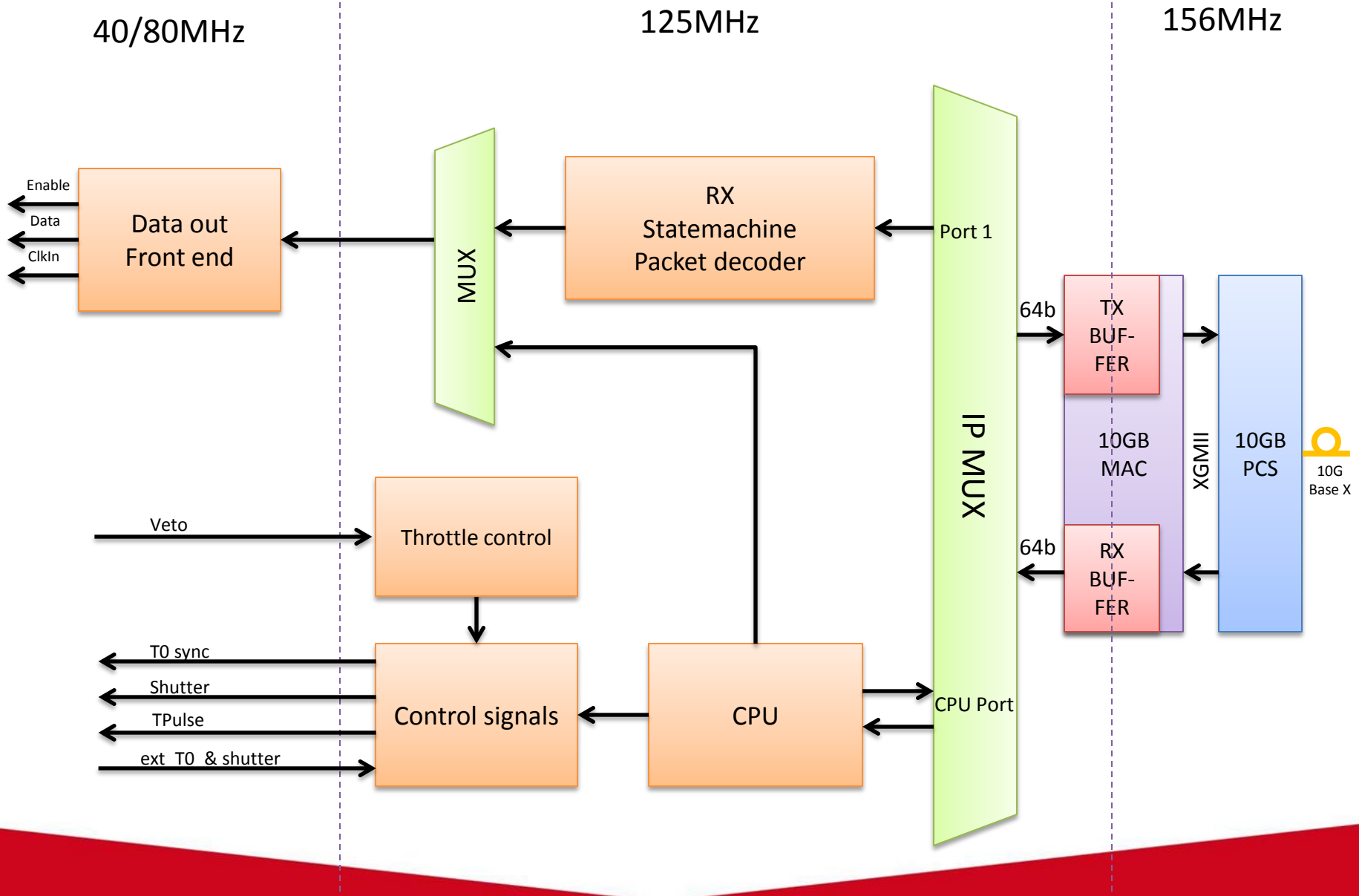


Pixel word 68b

Fast data path summary

- Add 20 bit timestamp to 48 bit pixel packets from TPX3
- data of up to 8 serial links merged into one fifo (round robin)
- strip off 4 bit ctrl header in ethernet packet builder
- use 4 bit ctrl header to route data (to GBE / CPU)
- GBE packet transmitted when either max. length reached or when time-out (configurable)
  - max. collection time given by 14+20 timestamp @40 MHz -> 7 minutes

control data path

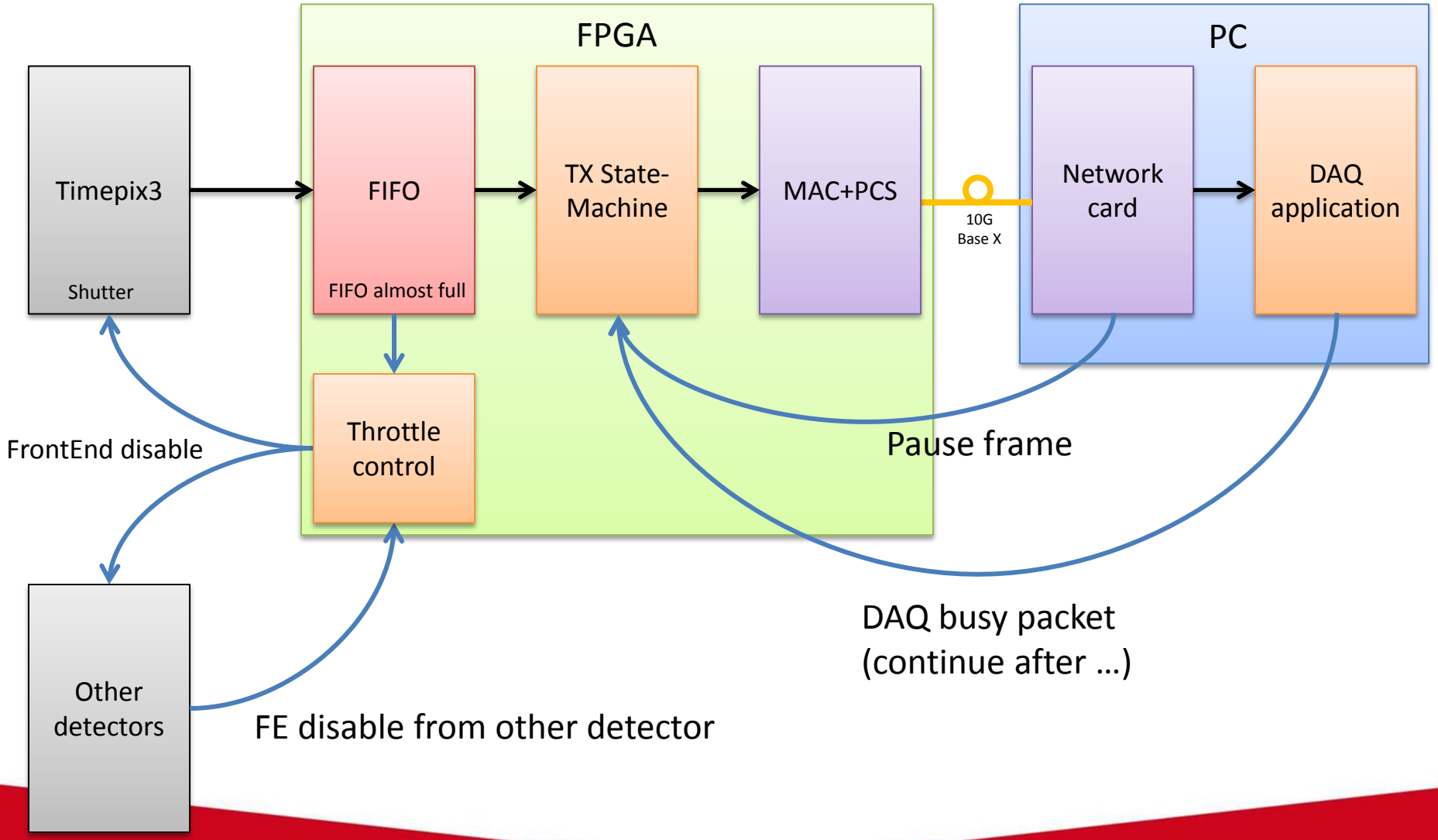


control path summary

- Configuration / control via soft-core CPU (Leon)
- Configuration directly from GBE also possible via Rx statemachine
- Rx statemachine also for throttling (pause frames)
- The Soft-CPU + firmware take care of the HW specific details

- Testpulse generator
- Shutter control

Throttle structure



Hardware status + plan for next 3 months

- 2 hardware engineers full time + support for PCB design
- MPX3+RX readout working
  - 1 lane to MPX3, 1 Gbe to PC
  - not yet all modes are implemented/tested
  - further VHDL development is temporarily stopped; focus on TPX3 specific parts

- Aim to have ready before TPX3 returns from fab:
  - Chipboard
  - 10 GBE (fallback to 1 GBE possible)
  - VHDL statemachine, interface to TPX3
  - Pixel packet receiver and packet builder for 10 GBE

- Later this year:
  - features and testing max. data throughput
  - custom FPGA board
  - tileable chipboard for MPX3 and TPX3 (2 versions)

Software status and plans

- Simultaneous code development for soft-CPU in FPGA and driver library at PC side
- Library (“API”) for MPX3+RX functions almost complete, being tested/debugged at the moment
- Low level TPX3 calls will be added the coming months
- Testprograms (“scripts”) are simply a collection of calls from the library
  - Calls like: “SetDACs”, “openShutter”, “ReadFrame” etc.
  - written in C/C++, compile before running (MS Visual Studio Express 2010, free version)
- Pixel data written to disk and /or on primitive display
  - decoder for offline display (Root) will be provided
- Additional layer of code will be added to adapt to Pixelman API
- High speed DAQ program will follow later this year

Software tools

- (V)HDL graphical entry tool: Ease from HDLworks
- Simulation: Questasim latest version
- Synthesis: Xilinx ISE version 14.x
- Use of SVN

- Software development: MS Visual Studio Express 2010
  - free version
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We would like to have/know:

- Final pinout / dimensions of TPX3 for chipboard
- Up to date manual (working document?)
- Simulation model of TPX3

Other

- S-LVDS issue? converter needed?