SRS, S-ALTRO and DESY GridGEM Module Developments

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HELMHOLTZ GEMEINSCHAFT

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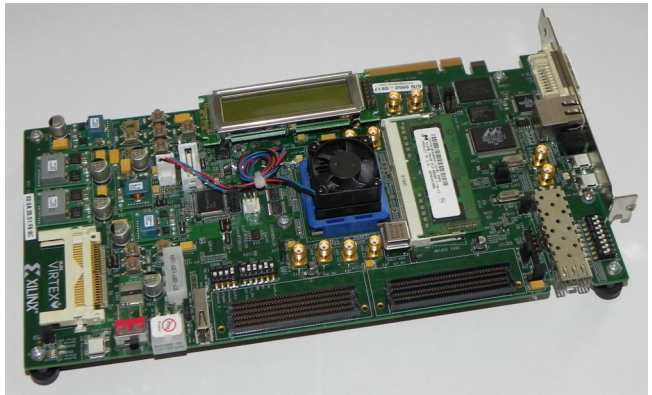
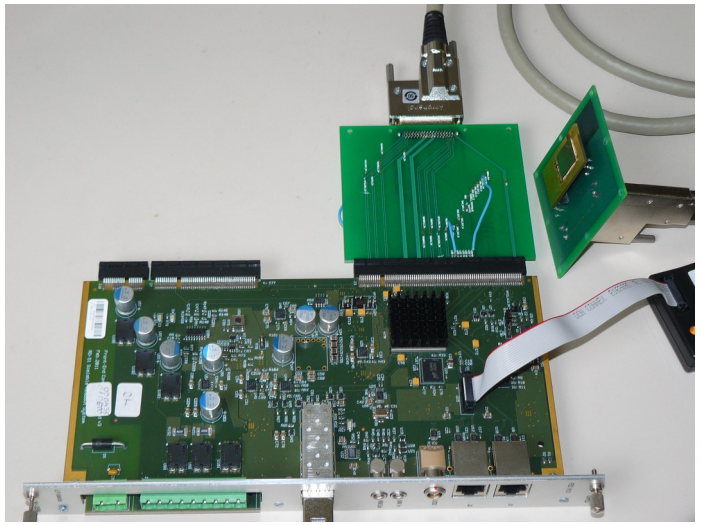
SRS Developments

Slides from Michael Lupberger (University of Bonn)

Status of pixel chip readout system

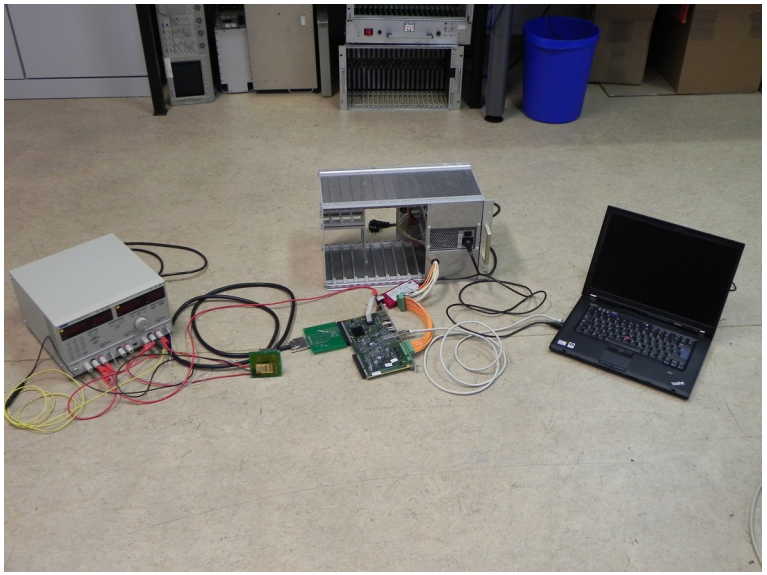
- Subtask 9.2.3 (CEA, DESY, Bonn, NIKHEF): Common readout systems for gaseous detectors. Auxiliary electronics for the read-out of pixellated front-end chips, aimed at highly granular pixel read-out of gas detectors, are to be developed.
- Decision:
  - CEA, DESY, Bonn: Readout Timepix chip with Scalable Readout System (SRS)
  - Nikhef: SPIDER: Readout System for Timepix3
- This presentation: SRS + Timepix
- Status last year:
  - Single chip readout + Xilinx evaluation board working
  - Single Timepix + SRS just started

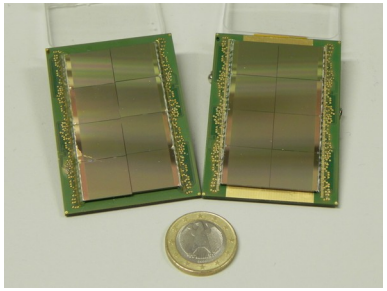




Status 2013

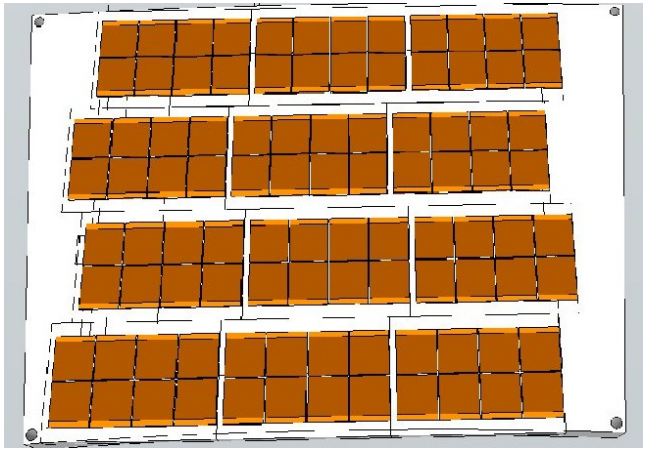
- SRS + Timepix:
  - Milestone MS41 in Jan2013: Intermediate stage
- Additional functionality in firm/software:
  - Triggered data acquisition
  - Threshold equalization
  - DAC scan using oscilloscope (no ADC yet)
  - Calibration using external test pulses
  - Use of DDR2 memory implementation on the way
  - Readout of octoboard
  - System ready for data taking
  - Testbeam at DESY: 2 weeks of operation, excellent performance
- Xilinx evaluation board + Timepix:
  - No further development last year
  - Updated Firmware from SRS will be implemented
  - Readout system of single InGrid chip for the CAST experiment





Outlook for next year

- SRS + Timepix will get an upgrade:
  - HDMI cables between FEC and chip
  - New adapter card to FEC with LVDS drivers
  - Use I2C for control signals
  - DACs to set voltages for a multiplexer (test pulses for chip)
  - ADC to read back chip DACs
- Long term goal: read out 96 chips (12 x octoboards) with 4 FECs
  - Construct a module for the LCTPC prototype at DESY
  - 96 chips = 50% surface coverage
  - Cooling, powering, density of electronic components are challenging

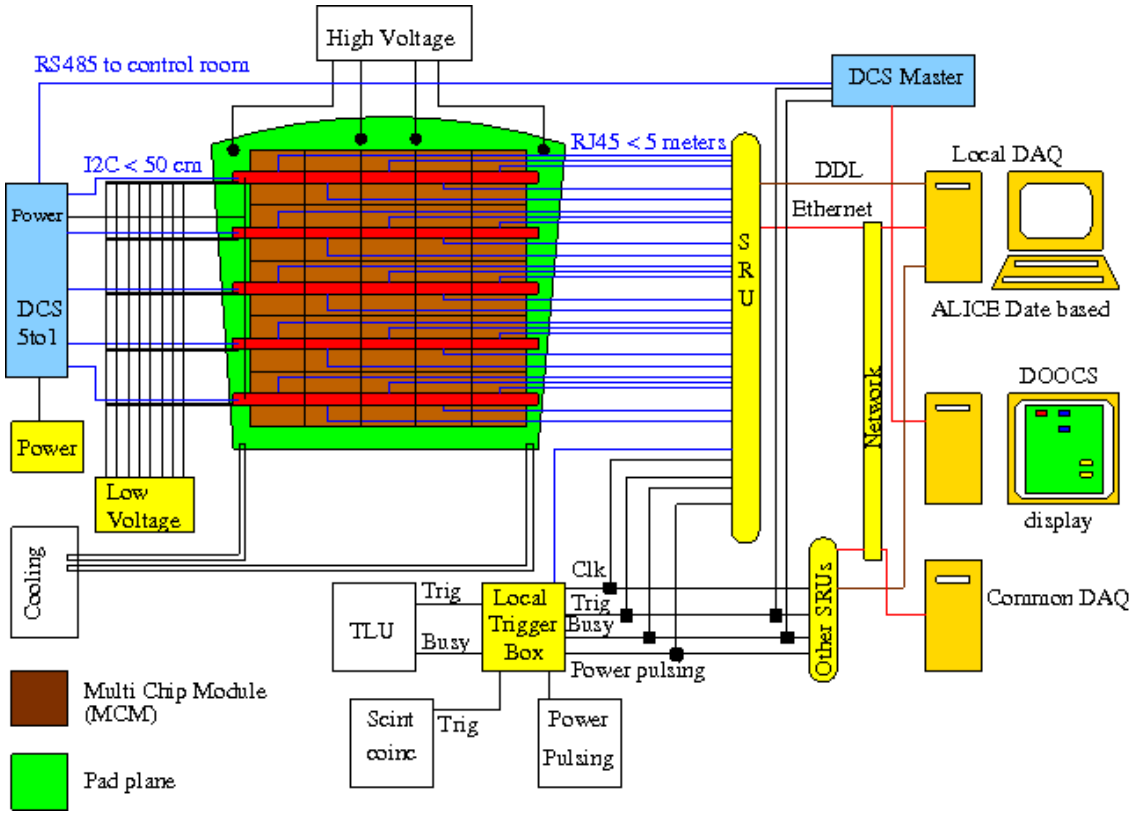


S-ALTRO Developments

Information from Leif Jönnson (Lund University)

Status of the S-ALTRO Development

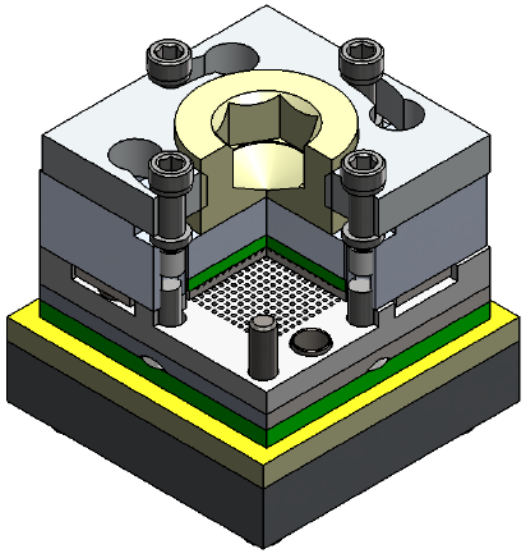
- Advanced project with several different subsystems
- Subsystems need to be developed in parallel

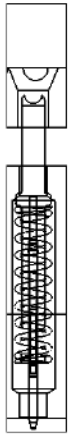


Status of the S-ALTRO Development

- Carrier Board of the S-ALTRO chip
  - Final design is ready
  - Final details of the contract with a company is currently being worked out

- Test Socket for testing S-ALTRO chips on the carrier board
  - Interface to the CERN S-ALTRO test board
  - Design is finished and will be ordered after S-ALTRO carrier boards are being ordered





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DESY

Status of the S-ALTRO Development

- Multi Chip Module Board (MCM-Board)
  - 25 MCM-Boards on each module
    - 3200 channels per module (1 x 8,5 mm^2 sized pads)
  - 8 carrier boards, connectors to the pad plane, a CPLD, connectors for data transfer and LV- support
  - Power pulsing will only switch off the S-ALTRO chips
  - Not ideal for development work and functionality verification
  - Design of a stand alone MCM-prototype board: single S-ALTRO chip and voltage regulators included
  - Programming of the CPLD in Brussels
- Low Voltage Board (LV-board)
  - Supply of up to five MCM-Boards with eight different voltages
  - I/O registers to power on/off voltage regulators (power pulsing)
  - Currently in the process of submitting the design of a prototype

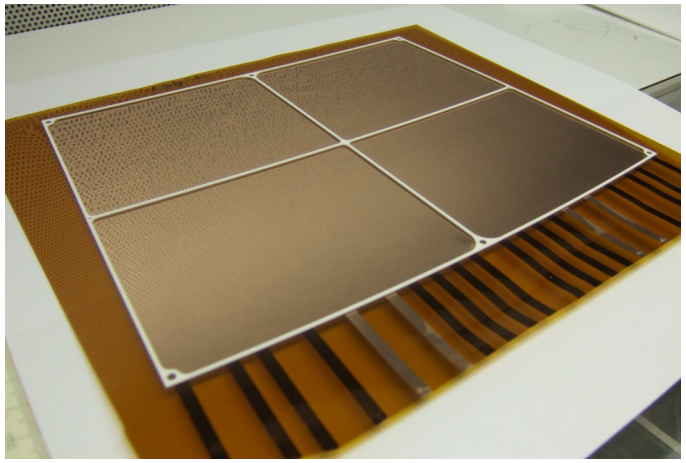
Status of the S-ALTRO Development

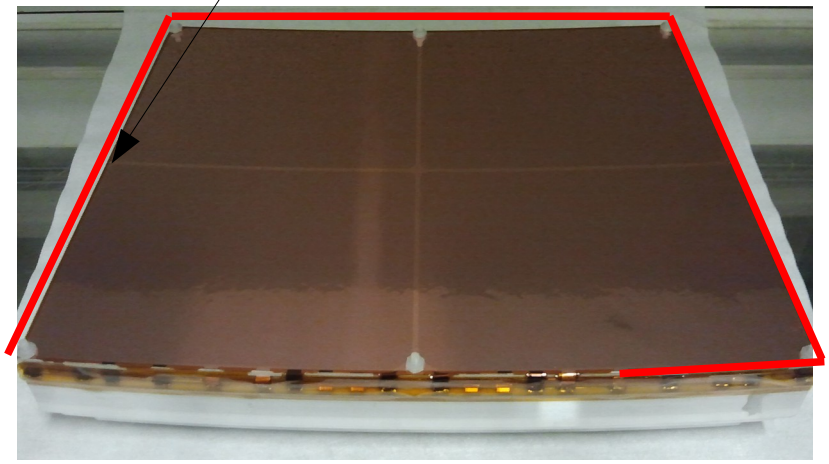
- Monitoring and Control System
  - Master and Slave Module (called 5to1)
  - Submitting phase of the design document
  - Firmware of both boards nearly finished
  - 700 parameters will be monitored per module
  - DOOCS control system to monitor the parameters is under discussion
- Serial Readout Unit (SRU)
  - Is ready to be picked up at CERN
  - Modifications on the firmware needs to be done
- Open Questions
  - Connectors on the final MCM-board to connect to the outer world
  - How is the power pulsing going to be implemented
  - How is the trigger going to be implemented
  - The two latter questions are mainly that the interfacing to Serial Readout Unit has to be fully understood.

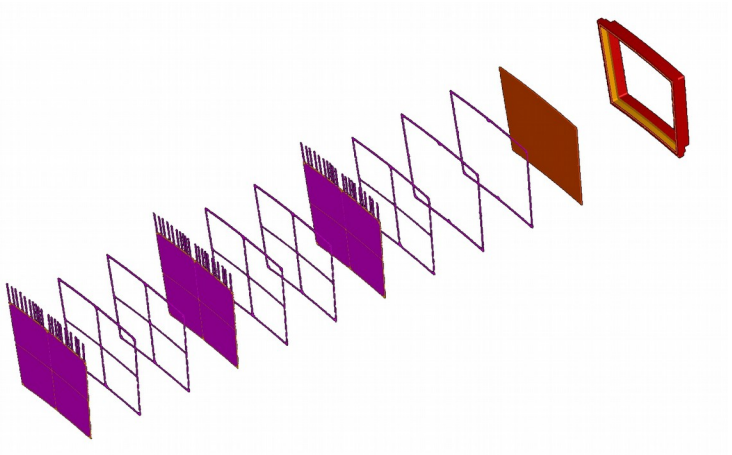
DESY GridGEM Module Developments

DESY GridGEM Module

- Triple GEM Module with pad readout
- Integrated support structure
- Aluminum Oxide grid
- Fully sensitive readout board ~23 x 17 cm^2
  - 4829 readout pads (size 1.26 x 5.85 mm^2)
- Bottom side of the GEM divided in 4 sectors
  - Reduces energy stored in one sector to avoid destructive discharges
- Additional field shaping electrode around the module (wire) to reduce field distortions

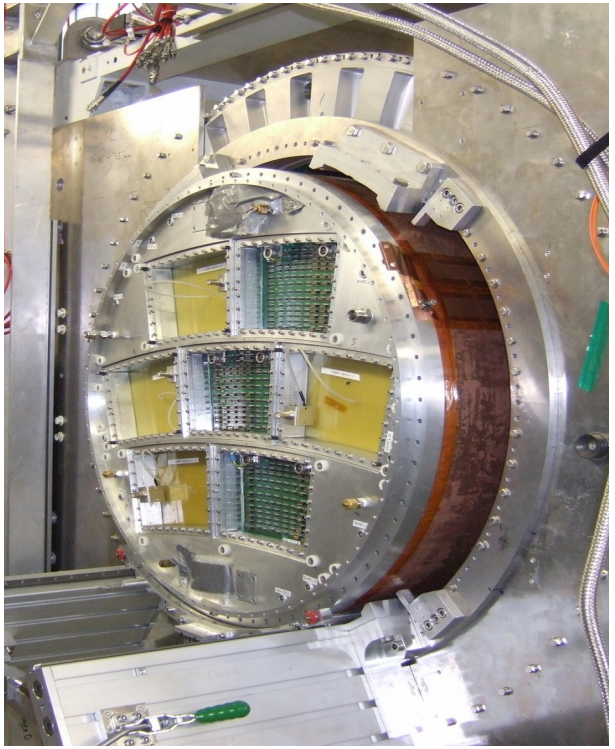


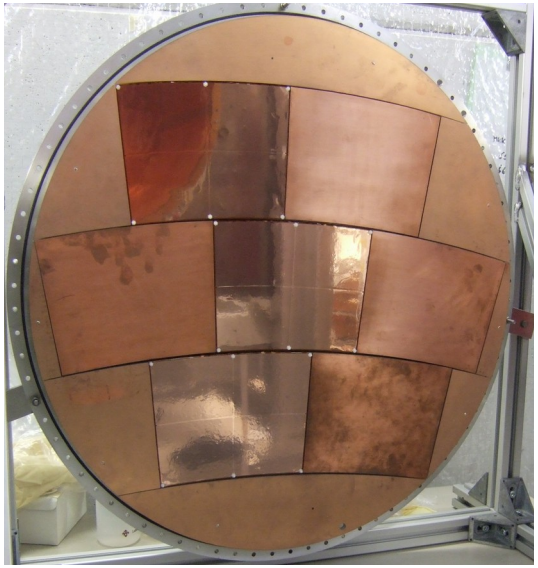




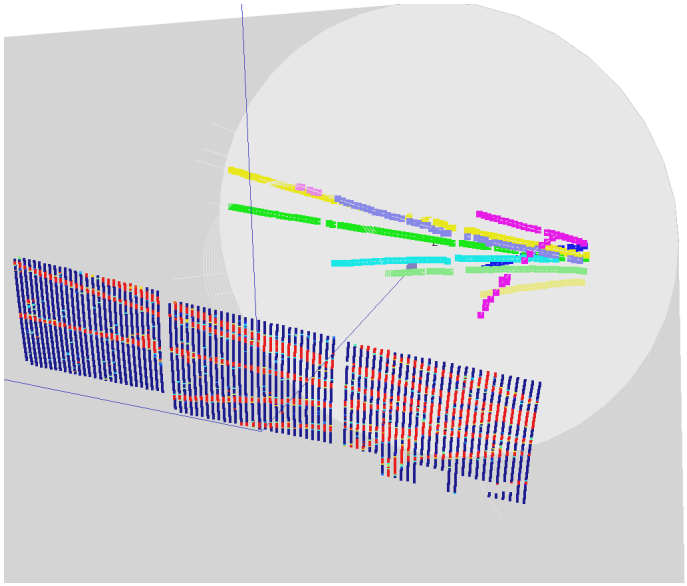
Test Beam Setup

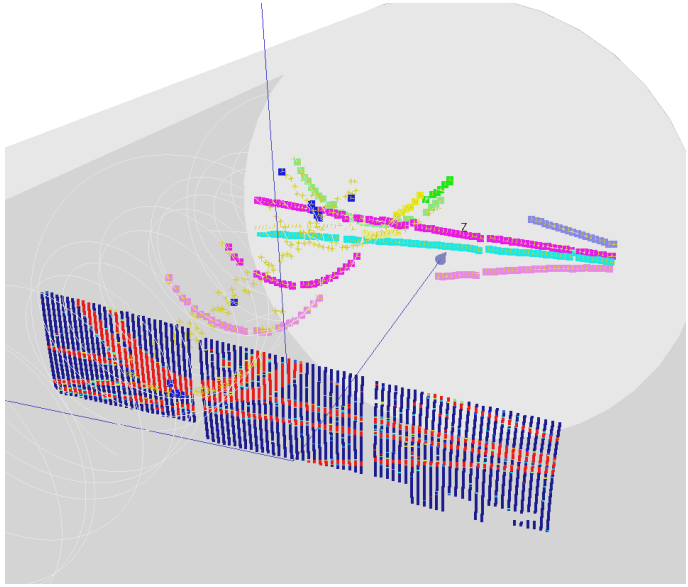
- 3 DESY GridGEM Modules
- Beam area T24/1 at the DESY II accelerator
- ALTRO electronics
- Readout half of the three modules
- ~7200 channels along the beam profile
- 3.5 M events in ~50 hours





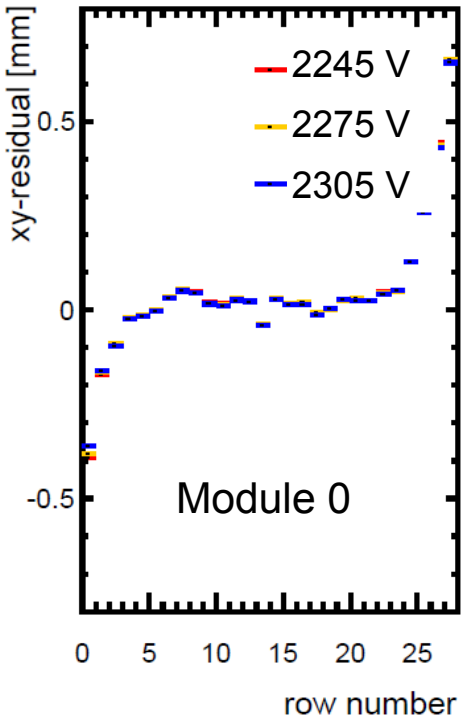
Event Displays

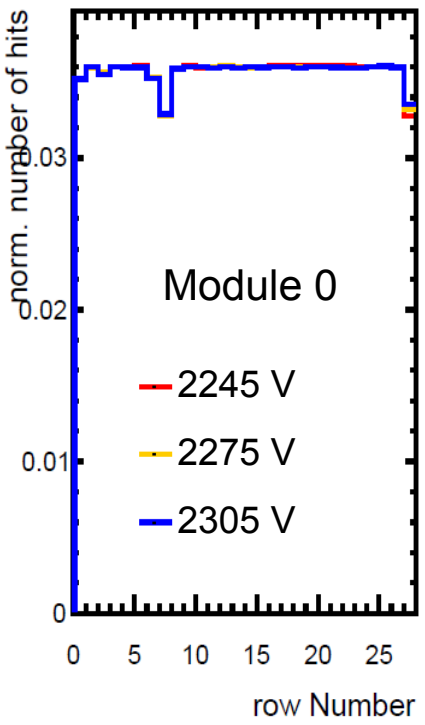




Field Distortions

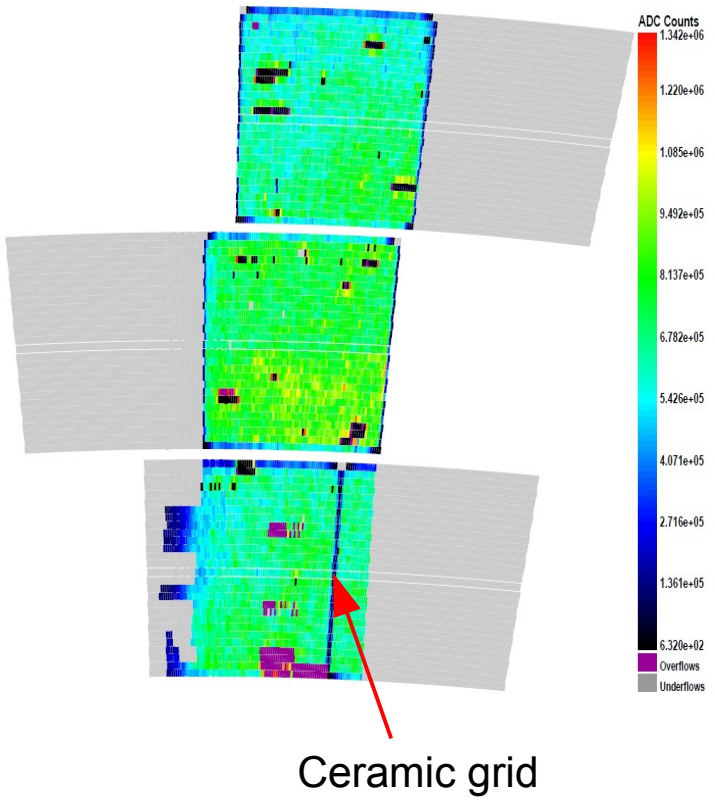
- Field distortions at the edge of the module alter the path of the primary electrons
- 30% of the hit efficiency was recovered with the additional electrode (reaching >90%)
- Small influence on the residual of the hits
- Can be corrected during analysis





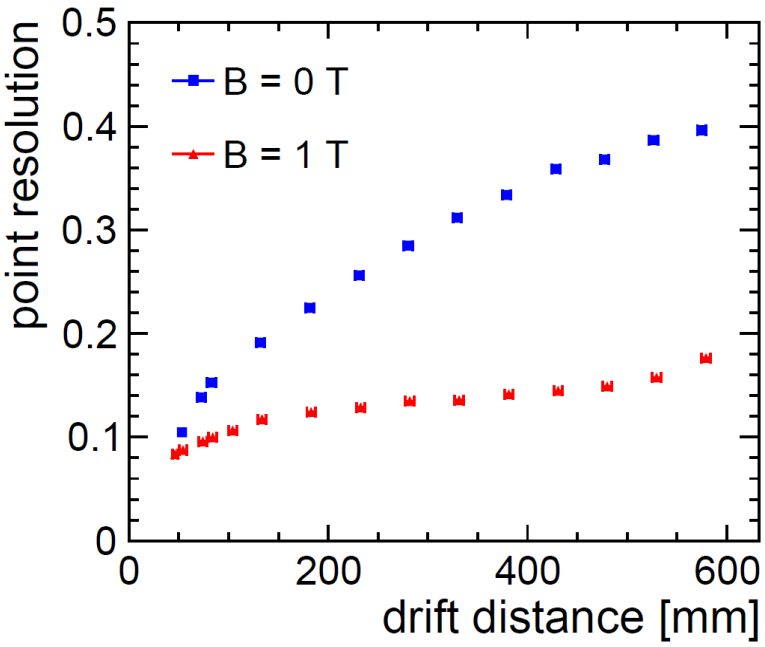
Efficiency

- X-scan while taking data
- Hit efficiency very high but charge efficiency reduced at the outer rows
- Reduced gain or reduced number of primary electrons
- Readout system difficult to assemble
  - Two days to complete setup
  - Dead and noisy channels



Transverse Point Resolution

- Track finding and fitting with CLUPATRA
  - Track fitting tool for ILD TPC simulation
- Point Resolution for B=0 T shows the expected behavior
- Point Resolution for B=1 T displays a rise at large drift distances



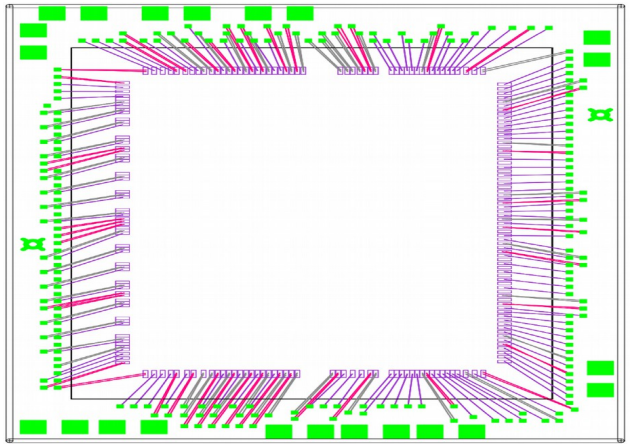
Summary

- The SRS project is getting closer to realize a fully pixelized readout of a module
- Test setups for the S-ALTRO readout are currently under development and most parts are close to be submitted
- The DESY GridGEM Module was developed further and a beam test with 3 modules was performed
- The results look promising but need further analysis

Backup

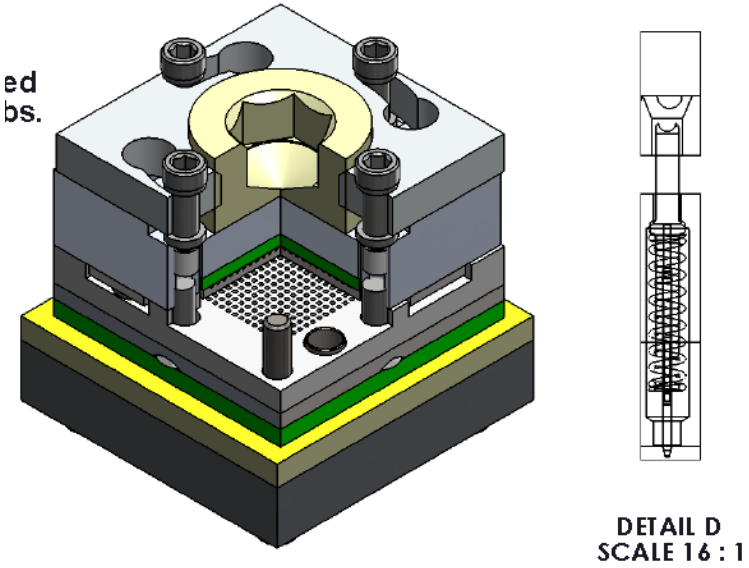
Status of the SALTRO-development in Lund

1) Carrier board



Size: 12.0 x 8.9 mm^2 (die; 8.7 x 6.2 mm^2)
Design ready, final modification due to power pulsing
Specification document ready
Contact with company for mounting components has been established and final discussions are ongoing
Bids for production of boards awaiting

2) Test socket for testing SALTRO-chips on carrier boards



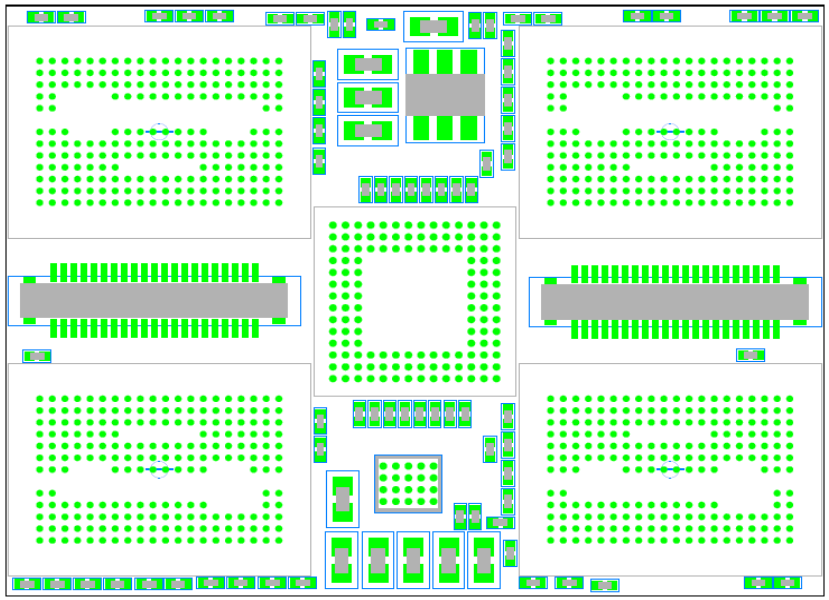
Contact with company established
Will be ordered as soon as we get green light from the company mounting the components on the carrier board

3) The MCM-board

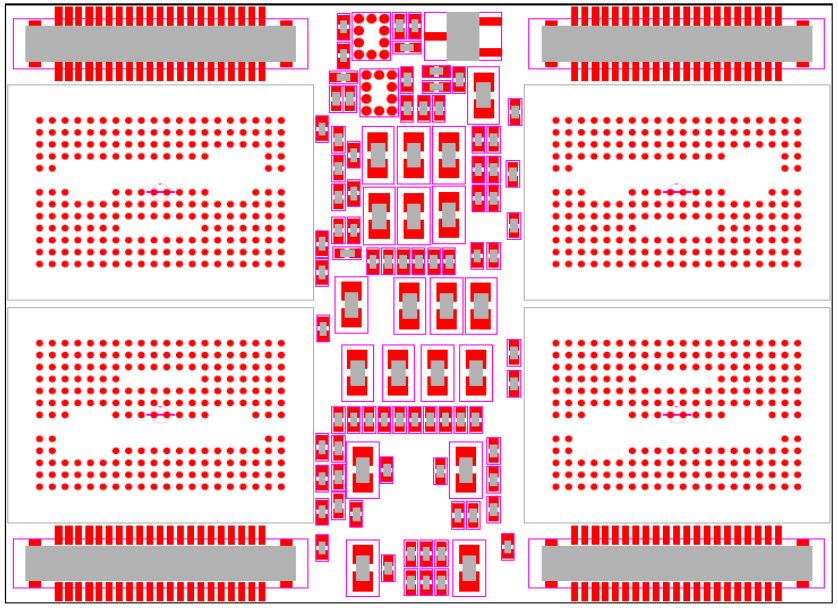
Size: 32.5 x 25 mm^2
The main components on this board are:
8 carrier boards, connectors to the pad plane, a CPLD, connectors for data transfer and LV-support

Layout almost ready; type of CPLD still to be decided as well as connectors for LV support and data transfer and how the power pulsing will be handled.
The power pulsing will only switch of the SALTRO chips
Power consumption 12mW at 5 Hz (compared to 757 mW by continuous running)

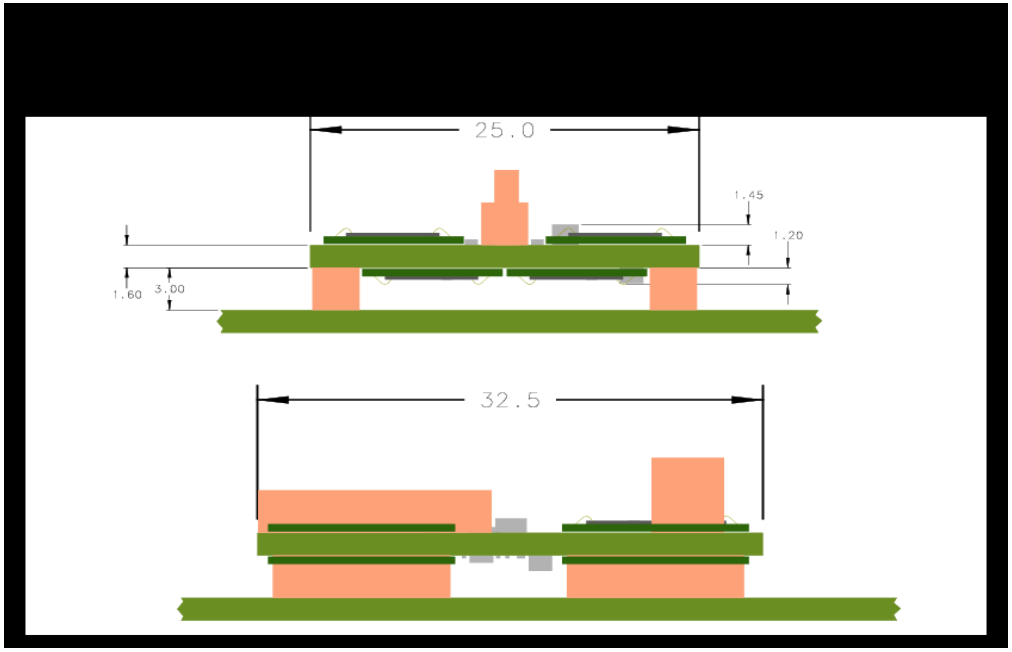
Top side



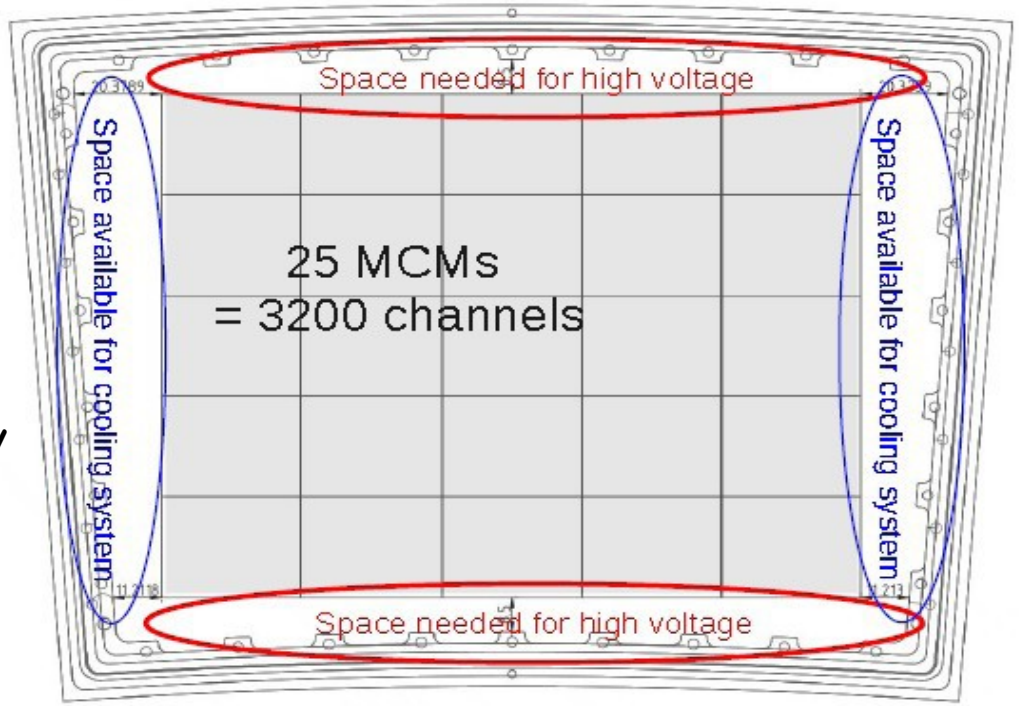
Below side



Side view of the board assembly
Since it was necessary to add two layers (8 instead of 6) the carrier board has become 0.2 mm thicker.
It means that the available space For cooling planes between the MCM and the pad plane is 1.6 mm.



Organization of the MCM-boards within a module
3200 channels corresponds to a pad size of 1 x 8.5 mm if the whole area of the module is covered.
The construction of the pad plane and the cooling system is the responsibility of the Japanese groups



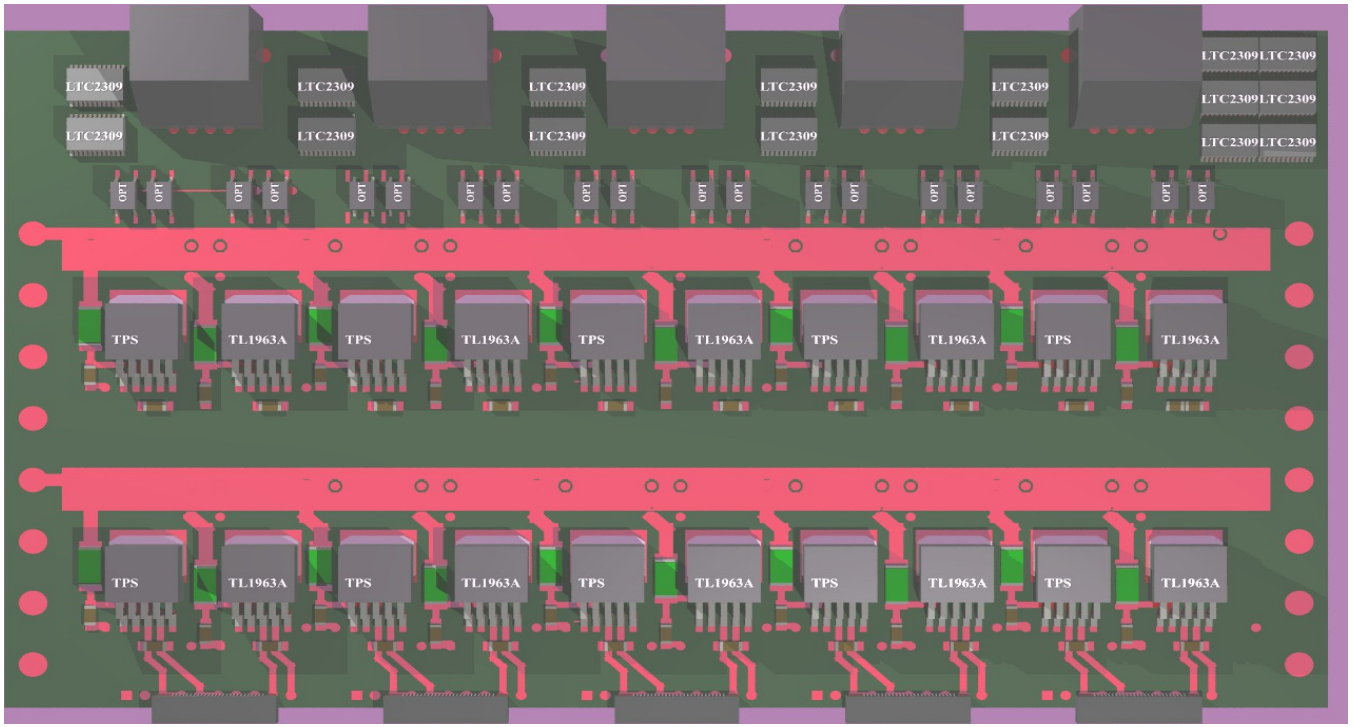
4) LV-board

1st design made. However the number of voltage regulators needed depends on which CPLD we decide to use
Voltage regulators are placed on both sides of the board
Size of the board 184 x 110 mm2

We will implement the following functions: switching on/off the voltage regulators dynamically, monitoring of the voltages and currents, monitoring of the temperature on the LV-board and the MCM-board

RJ45 connectors for serial readout

LV connection



LV connection

Towards MCM-board

Schematic view of the setup with serial readout using an SRU

In the solution shown below the SRU communicates directly with the MCM-board via the Data Trigger Control (DTC) link.
This requires however that the FPGA firmware on the SRU is modified
Depending on the type of CPLD we might need 8 or 9 different voltages