A Trigger/Timing Logic Unit for AIDA

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AIDA II ANNUAL MEETING
10^{th} - 12^{th} April, 2013
INFN - LNF, Frascati, Italy

Outline

A Trigger/Timing Logic Unit for AIDA

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The AIDA TLU project

Hardware

mini-TLU connectivity

HDMI Fanout

mini-TLU components

Firmware

IPbus

Handshake controller

TDC

DAQ Software

Next steps

Conclusions

The AIDA TLU project

New TLU must provide:

- Increased trigger rate: Move to one-trigger-per-particle for LHC detectors.
- FPGA system available for lifetime of AIDA.
- Cheaper to produce TLUs for integration in home labs.

Project phases

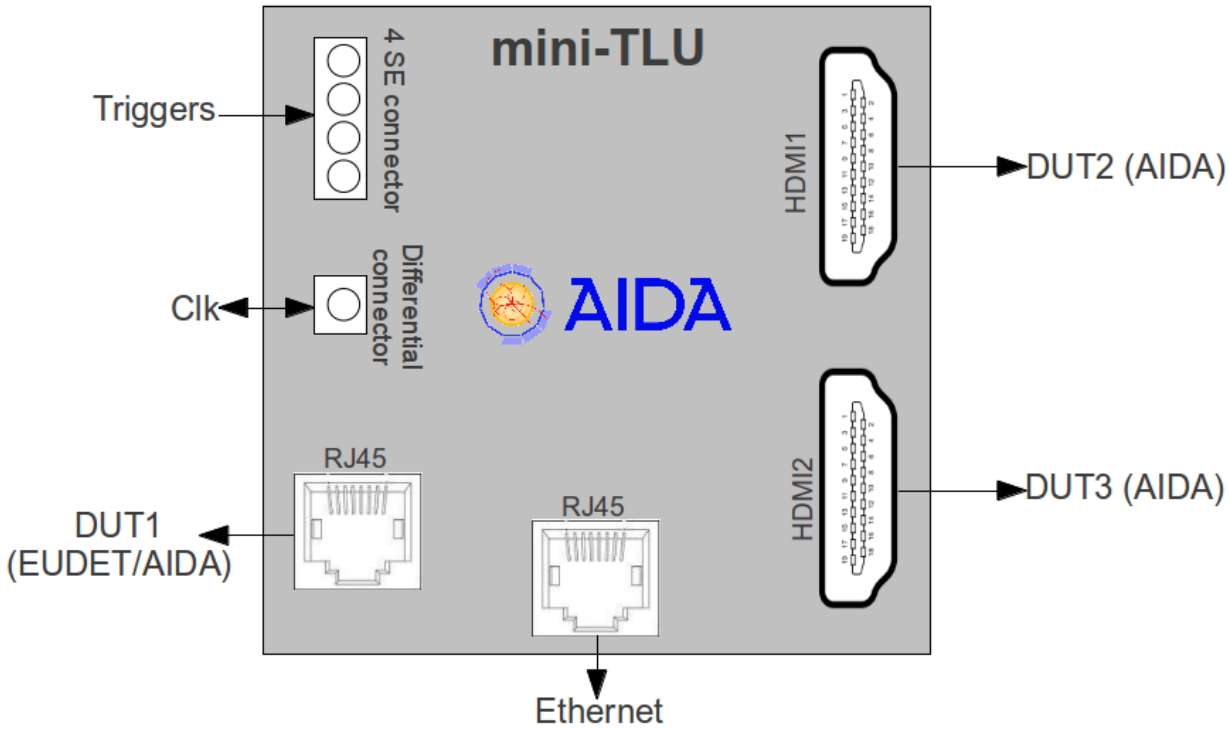
- Build a prototype to test out ideas: mini-TLU. It must be cheaper and easier to produce than EUDET and final TLUs.
- Build the final TLU with complete capabilities and new needs learnt from mini-TLU.

Developers:

- F. Crescioli[1] $\Rightarrow$ Software
- D. Cussans[2] $\Rightarrow$ Hardware, firmware and PC
- A. Dosil Suárez[3] $\Rightarrow$ Firmware

[1] Laboratoire de physique nucléaire et des hautes énergies, Paris, France
[2] University of Bristol, Bristol, United Kingdom
[3] University of Santiago de Compostela, Spain

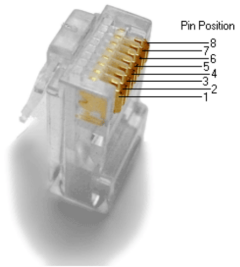
mini-TLU connectivity



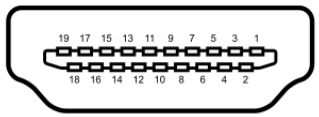
Connections:

- 4 Trigger input: Lemo single-pole size-00
- Clock I/O: Lemo two-pole size-00
- 1 RJ45 EUDET/AIDA style (4 differential signals)
- 2 HDMI AIDA style (5 differential signals)
- 1 Ethernet connection (copper or optical)

mini-TLU signals



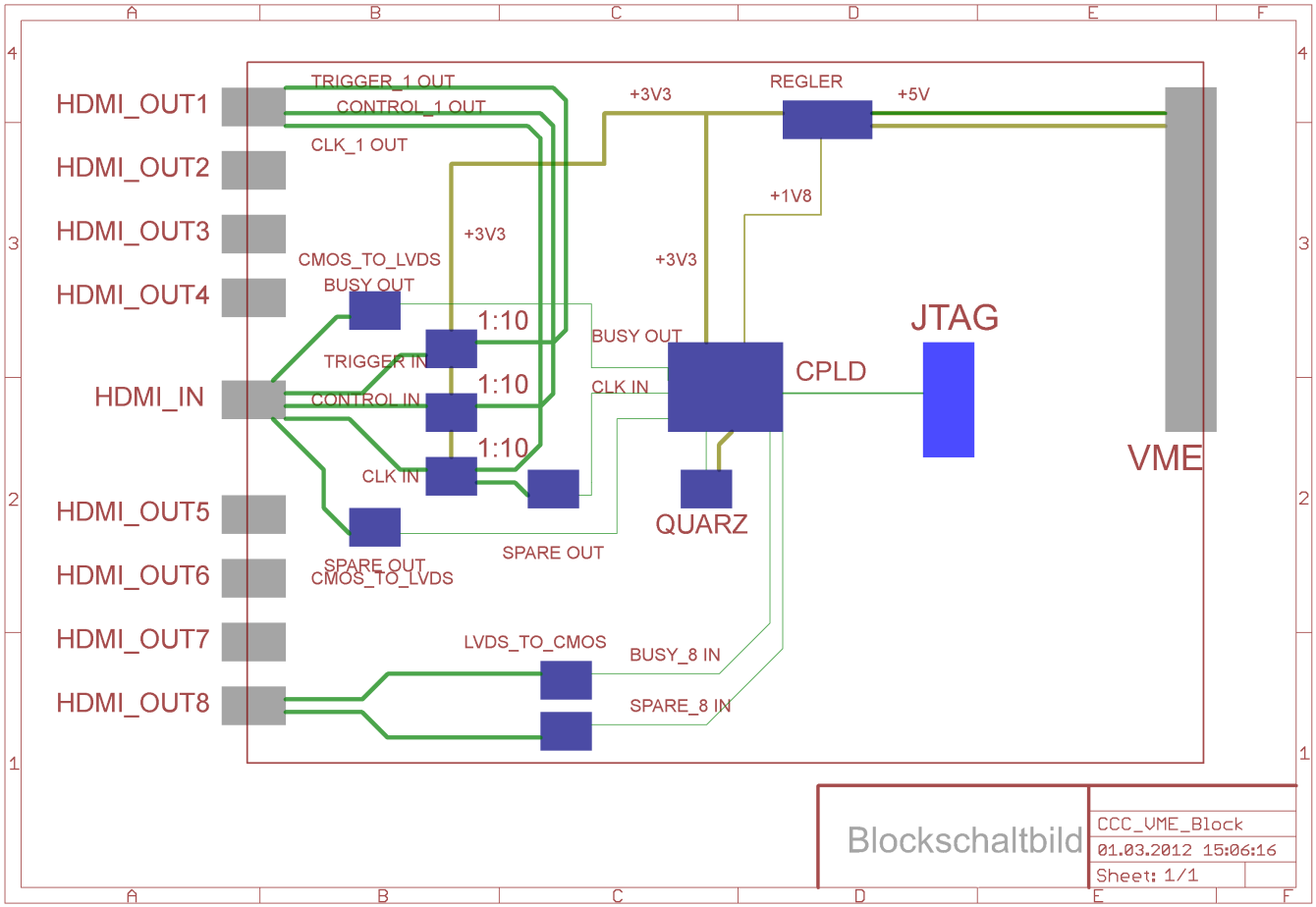
Name	Description	Signal type
Clock	Input/Output: Clock from/to DUT	LVDS
Busy	Input: Busy signal from DUT	LVDS
Control	Output: Shutter, spill-on, power-cycling	LVDS
Trigger	Output: Trigger signal to DUT	LVDS



Name	Description	Signal type
Clock	Output: Clock to DUT	LVDS
Busy	Input: Busy signal from device	LVDS
Control	Output: Shutter, spill-on, power-cycling	LVDS
Trigger	Output: Trigger signal to DUT	LVDS
Spare	Input: General purpose Input	LVDS

HDMI Fannout

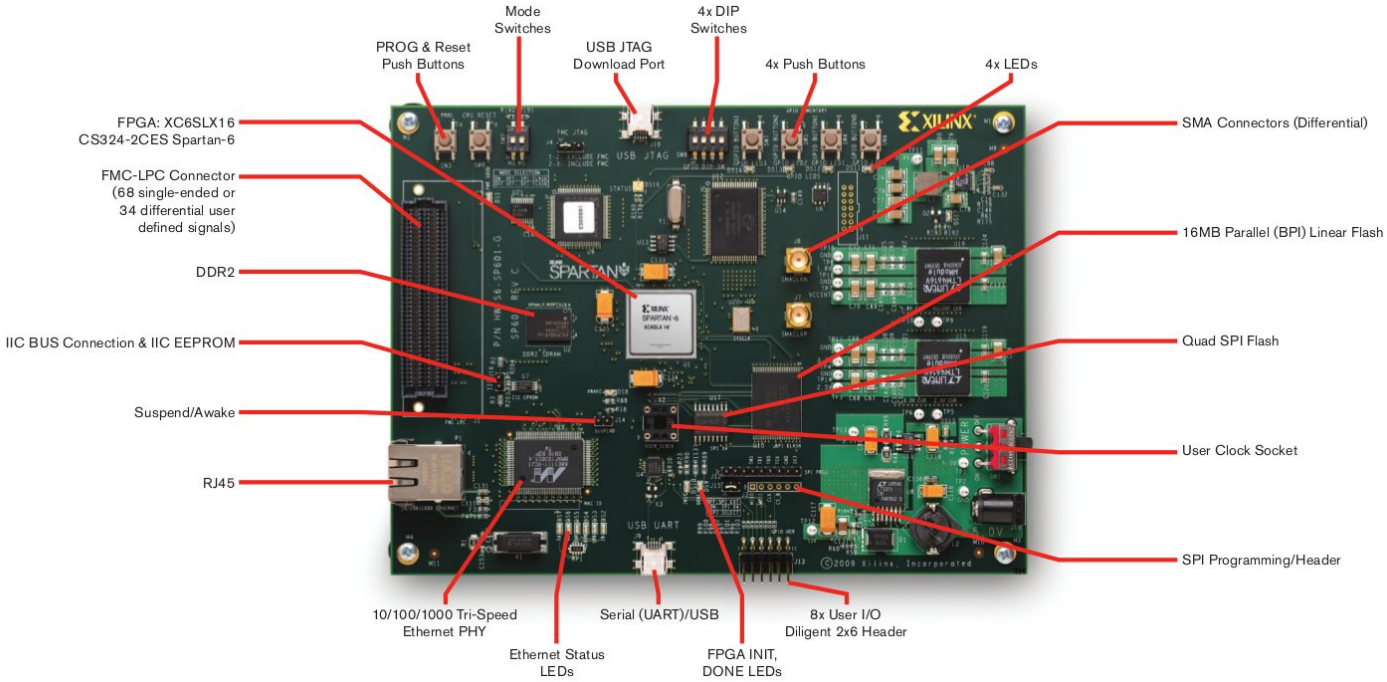
HDMI Fannout designed by the CALICE collaboration (Mainz)



- 1:8 fanout providing 3 differential signals.
- 8:1 fanin providing 2 differential signals.

mini-TLU components

Xilinx sp601



Clocking	Internal 200 MHz oscillator Socket for a single-ended user oscillator SMA connectors
Communication	10/100/1000 Tri-Speed Ethernet PHY
Expansion connectors	FMC-LPC connector (68 se. or 34 diff. user defined signals) 8 User I/O (Digilent 2x6 Header)

Firmware

- IPbus
- TDC
- Handshake controller
- Control for discriminator threshold DAC
- Controller for programmable shutter/spill-on/power-cycling signal

IPbus

Description:

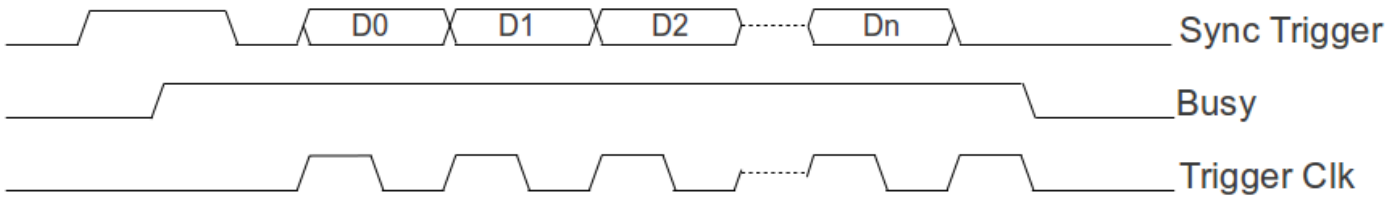
IPbus is a simple way to control and communicate μTCA-based hardware via the IPbus protocol

IPbus protocol:

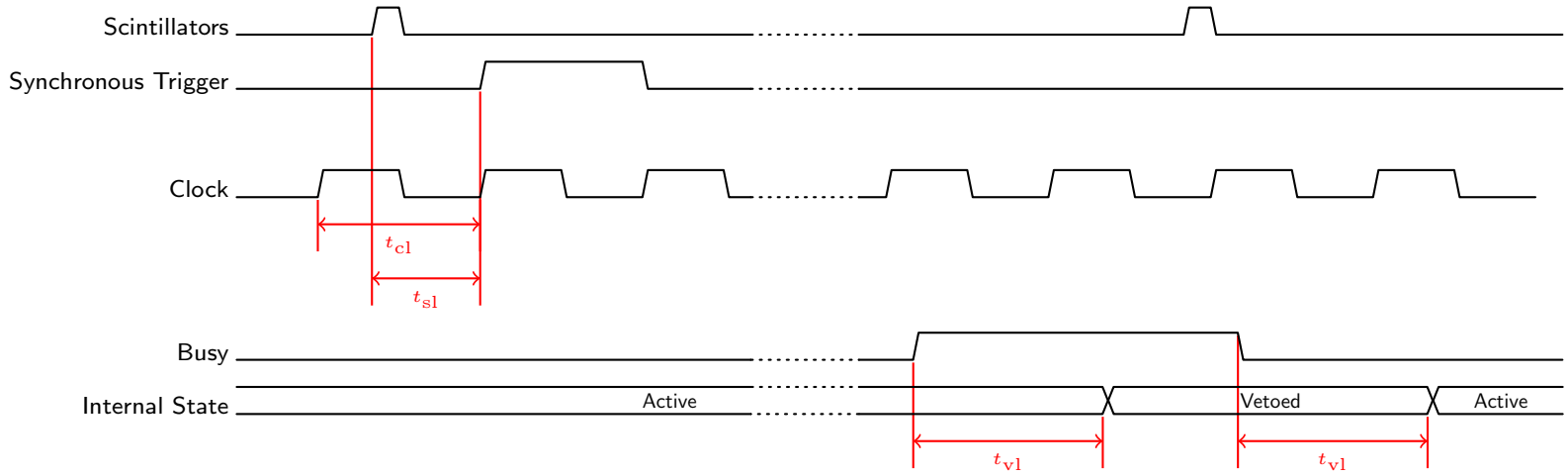
- Control hardware via IP over Ethernet
- Uses UDP as transport protocol
- Source code available to download
- IPbus firmware is written in VHDL
- Small footprint
- Originally developed by: J. Mans, *et al.*.

TLU-DUT Handshakes

EUDET Handshake (Trigger/busy with trigger number)



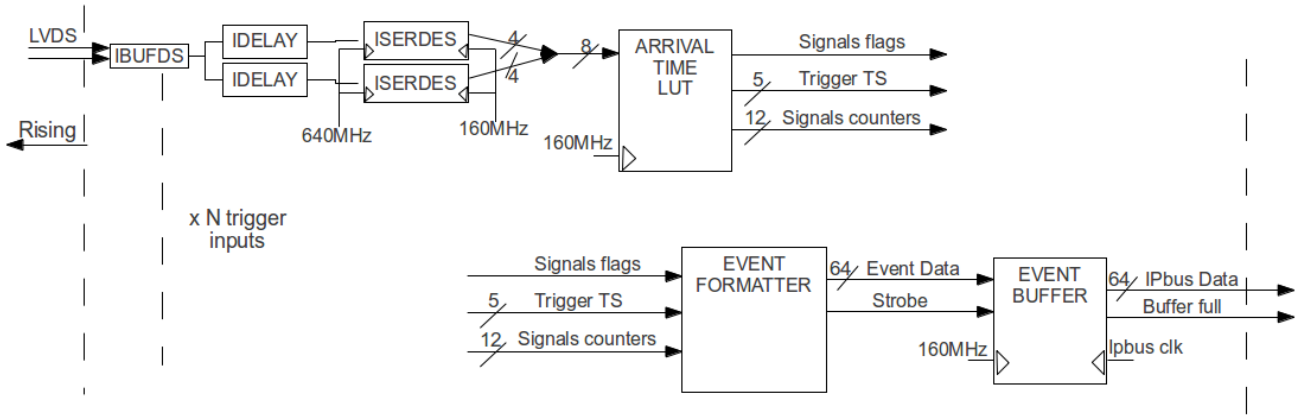
Synchronous mode (New for AIDA TLU)



$t_{cl} < 50$ MHz (Currently 5 MHz, 40 MHz)
Trigger frequency > 1 MHz sustained or $\approx$ 40 MHz instantaneously

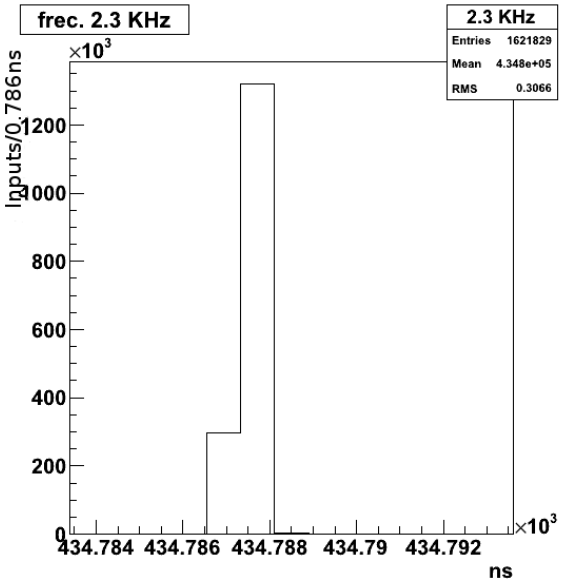
TDC

Internal scheme



Results measuring the rising edge of a periodic signal

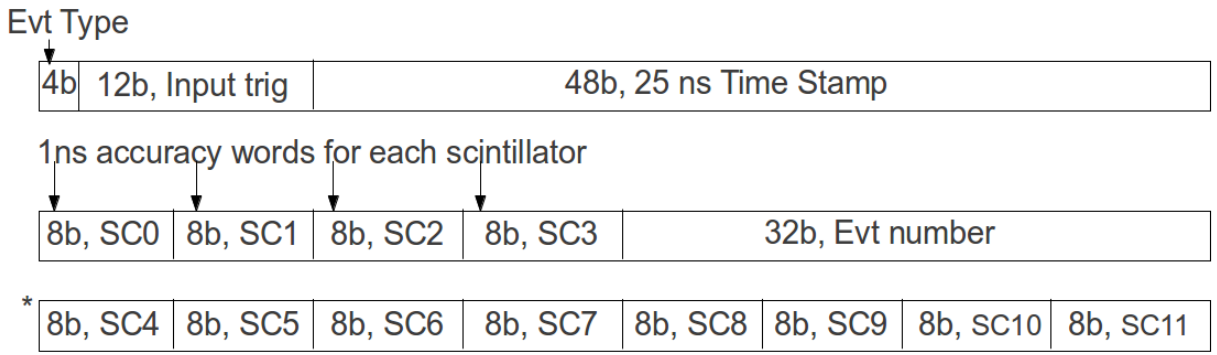
The plot represents the subtraction between the time stamp of one rising edge and the previous one.



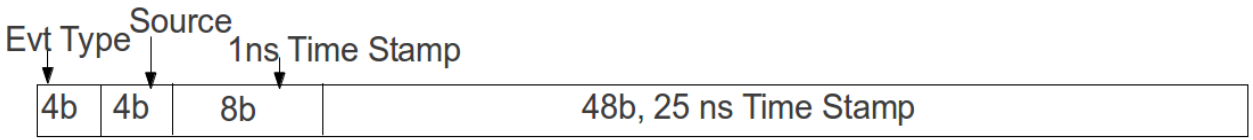
- $\sigma_{1-2} = \sqrt{\sigma_1^2 + \sigma_2^2} \Rightarrow \sigma_1 = \frac{\sigma_{1-2}}{\sqrt{2}} = \frac{0.3ns}{\sqrt{2}} \approx 0.2$ ns
- $\frac{1/(1280MHz)}{\sqrt{12}} \approx 0.2$ ns

TDC data formats

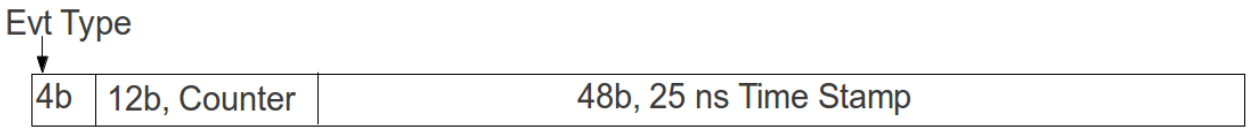
Trigger data format



Edge data format



Internal generated data format



*Only sent when at least one of the scintillators from 4 to 11 is enabled

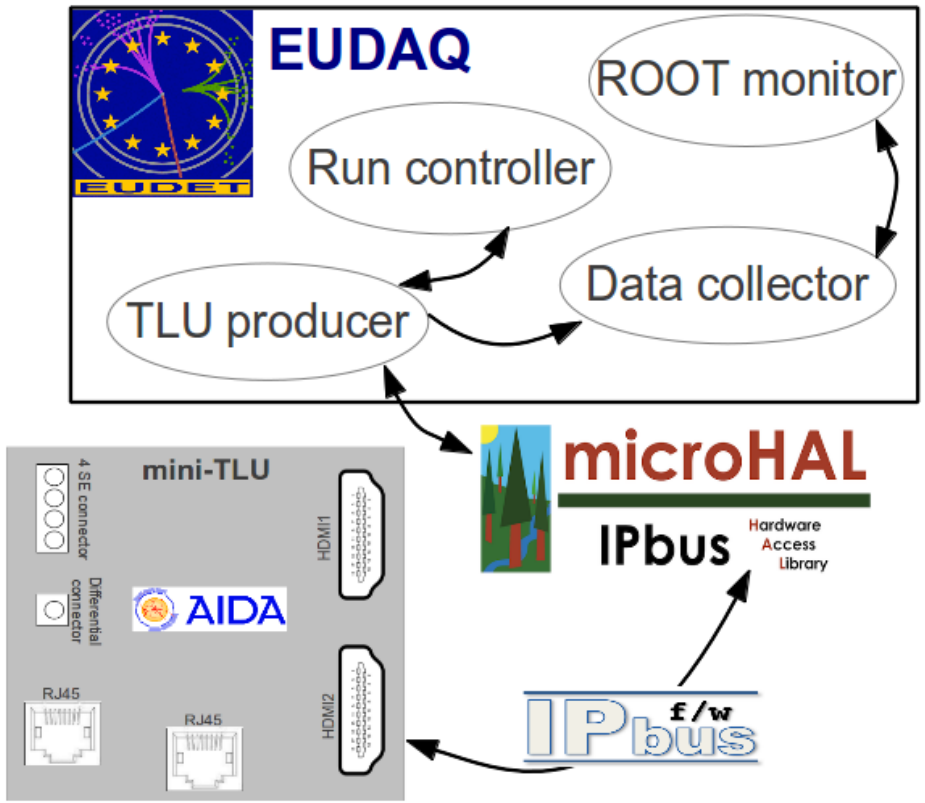
Software

EUDAQ

EUDAQ is a simple and easy to use data acquisition framework, written in C++ and originally designed to be used for the EUDET JRA1 beam telescope.

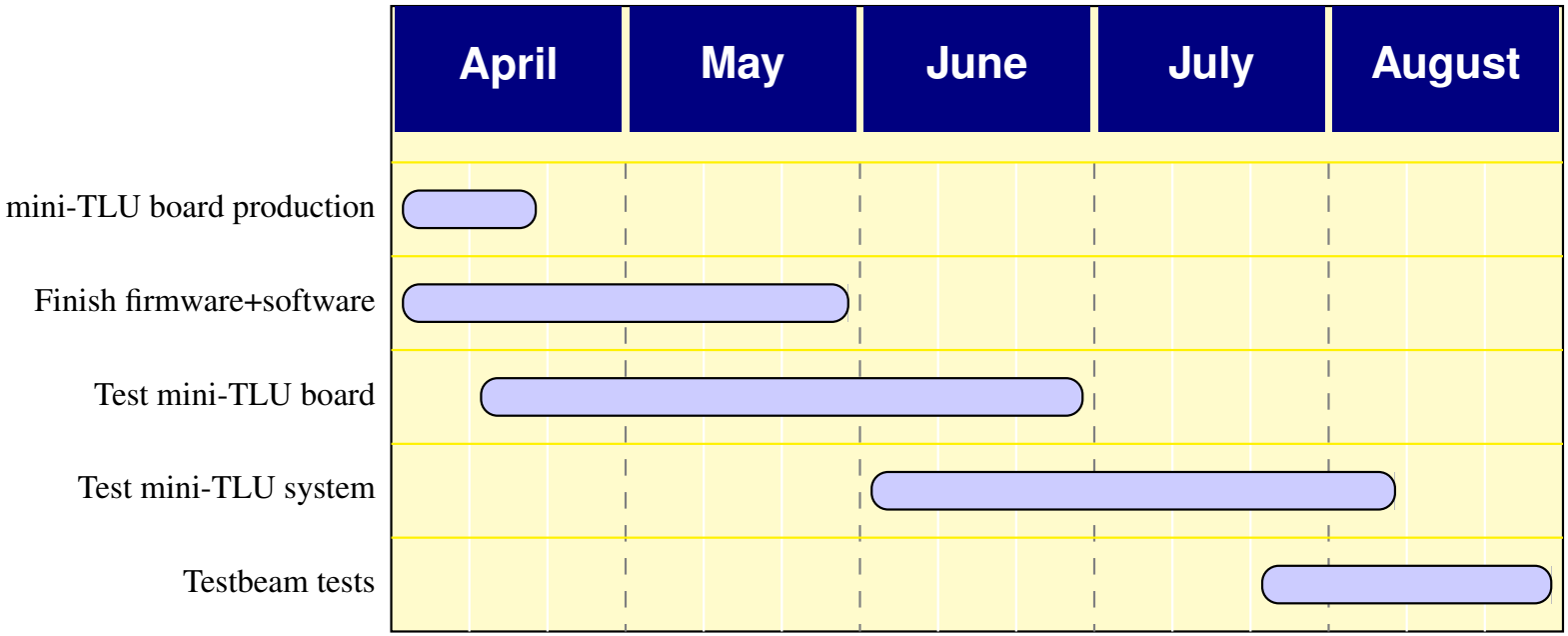
μHal

The μHAL library provides a simple and flexible way to describe the hardware registers and other memory elements. The hardware is described in XML files and it reflects also the internal hierarchy of the firmware.



See next talk: EUDAQ for AIDA - Igor Rubinskiy (Deutsches Elektronen-Synchrotron(DE)) Simon Spannagel (Deutsches Elektronen-Synchrotron(DE)) Simon Spannagel(K) Hanno Perrey (Deutsches Elektronen-Synchrotron(DE))

Next steps


April
May
June
July
August
mini-TLU board production
Finish firmware+software
Test mini-TLU board
Test mini-TLU system
Testbeam tests

Conclusions

- A prototype of the new TLU is almost done. The AIDA mini-TLU card is in production and firmware and software 90% finished.
- The AIDA mini-TLU is cheaper than JRA1 TLU.
- The AIDA mini-TLU will provide a larger trigger rate than its predecessor and will be able to handle more devices.
- The AIDA mini-TLU has a TDC accuracy better than 1 ns.
- Final tests will be held in a few months at DESY.