DAQ & control system for Si-W ECAL

or “CALICE DAQ2 as used on Si-W ECAL”

Rémi Cornat

Si-W ECAL Technical coordinator

Laboratoire Leprince-Ringuet

Ecole Polytechnique – IN2P3/CNRS

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EUDET (FP6) / CALICE DAQ2 system

- **Scalable :** Computing network architecture
- **Standard :** Giga-Ethernet
- **Compact :** "one cable for everything" Data Acquisition, Timing, Slow control
  - Backplane-less
  - HDMI : 50MHz 8b10B
  - Detector interface (DIF) could be unified among the calorimeters

Initial R&D from Univ. College London, Manchester Univ., Cambridge Univ., Royal Holloway ; continued at LLR-Ecole Polytechnique / IN2P3-CNRS

Low speed access to a chain of 10-100 very front end chips (1k-10k channels) : 1-5 Mbit/s

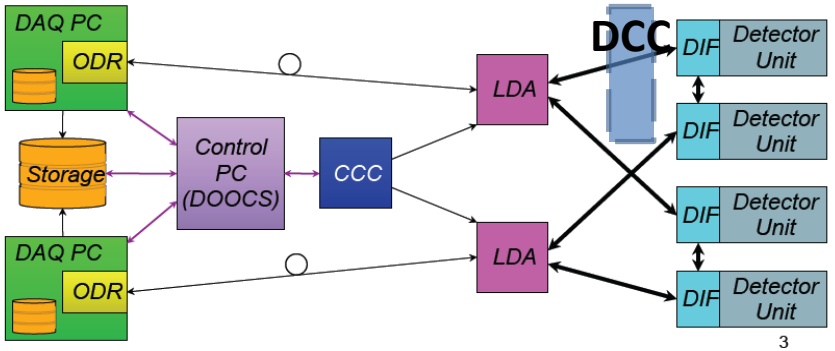
Therefore assume : auto trigger, zero suppression at VFE level

TFC interleaved with SC, DAQ using 8b/10b protocol : limited timing precision (>10 ns)

Events build at VFE level, read out during inter-spill train : limited buffering capacity (10-100 evt)

(**Detector Unit** : ASICs)
DIF : Detector InterFace connects generic DAQ and services
LDA : Link/Data Aggregator fans out/in DIFs and drives links to ODR
ODR : Off-Detector Receiver is PC interface
CCC : Clock and Control Card fans out to ODRs (or LDAs)
Control PC : Using DOOCS

Added a **DCC** : Data Concentrator Card (optional)



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Hardware

Si-W –ECAL firmware's are ~100% LLR made

CCC :

ODR : not used

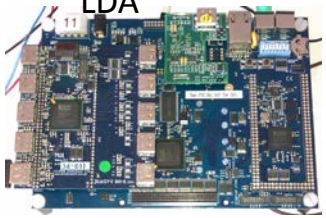
LDA : to be replaced by GDCC
- 1:10 switch
- Giga-Ethernet

DCC :
- 1:9 switch, multiplexed buffers

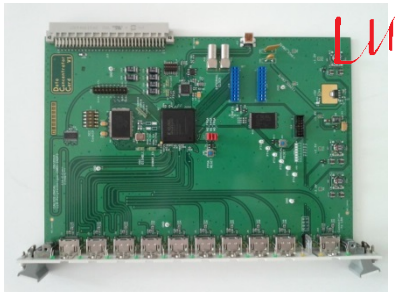
DIFs : specific to each detector

Software :

LDA



GDCC



	Si-W -ECAL SDHCAL'11	SDHCAL	Sc-ECAL AHCAL
	✓ Standard LAN switch + NIC	Sync. DCC	New HW in prep
	✓		
	(✓)	✓ Specific FW	
	✓ 8b10b HDMI	✓ USB	✓ USB
	C++ / Python	C++ / XDAQ	LabView

Software

CALICOES framework

C++ core handles Run control, DCS, Slow Control & DAQ

- Set of TCP/IP services
- Allow distributed operations, extremely modular
- Easy integration using sockets

Comes with a set of

- Python clients
- Shell scripts

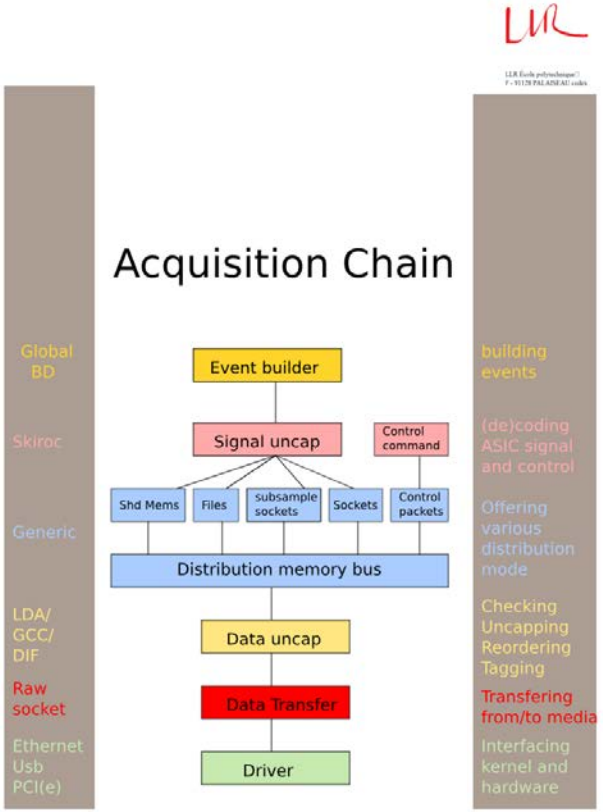
Acting as user interface at ANY level

Configured with XML files

- Parameters & configuration of physical setup
- Registration of API functions

Few detector specific modules (uncap)

Basic event builder



In use for Test beams

EUDET hardware + LLR firmware's & CALICOES framework

Used for Si-W ECAL test beams

- 1 CCC + 3 LDAs + up to 10 detector layers = DIF (12 at lab)
- If DCC were used : equivalent to 90 DIFs (=2/3 SDHCAL m^3)

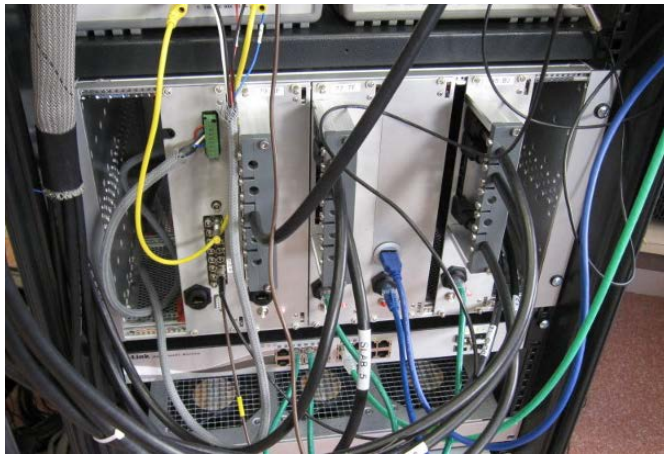
or one ILD ECAL module !

Instabilities seen

- Injured SFP cage on one LDA (fixed)
- Faulty reset system (late devel. of an arduino board)
- Packet loss (fixed in GDCC)

All boards put into mechanical modules

- Old-fashioned but cheap 19", 6U
- Better EMI, Cable handling, Connectors



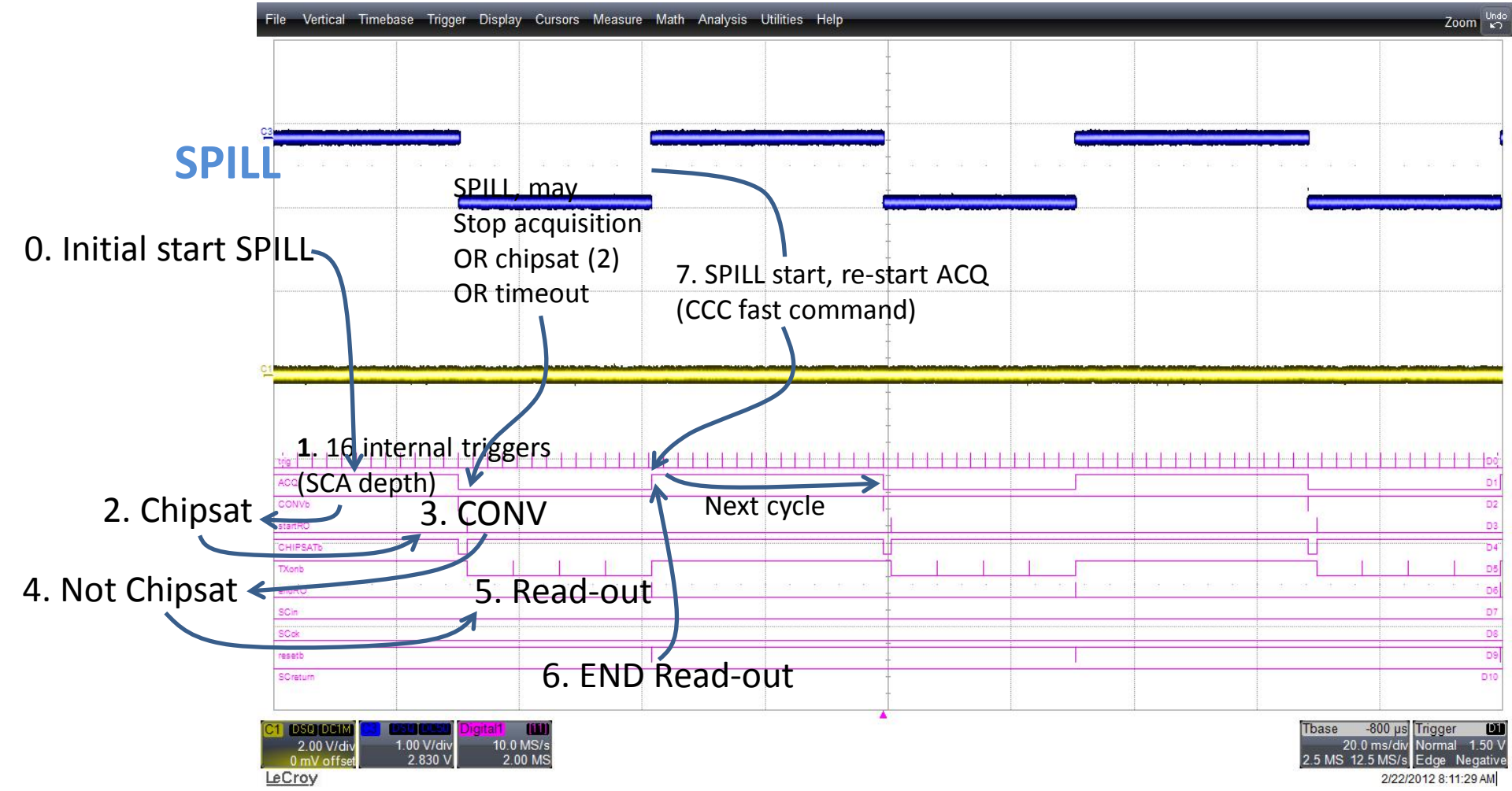
All form factors are to be redefined for larger scale integration (eg. ILC)

Backups

How it is working ?

ILC mode (normal duty cycle should be <1%, here 50%)

Requires a SPILL signal indicating a burst of bunch Xings



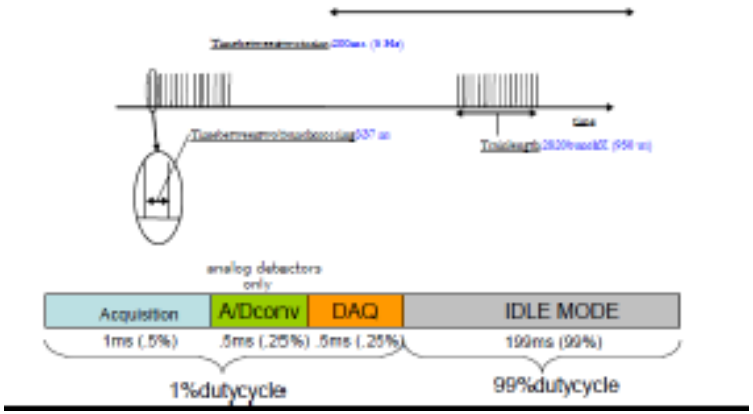
Other optional modes

- “Test beam” : first external trigger stops acquisition
- “Beam clock” : clock replaced by beam clock (~external trigger)
  - Use of external trigger path to provide a “well in phase” clock
  - For tests (will be standard mode using a machine interface “BIF”)
- “busy” : busy signal generated during read-out + end of busy automatically restart acquisition (supersedes startSPILL)

- These modes are NOT used for the ECAL (but could be…) and have originally been defined for common operations
  - Si-W ECAL chip (SKIROC2) cannot afford external trigger
  - Hardware path for BUSY in unsure

Event synchronization

- Bunch counter is reset at each SPILL start
- Increments at each slow clock
  - Slow clock is a submultiple of the system clock
  - Can be replaced by custom clock during acquisition (“beam clock” option)
- Additional SPILL ID in the data stream
  - Is reset at start of RUN
  - Increments at each SPILL start



Custom 8b10b serial link

3 twisted pairs + 2 optional :
- **reference clock** (50 - 100 MHz), fan-out from CCC
- **data in** (fast control, slow control, data)
- **data out** (slow control, data, det. Read-out)
- trigger (used for test beams if not ILC structure)
- busy (used for test beams if not ILC structure)

custom PHY layer, similar to Fast-Ethernet
- PMD : 3 LVDS pairs (clk, din, dout)
- PMA : Word size extended to 16b

same 8b/10b characters as for ethernet
- PCS : 2*(8b/10b) for data

Simple MAC layer for synchronization
- IDLE detection (carrier)
- Word clock alignment

FAST control commands sent
from a central CCC board (LEMO connector)
- Start/stop **SPILL**

From local switch
- Pause/resume **LINK**

broadcasted Control + Data characters interleaved with data flow