AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

AIDA WP3 IP block activities at AGH-UST

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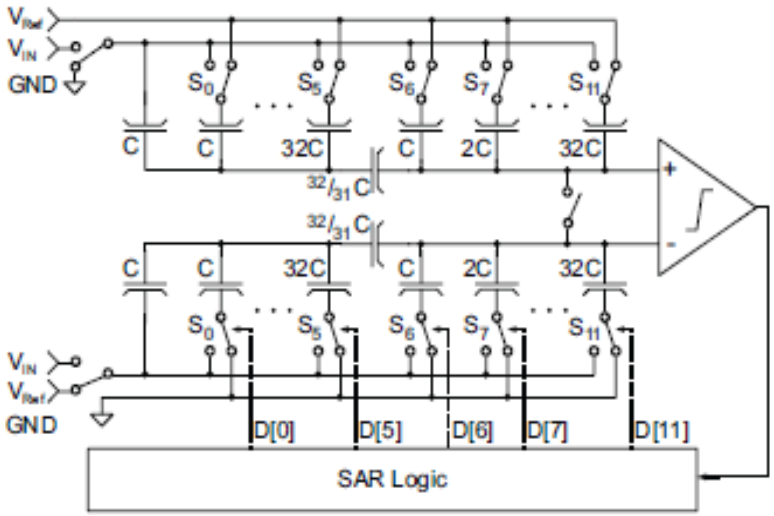
Status of 65 nm and IP block activities

- NDA for 65 nm signed
- Technology files downloaded, installation not yet finished
- At the beginning of AIDA we proposed to develop some blocks in IBM 130 nm
  - Fast (>40 MSps) SAR ADC (6 or 10 bits)
  - Variable frequency PLL
  - SLVS interface
- All these blocks were designed in IBM 130 nm and 1st prototypes were produced
- Tests are ongoing...
- We hope to move one/two blocks to 65 nm

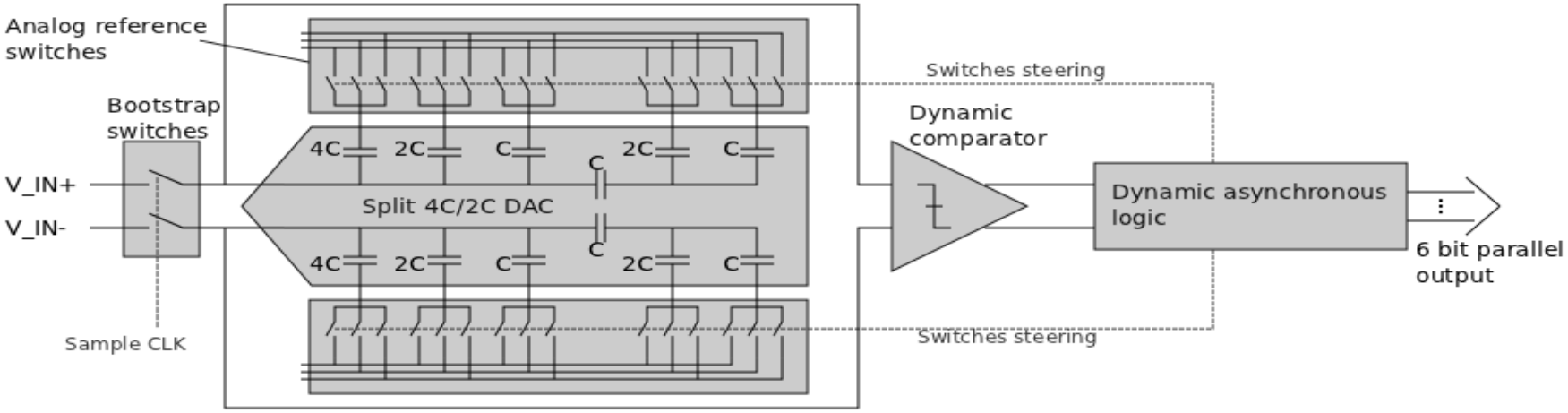
Development of 10-bit ADC in IBM 130 nm



Designs specs:

- 10-bit SAR ADC
- Architecture: SAR ADC with segmented/split DAC
- Asynchronous SAR logic – Only sampling clk, No fast bit clk
- Scalable frequency (up to ~50 MS/s) and power consumption
- 1-2mW at 40MS/s
- ~150um pitch
- ***Submitted and fabricated in 2012, presently under test…***

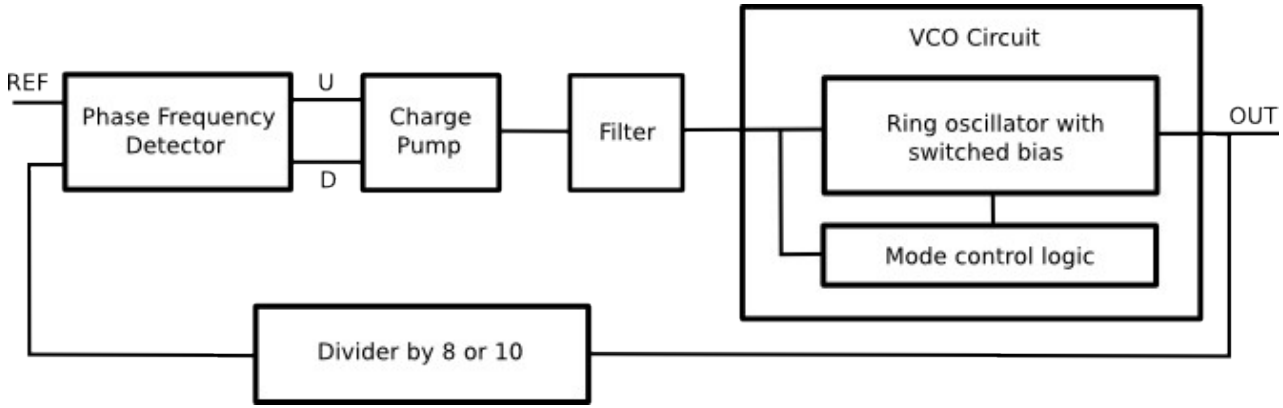
6-bit SAR ADC



Design specs:

- 6 bit resolution, simulated ENOB > 5.8 bits
- Architecture and blocks similar as 10-bit design
- Maximum sampling rate > 80 MS/s
- Channel pitch = 40um
- Power consumption ~ 0.3 mW per channel @40 MS/s
- ***Submitted and fabricated in 2012, PCB test board in production, tests should start ~ May 2013***

Design of PLL for data serialization in IBM 130nm



Two prototypes submitted and fabricated in 2012:

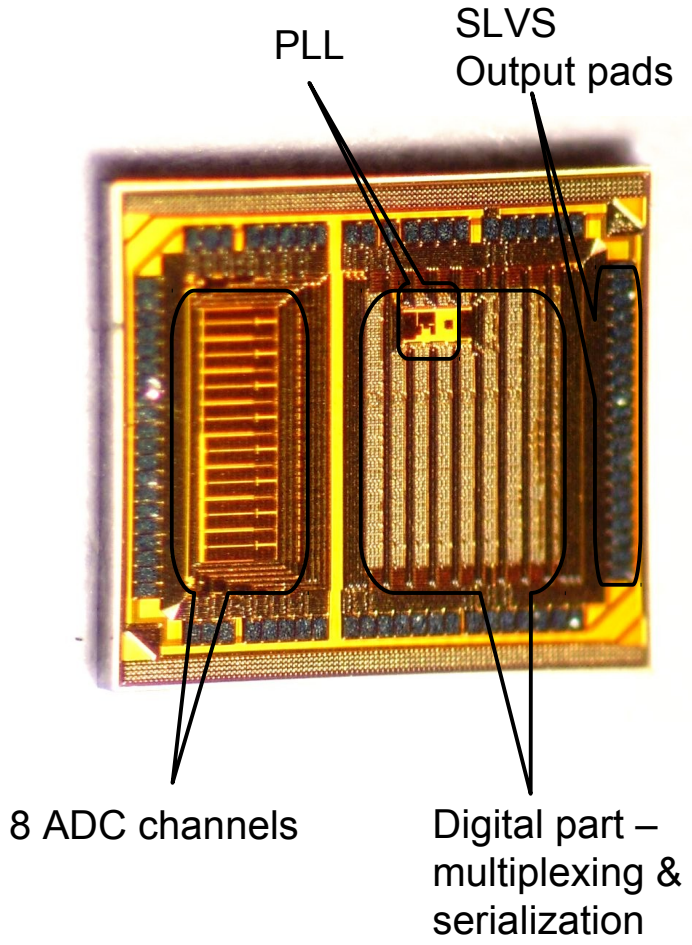
- Architecture: type II PLL with 2nd order filter
- Scalable frequency&power
- Automatically switched VCO freq. range
- VCO frequency range 60MHz – 520MHz,
- VCO frequency division by 8 or 10
- Power consumption <0.5mW at 500MHz
- Area 200um x 160um

- Architecture: type II PLL with 2nd order filter
- Scalable frequency&power
- Automatically switched VCO freq. range
- VCO frequency range 8MHz – 3GHz,
- VCO frequency division by 6, 8, 10 or 16
- Power consumption <2mW at 3GHz
- Area 300um x 300um

First prototypes in IBM 130 nm under test 10-bit ADC, PLL, SLVS

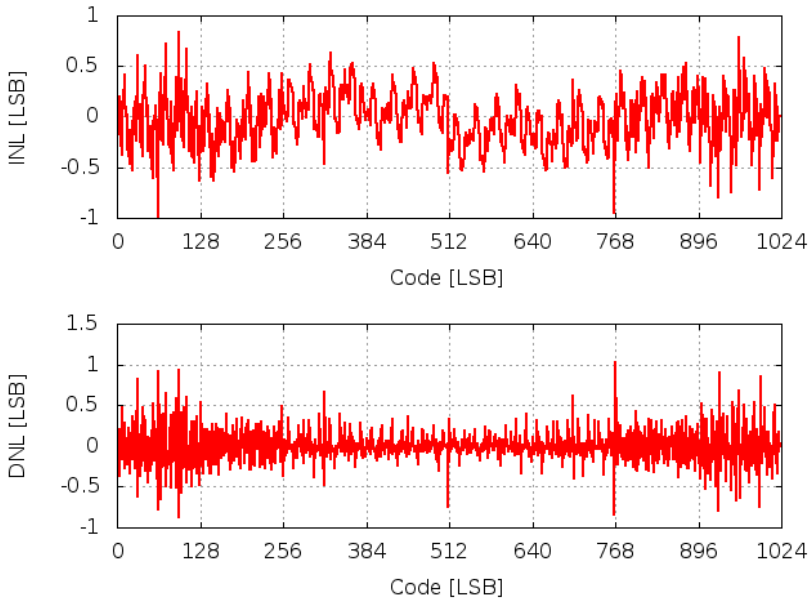
Prototype ASIC contains:

- 10-bit SAR ADC
- PLL
  - Tests are just starting. By now first measurements of PLL were done and high frequency clk signal generated at its output was observed.
- SLVS interface
  - No dedicated tests of SLVS interface were done, but looking at ADC and PLL differential outputs it was veryfied that SLVS driver operates at least up to 700 MHz

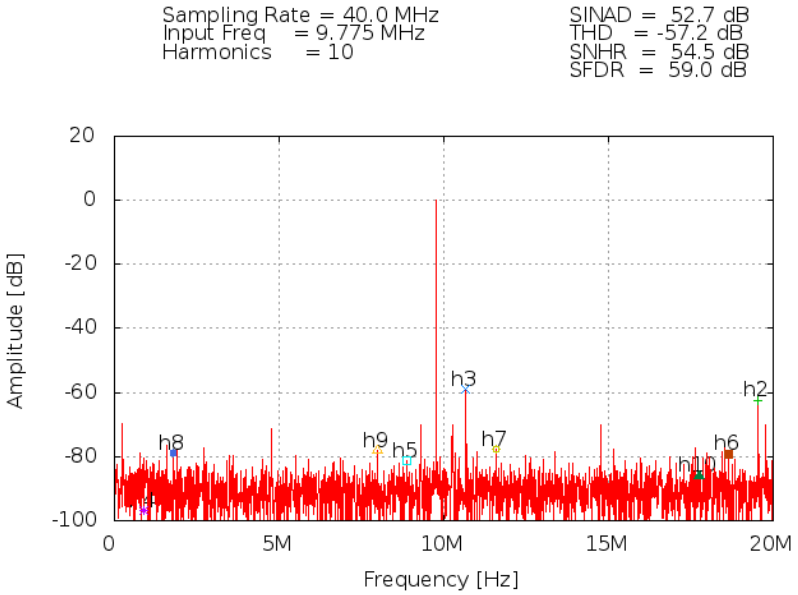


Preliminary measurements of 10-bit ADC
Example measurements at 40Ms/S

Static measurements



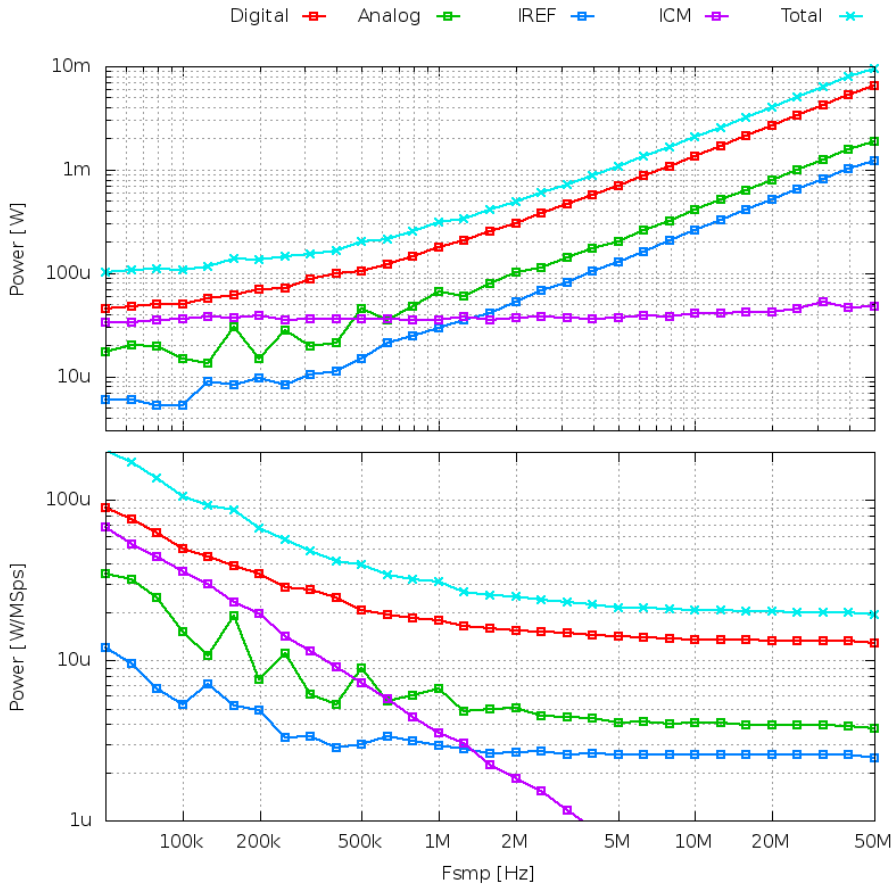
Dynamic measurements



- First conclusion is that ADC works in the whole simulated frequency range, at least up to 50MHz
- Quantitive results will be probably worse than simulated (ENOB 8-9 bits ?)
- Tests are in progress...

Preliminary measurements of 10-bit ADC
Power consumption vs sampling frequency

- Power measured for 8 ADC channels
- At 40Ms/S the consumption is about 1 mW per channel – in agreement with simulations



Summary and Plans

- We are almost ready to start design in 65 nm
- First prototypes of 10-bit SAR ADC, 6-bit SAR ADC, PLLs, SLVS already designed and produced in IBM 130 nm, and presently under test:
  - 10-bit SAR ADC: first results show its functionality, the effective resolution seems to be less than simulated - quantitative measurements are still progoress
  - PLL tests are just starting
  - SLVS interface works well at least up to 700 MHz
- Depending on test progress and results we plan next submission in IBM 130 nm at the turn of 2013/2014
- It is difficult to estimate the submission in 65 nm...