THE MEDIPIX3 TSV PROJECT

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CERN
Geneva, Switzerland

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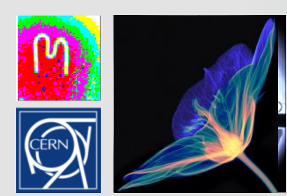


Outline

Summary of project plans

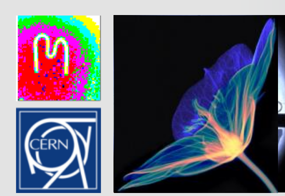
Medipix3 – designed for TSVs

LETI process reminder

Status of project

Some key numbers for the LETI process

Future plans



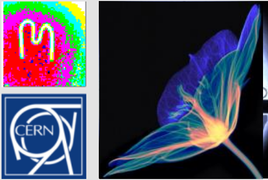
Project Outline

- Phase 1: TSV processing of Medipix3 wafers
  - Process 10 wafers in CEA LETI
  - Separated in 3 lots in order to improve the process step by step
  - Third lot gave good preliminary results!

- Phase 2: Hybridization of the TSV processed chips
  - Chip pick up and selection of KGD
  - Preparation of sensors
  - Flip chip to KGD
  - Test of single assemblies

Phase 3: Demonstrator Module
  - Mount single chip assembly on appropriate support cards
  - Demonstrate multichip module operations

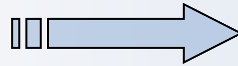
* LETI contract supported at the level of 14% by AIDA
Other partners: Alice, LCD, Medipix3 Collaboration

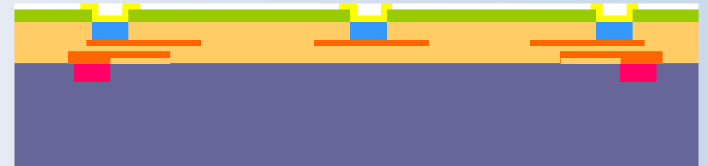


Reminder of LETI Process

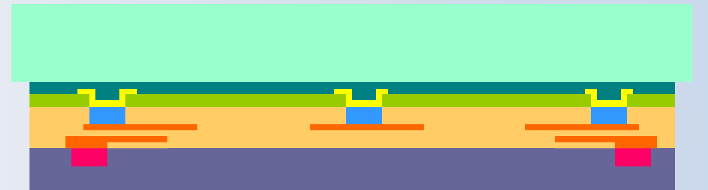
- **Front Side UBM**

UBM
- TiNiAu Deposition
- Litho UBM
- UBM etch



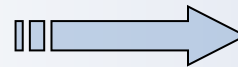


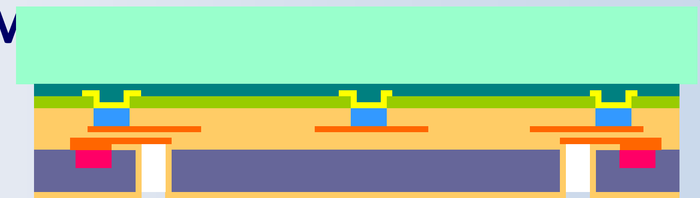
- **Bonding / Thinning**
  - Bonding
  - Grinding/edge dicing
  - CMP Si



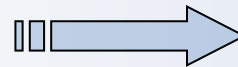
- **Back Side: TSV Last + RDL + Passivation + UBM**

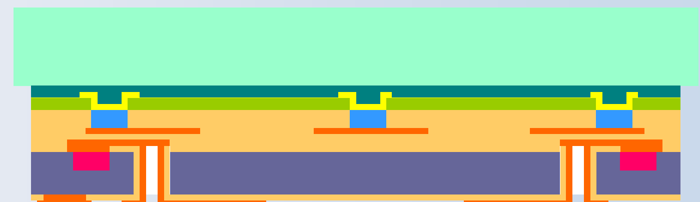
TSV
- Litho TSV
- TSV AR2 etch
- SiON conf deposition
- Etch back



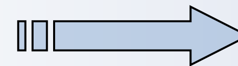


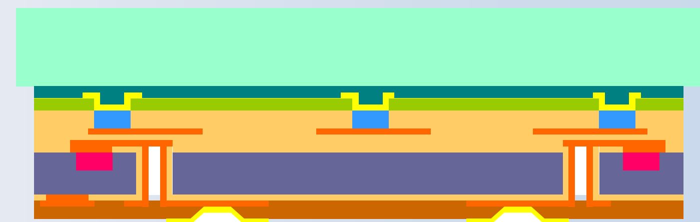
RDL
- SEED TiCu
- Litho RDL
- ECD Cu
- Litho PASSIV

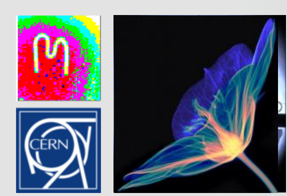




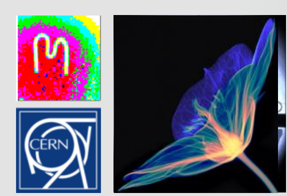
UBM
- TiNiAu deposition
- Litho UBM
- UBM etch
- Debonding / Dicing



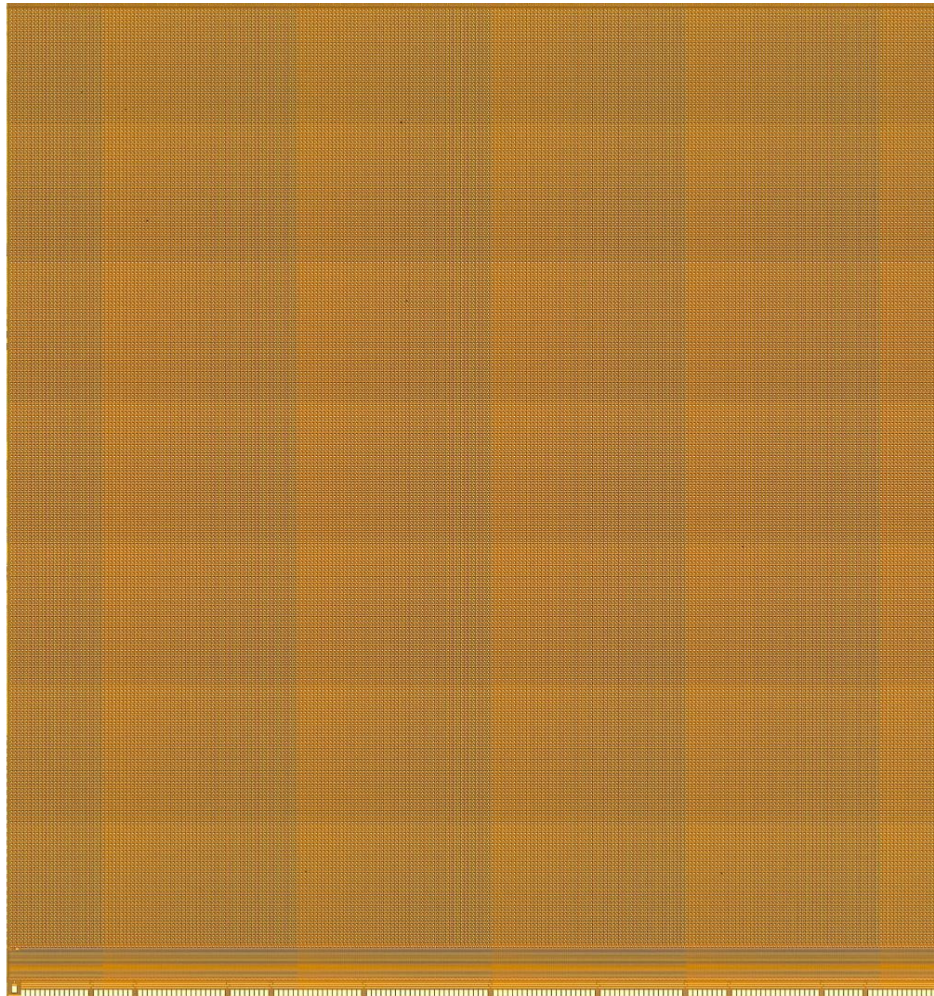




Medipix3 chip photo



Medipix3 ready for Through Silicon Vias



All IO logic and pads contained within one strip of 800μm width

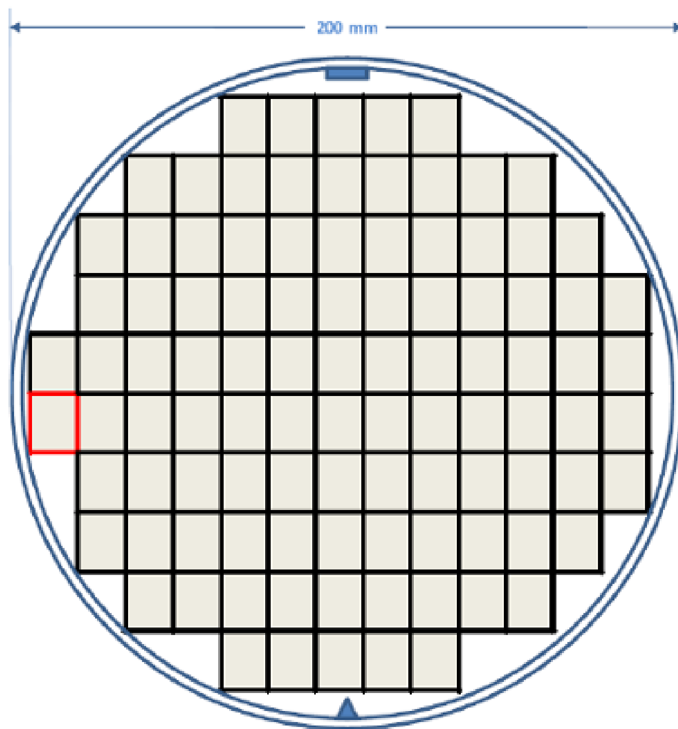
All IO´s have TSV landing pads in place

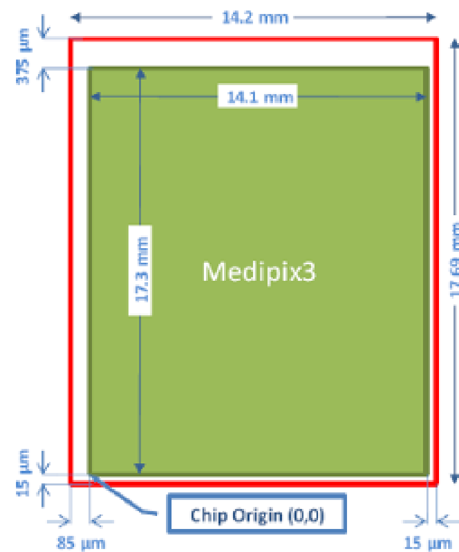
Permits 4-side butting

94% sensitive area

Wafer Layout

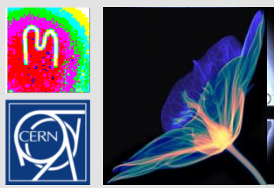
- **Approximatively 100 chips per wafer**



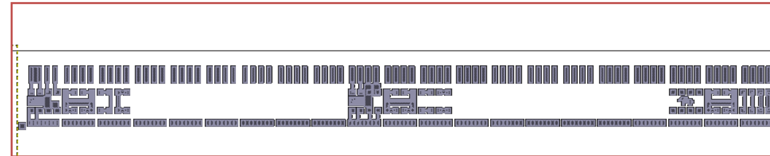


Chip frame's outer size (metal ring) is 14099.600 um in X and 17299.6 um in Y.

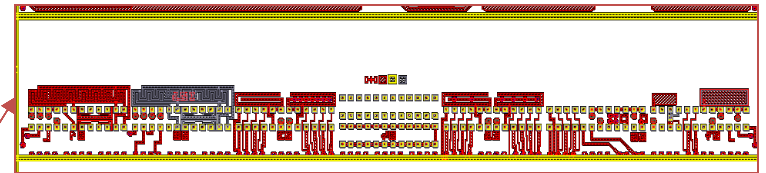
The red frame indicates the reticle size (chip + dicing lane)



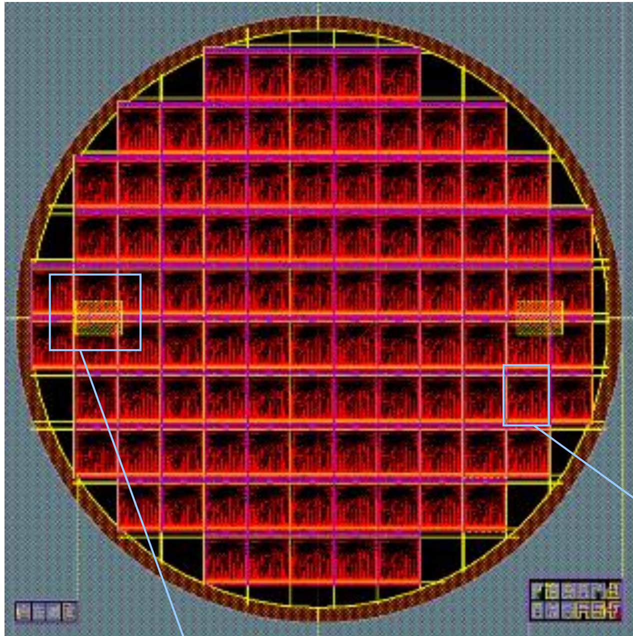
RDL design (Timo Tick)

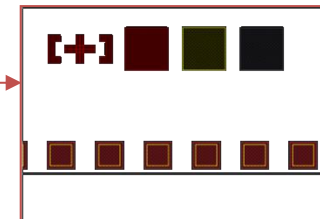


Front side Electrical tests area



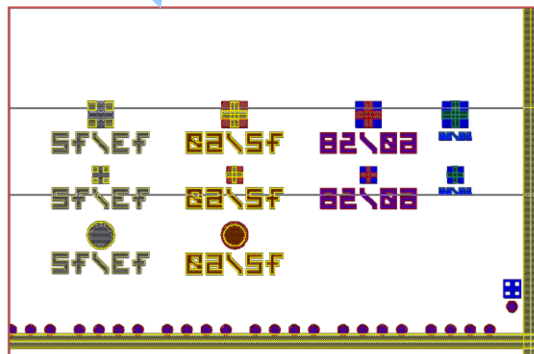
Back side Electrical tests area



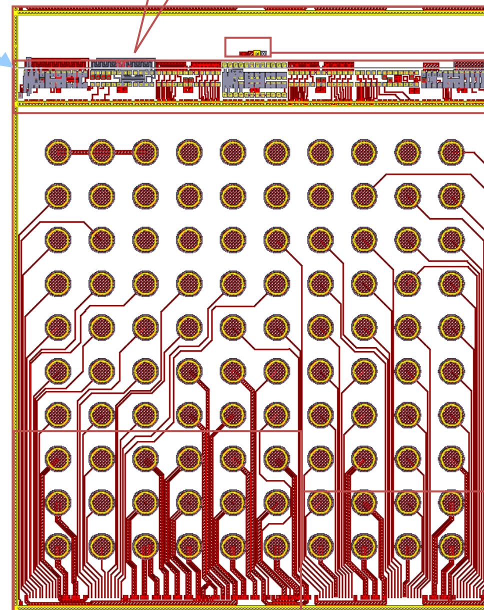


Metrology boxes

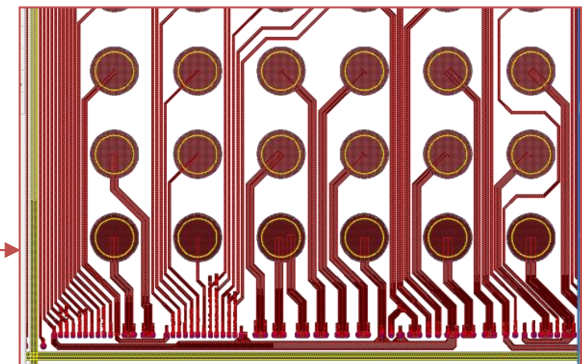
Complete map



Alignment Marks



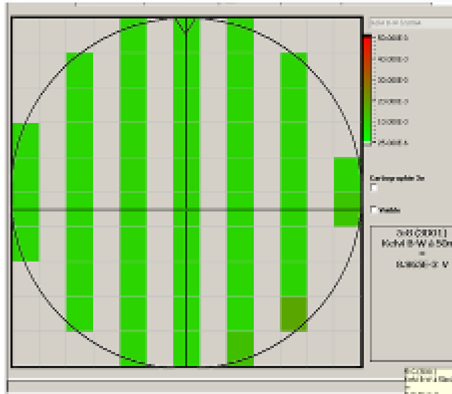
Active chip



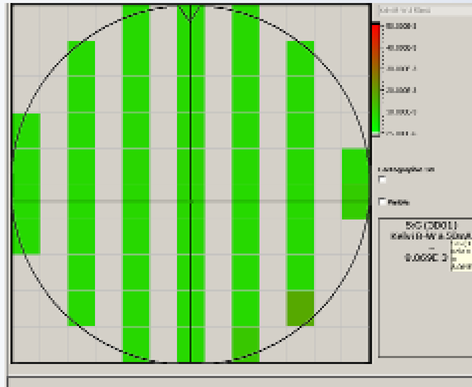
RDL details

Medipix 3 project results / electrical tests (non exhaustive)

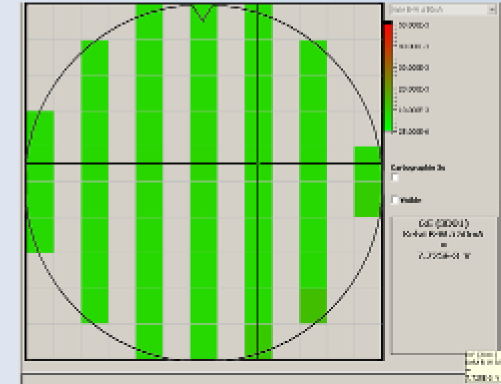
- **UBM/ Al contact resistance**



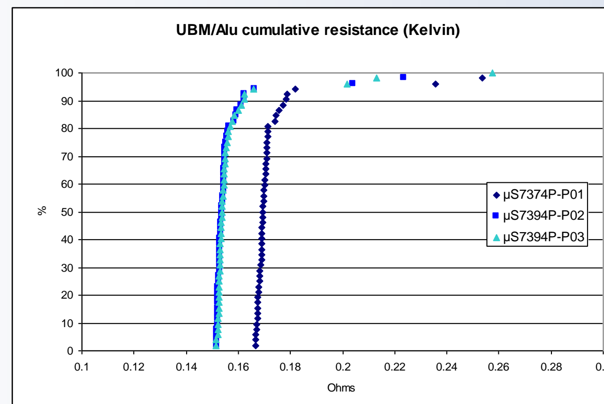
P01



P02



P03



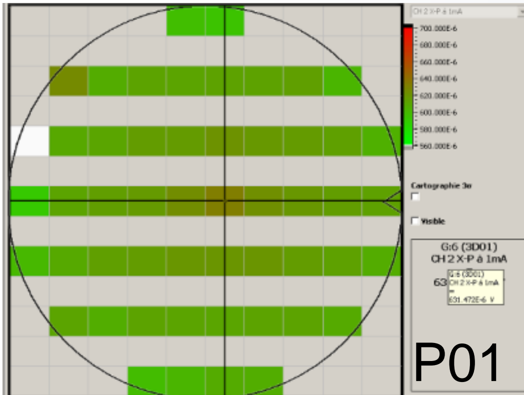
Cumulative resistance UBM/Alu
Mean value : ~ 150 mohms

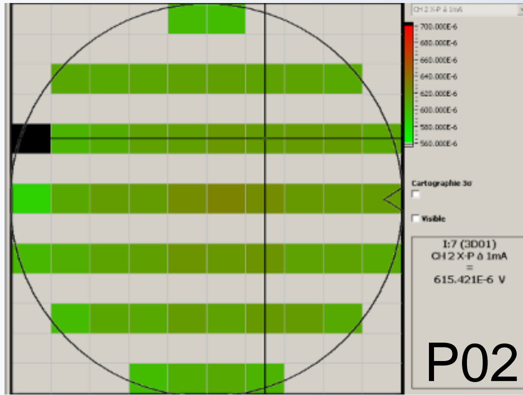
- **Conclusions:**
  - ☺ Isolation between UBM lines OK
  - ☺ Alu/UBM contact resistance is OK

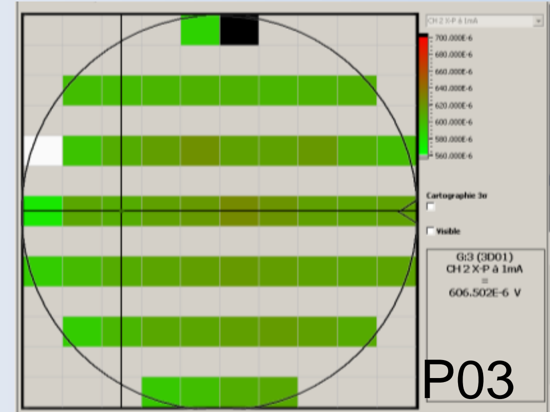
Medipix 3 project results / electrical tests (non exhaustive)

- **2 TSV chain resistance (by Vdd)**

1.23 Ω ± 3.6 % (1σ)

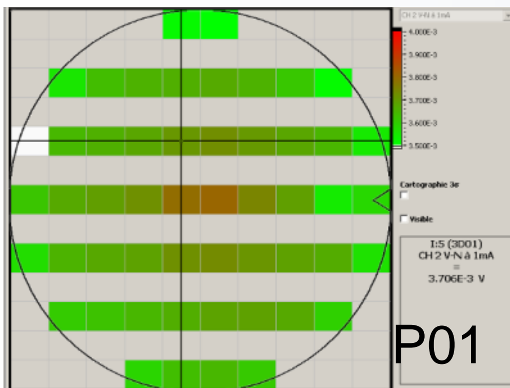


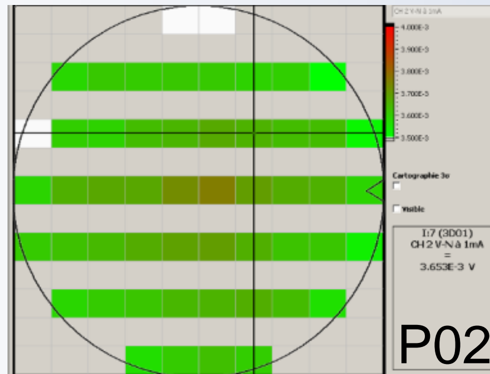


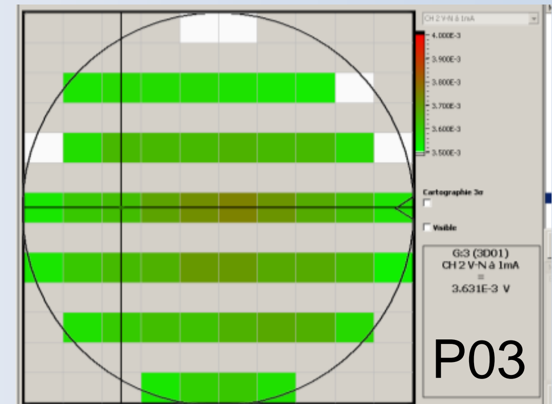


- **2 TSV chain resistance (by Vss)**

3.60 Ω ± 1.9 % (1σ)



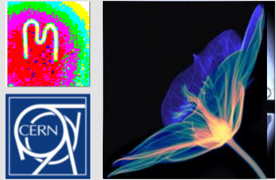




D. Henry, LETI

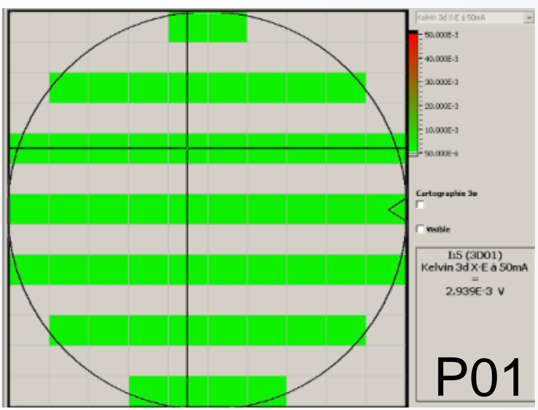
- **Conclusions:**

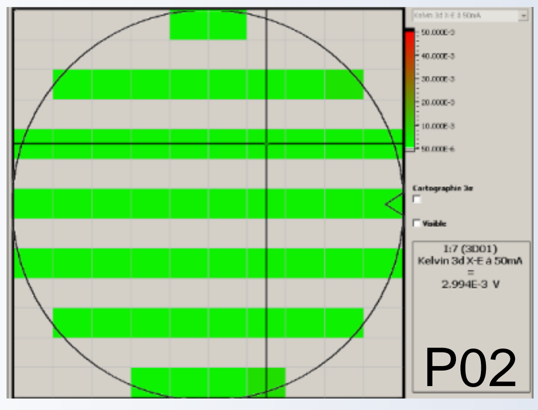
☺ Uniform distribution of values ➔ no comparizon with reference value possible

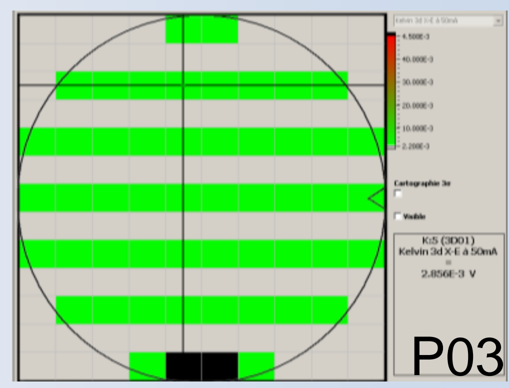


Medipix 3 project results / electrical tests (non exhaustive)

- **Kelvin TSV ➔ Mean value** **50 mΩ ± 14 % (1σ)**



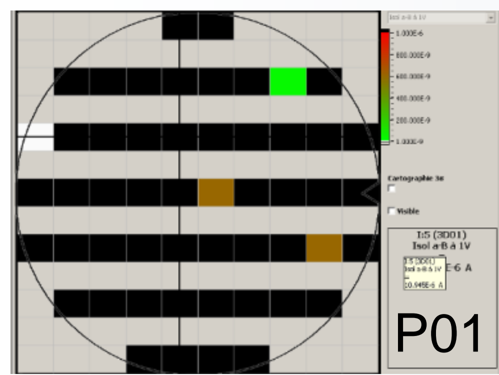


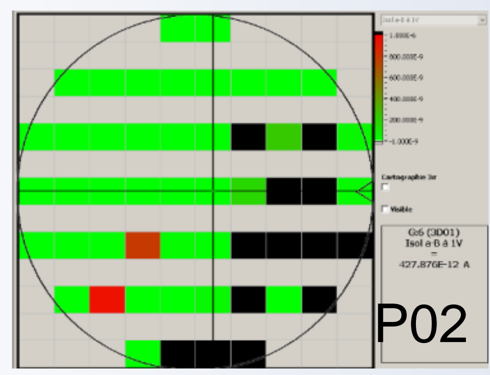


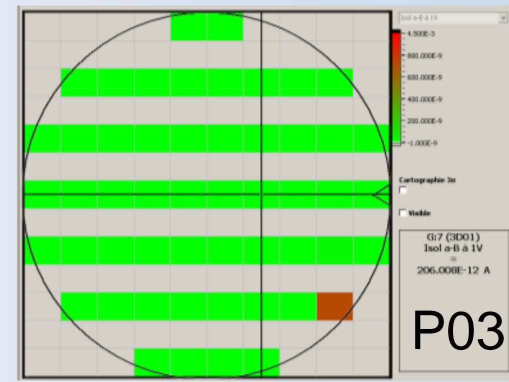
Kelvin3D (Specs < 1 Ohm/TSV) / Yield: 100%

Kelvin3D (Specs < 1 Ohm/TSV) / Yield: 96%

- **Insulation between 2 TSV (1 connected TSV to M1 & 1 non connected) – Applied voltage : 1V**







- **Conclusions:**

  Insulation issue on P01 & P02 / Root cause identified

  Correction on P03

I_{leak} < 1 E^{-06}A

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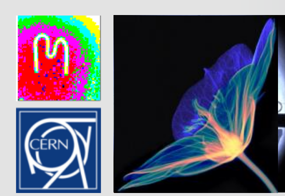
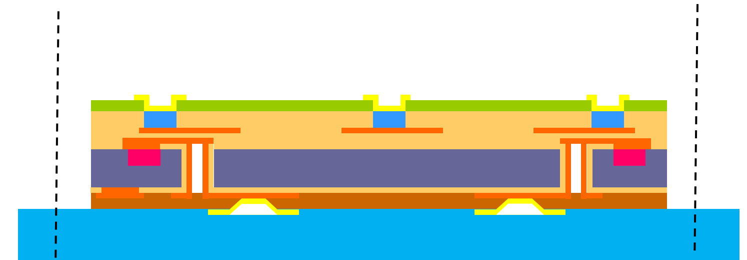
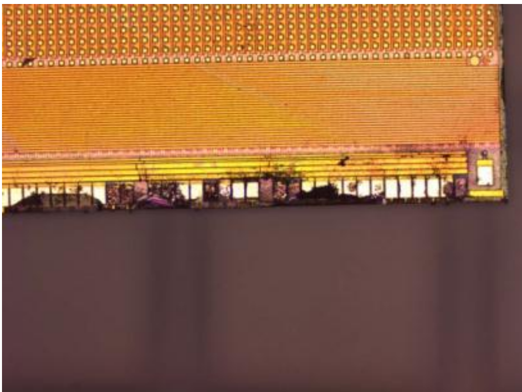


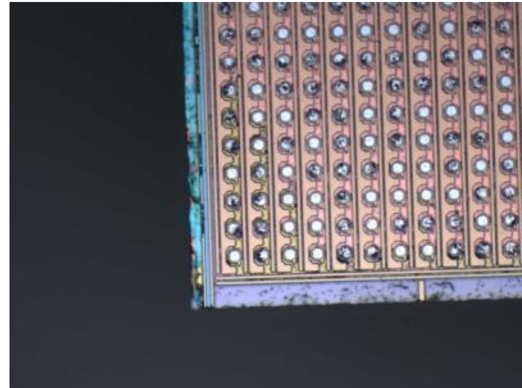
Dicing/chip pickup issues

- **Chips Dicing & boxes packaging**
  - First delivered wafers :
    - Metal delaminations on front side
    - High chipping on the edges
    - Chips breaking during pick out process
    - Tape residues on pixel side

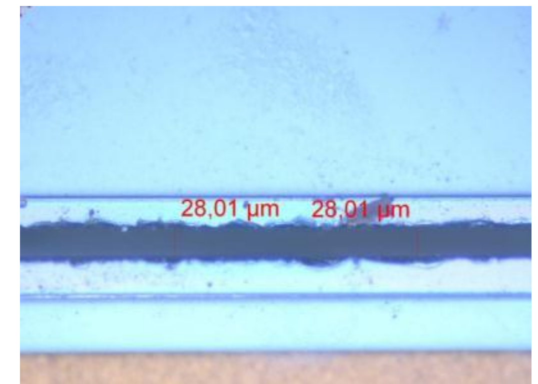




High chipping + pad delamination

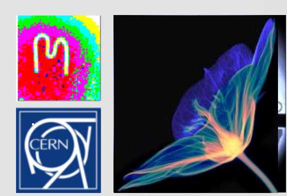


Tape residues



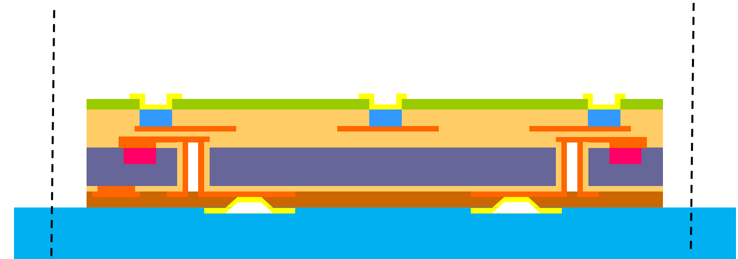
Backside chipping

- **Need to develop an optimized dicing process :**
  - DISCO collaboration

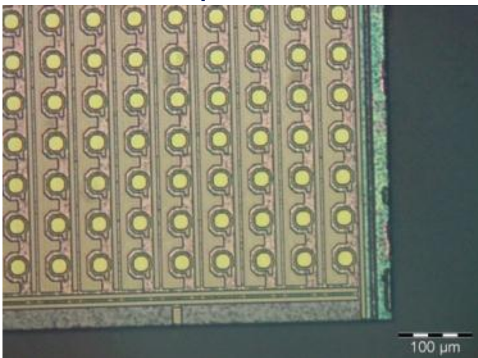


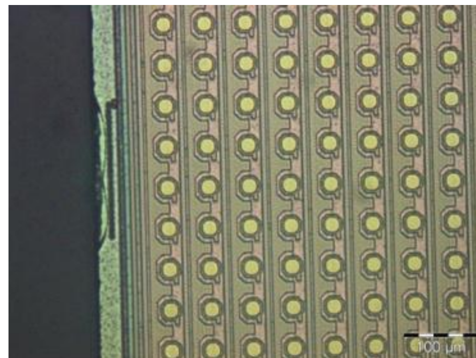
Dicing/chip pickup issues

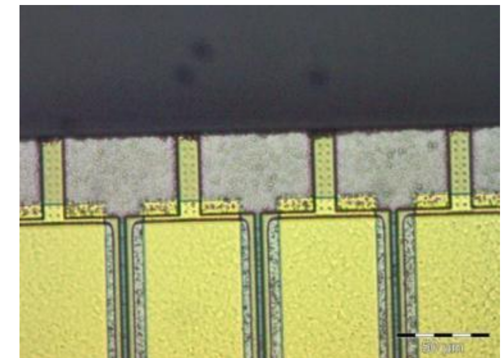
- **Dicing trials on DISCO plant (Munchen)**
  - Taping of BGA side on the tape
  - UV tape
  - Fine blade
  - High Blade rotation
  - Low Blade speed



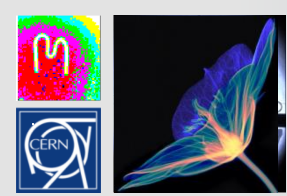
- **Pixel side observations**
  - Chip I4





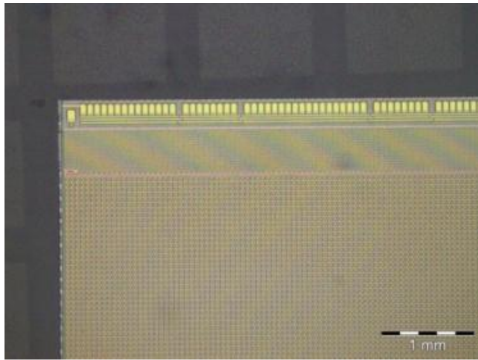


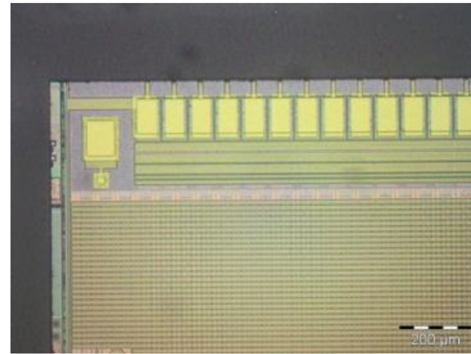
- Lower chipping compare to previous dicing
- Every defects localized on dicing streets

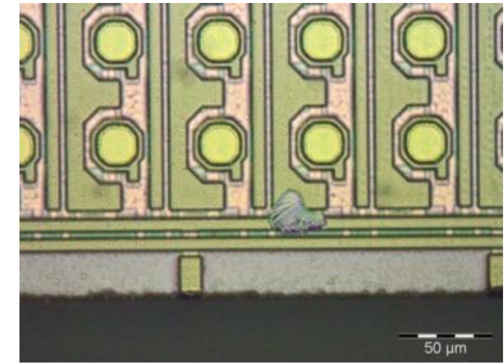


Dicing/chip pickup issues

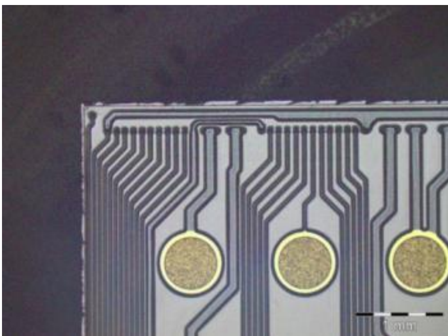
- **Pixel side observations**
  - Chip I4

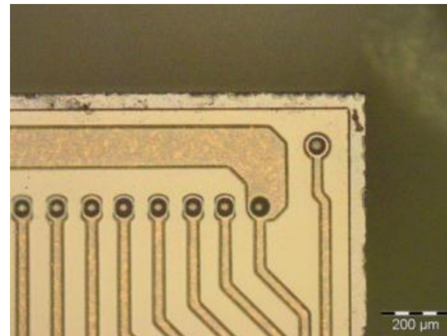


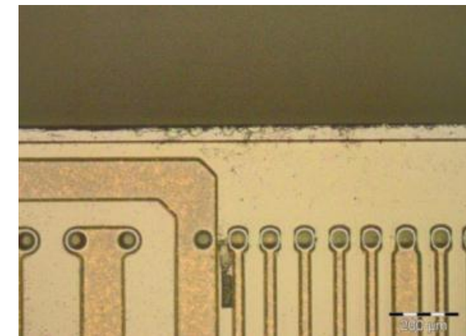




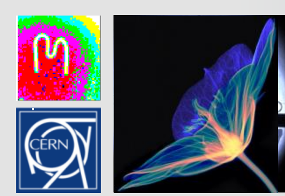
- **BGA side observations**





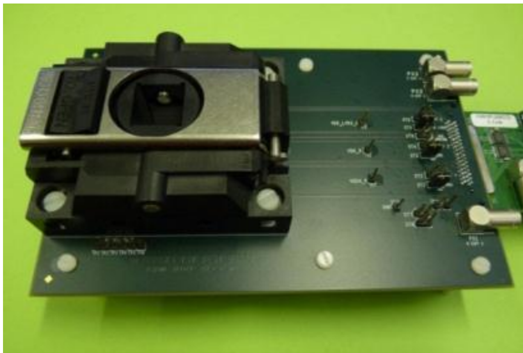


  - Higher chipping than on the pixel side ➔ contact with tape
  - All defects localized on the dicing streets ➔ polymer seal ring effect

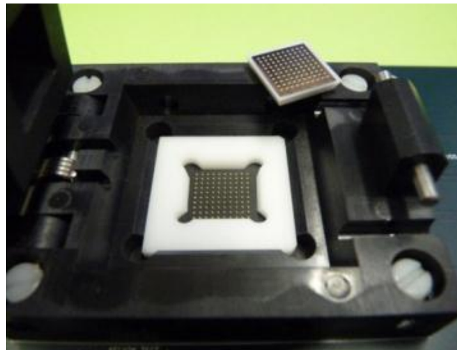


Test setup at CERN

- Test set-up :
  - Test board realize the interface between Medipix3 chip and readout interface
  - Test socket is embedded on test board to establish contact to the bga pads of the chip
  - We are using a custom readout interface (USB) common to most of MEDIPIX chip family



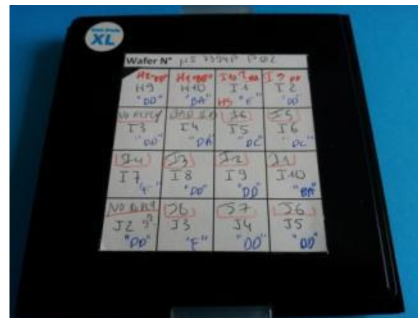
Test board

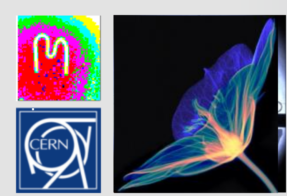


Test socket

Readout interface

- Test samples
  - LETI sent a complete GELPAK of 16 diced chips. (DISCO dicing)
  - Parts are from IBM wafer # AZNW5VH, at CERN it was identified as Wafer # 24





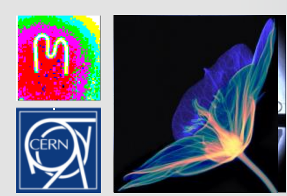
DAC scans (normal for Medipix3)

Threshold_0

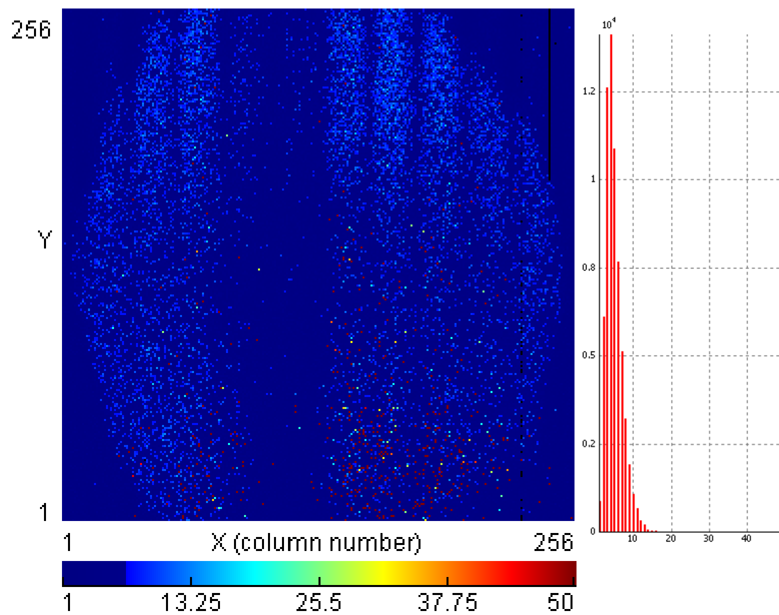
FBK

CAS

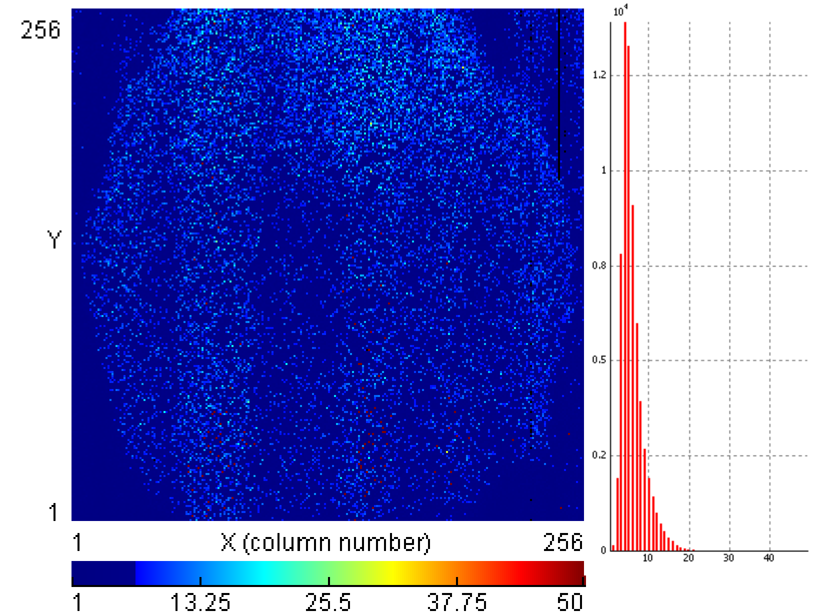
Chip H2 behaves as expected, only a small drift with DAC CAS is noticeable.



Noise floor comparison

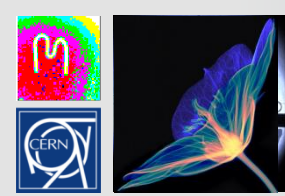


Before TSV



After TSV

- We could notice only a slight difference



CEA-LETI TSV process - key numbers

- AR (wafer thickness to TSV diameter) max 3:1

- Minimum TSV pitch 80um
- Minimum TSV diameter 40um

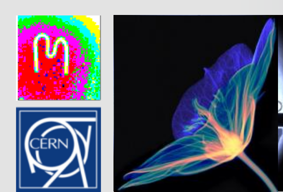
- RDL min track width 20um
- RDL min track space 40um
- RDL thickness range 2um to 12um Cu

- Front side UBM min space 30um
- Front side UBM min width 20um
  (For ref MPIX3 25um diameter on 55um pitch)

- Back side UBM min space 30um
- Back side UBM min width 20um

- TSV typical resistance 50mohm (60um on 120um thickness)
- TSV typical isolation >= 1Gohm

- Resistance UBM to Al pad 150mohm for 25um diameter.



Project status and future work

AIDA project

- First 2 assemblies have been received (VTT/Advacam)
- More to follow soon (need to bump sensors)
- Test card ready
- Low melting point BGA spheres ordered

Future work (Medipix3 Collaboration/LCD)

- Process a further 6 Medipix3RX wafers at CEA
- Cover large area
- Smallpix edgeless chip design