65nm CMOS activities at LAL/LAPP

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LAL/LAPP 65 nm projects

IP blocks for WP3.3

LAL -> Pixel (LAL/LPNHE)
-> OTA (Analog low noise Front-end)
-> PLLs

LAPP -> LAL Omegapix
-> DAC 12b 80 MHz -> 14b
-> Clusters centroid evaluation

Pixels readout

Two options:

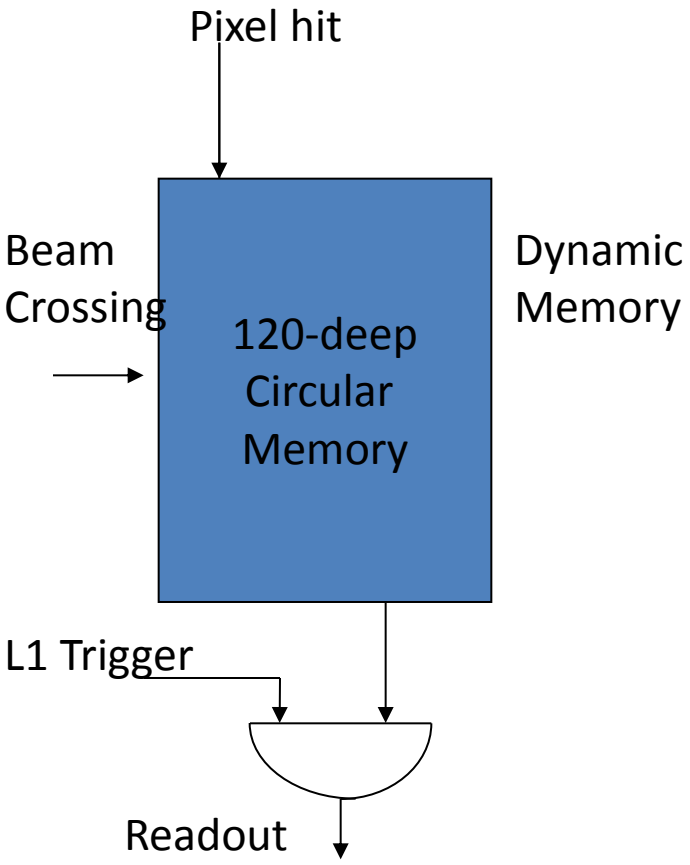
-1 In-pixel circular buffer

-2 Use in-pixel storage (FIFOs) instead of circular buffer to reduce power and Silicon area

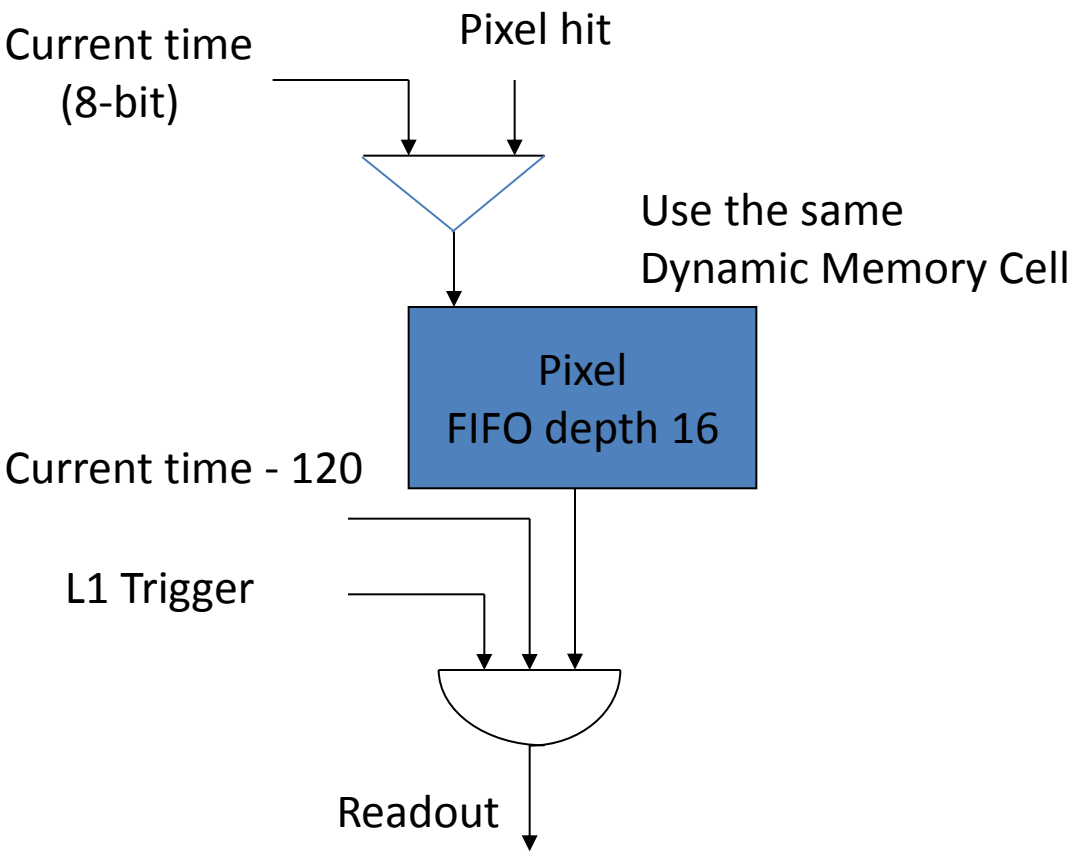
- Hit times are recorded for the L1 latency
- At L1, hit times in FIFOs are compared to the current time and selected for L2 if hit time matches L1 time

Pixels readout: on-pixel Circular buffer vs on-pixel FIFOs

Circular buffer scheme

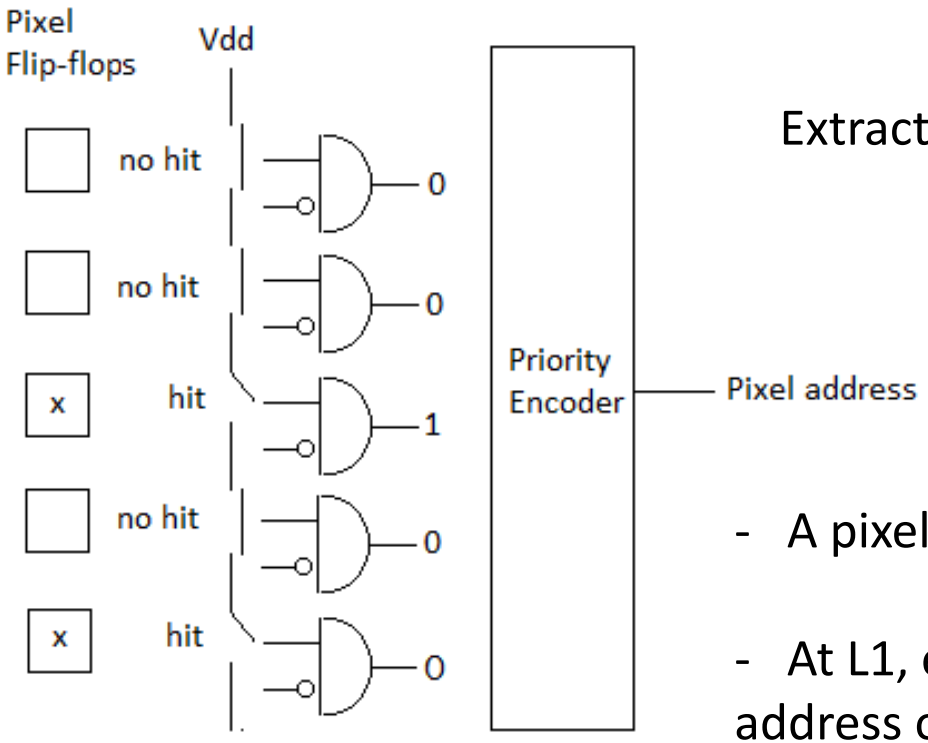


Selective readout scheme



Selective readout scheme: Save silicon area and power at the pixel level

Timing based pixels sparse scan readout



Extract a stack of addresses of pixels hit in time with L1

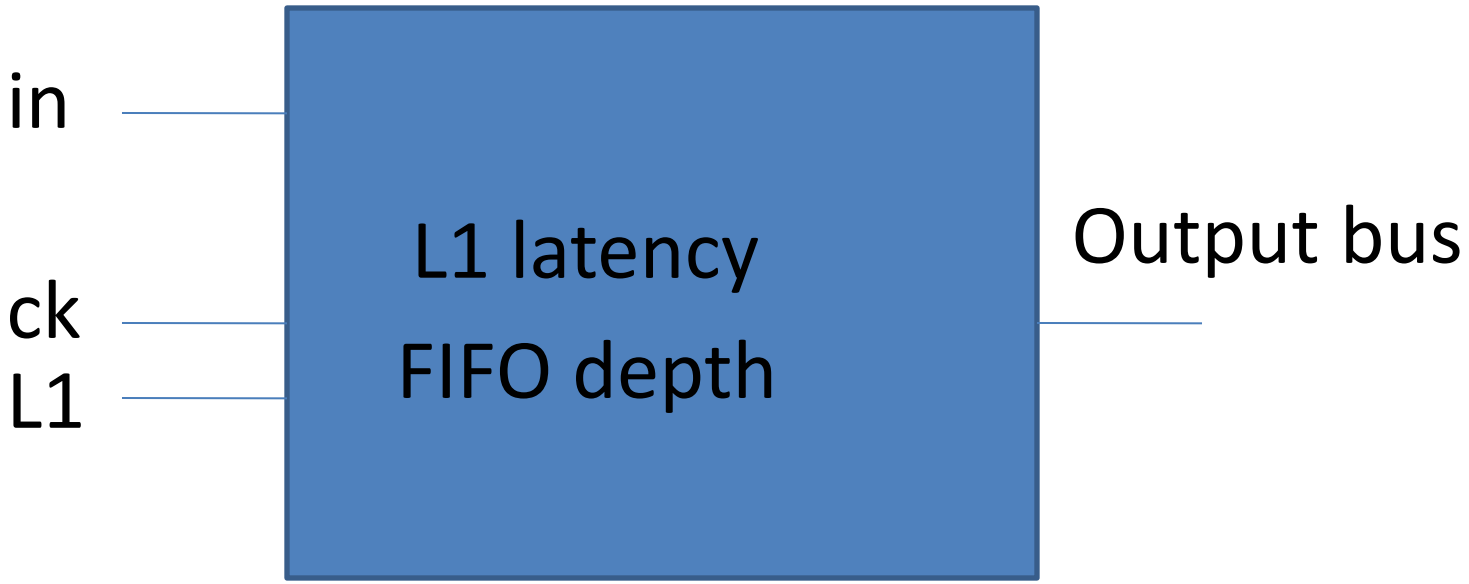
- A pixel switch is **open** on a hit

- At L1, each read clock cycle outputs the address of a pixel with a hit time matching this L1, from colum top to bottom

Scan all columns in parallel to end of column FIFOs

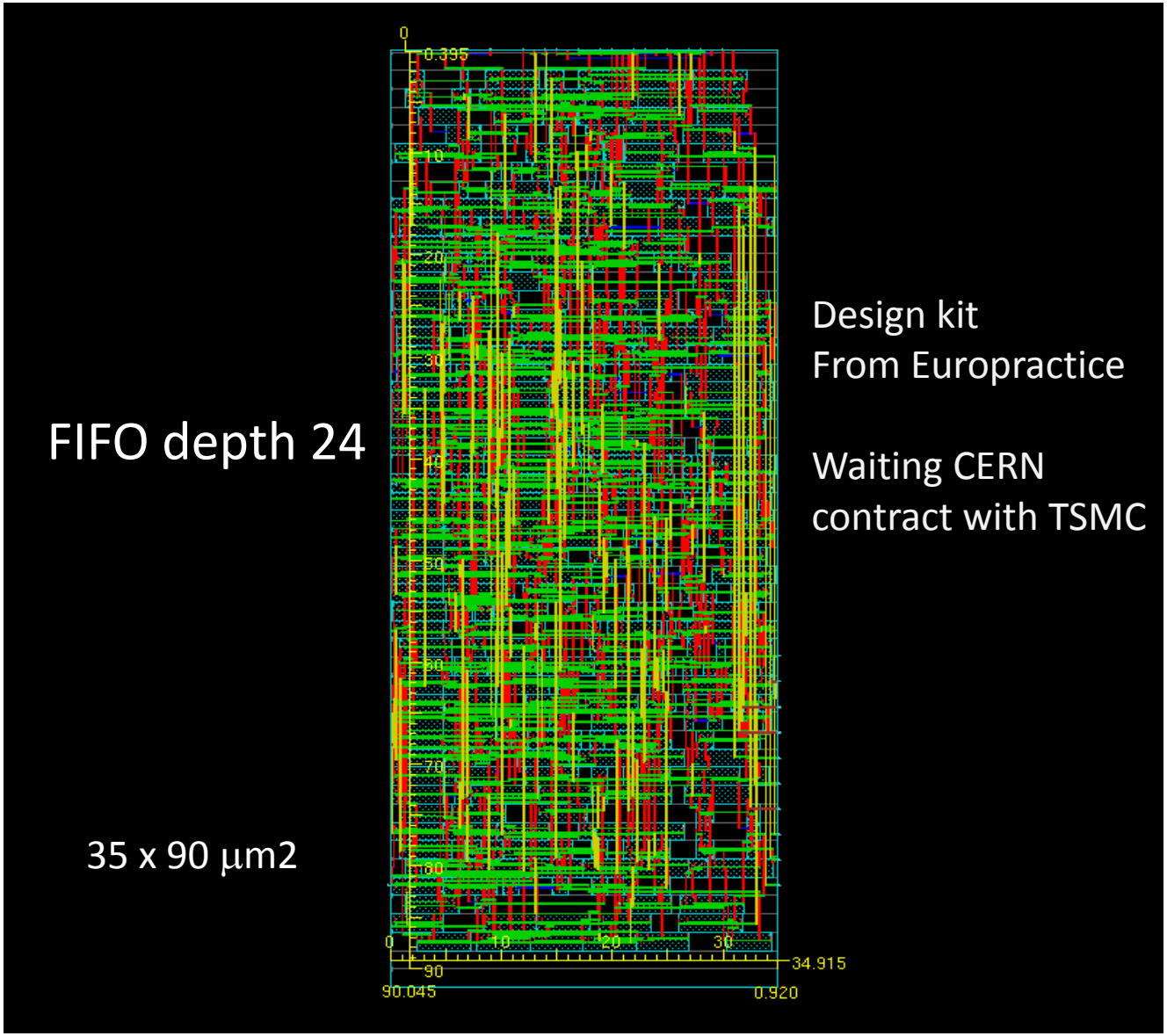
- The read pixel switch is **closed** after read
- The next hit pixel (switch open) is read

Building block



- VHDL model — OK
- Cells library — 65nm TSMC
- I/O locations file (x,y in microns) — text file
- Dimensions (FIFO depth 16) — 35 x 70 μm^2

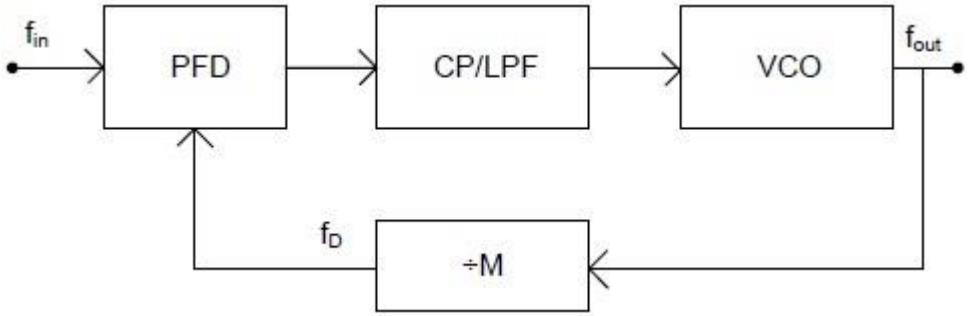
Layout in TSMC 65nm



PLLs (clock recovery)

Used as frequency synthesizers

Charge pump PLL (CP-PLL)



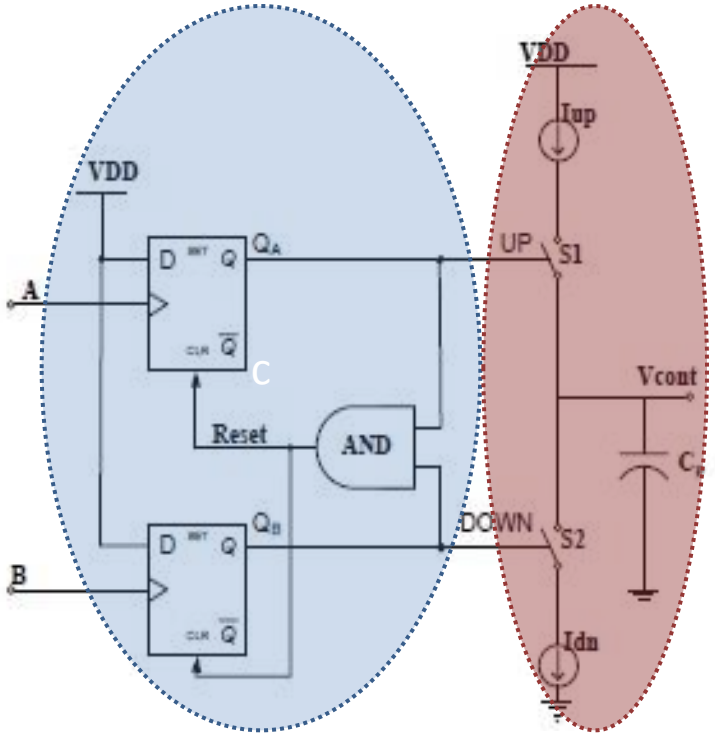
CP –PLL for frequency multiplication

Low power , low jitter , fully integrated

Typical Input frequency : 40 MHz
Output frequency range: 80 MHz-320 MHz

Slide from Jeanne Tongbong (LAL Orsay)

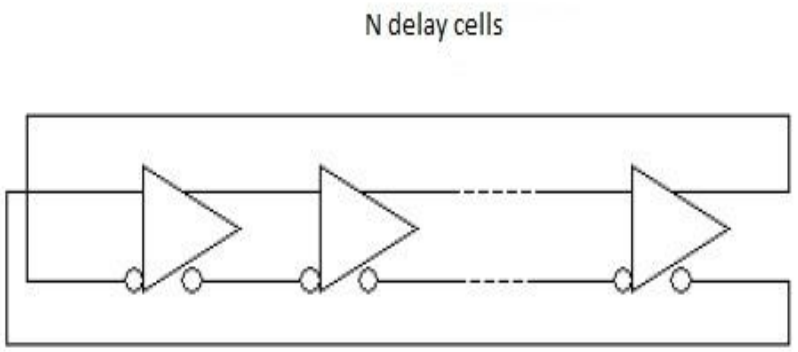
PLLs (clock recovery)



Phase Frequency Detector (PFD)

Chage Pump(CP) / Loop Filter (LP)

PFD-CP-LP basic implementation



Ring oscillator

Status: OMEGA develops PLL block in 350nm as a debugging block
Simulations going on in 65nm
Awaiting CERN design kit

Slide from Jeanne Tongbong (OMEGA)

LAPP involvement

- LAPP is strongly involved in the HL-LHC tracker upgrade (services, ALPINE design, cooling) and aims to be involved in tracker-related micro-electronics developments.
- support to OMEGA ;

  support to CPPM and FEi5 design.

→ LAPP team works on 65nm building blocks for future trackers which may be included in tracker readout chip.

Slide from Renaud Gaglione LAPP

Developments

- Present: design of a capacitive 12 bits DAC for CPPM 12 bits SAR GADC. 1V, 1MHz, ~mW

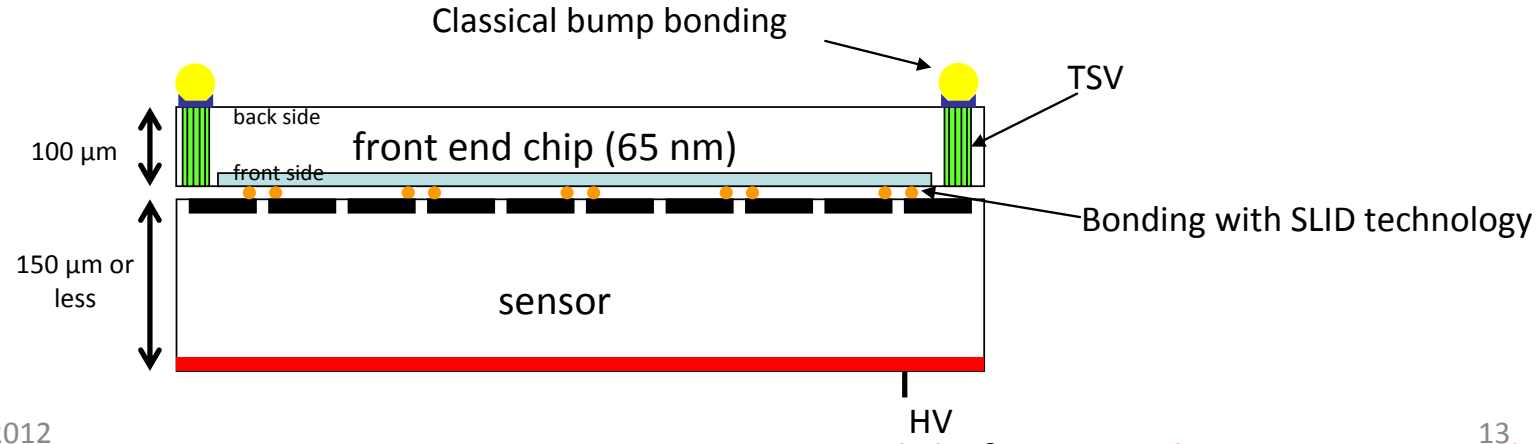
- Soon: specs and design of comparator for CPPM SAR GADC and for LAL Wilkinson ADC;
- Considered: JTAG block.

Slide from Renaud Gaglione LAPP

The end...

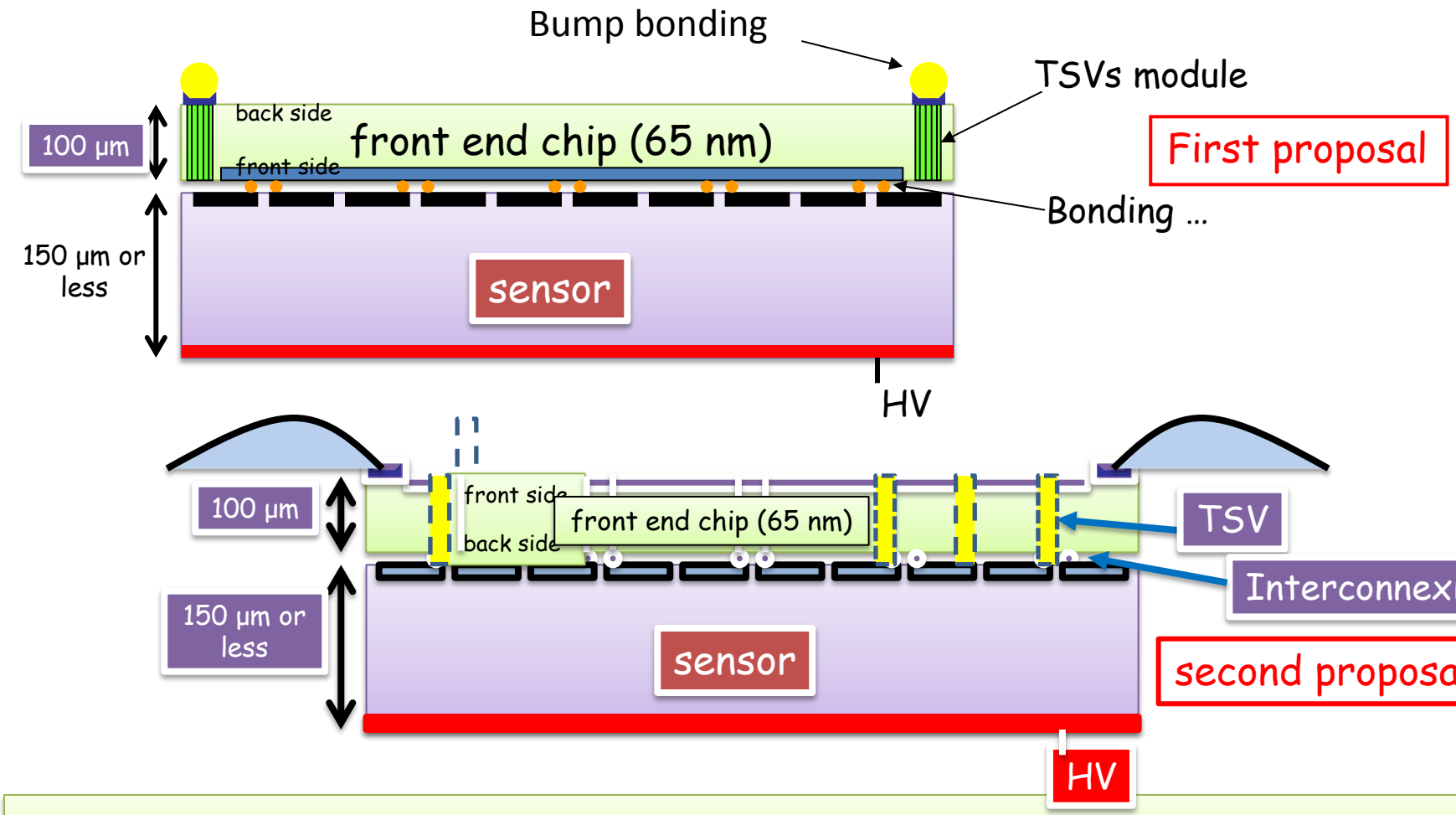
65 nm OMEGAPIX2

- A new OMEGAPIX chip in 65 nm techno as an alternative to the 3D chip
  - Same pixel form factor: 35x200 µm
  - New analog front-end (LAL), new digital pixel (LPNHE)
  - TSMC 65 nm techno
    - 3x1z1u metal stack (RF, CRN65LP), 6 metal layers + RDL
    - tcbn65lp standard cells library
  - In waiting for the common PDK provided by CERN



Slide from **D. Thienpont, J. Tongbong**

Sensor + Readout chip in 65nm



Via Last AIDA project: LAL + LPNHE+ LAPP

Slide from **Abdenour Lounis** **(IN2P3 LAL Orsay)**