

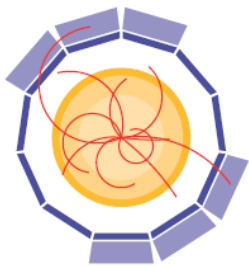
AIDA WP3 Annual Meeting

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- **Status of milestones and deliverables**
- **Progress report by sub-projects**
- **AOB**

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Frascati, April
2013



Milestones

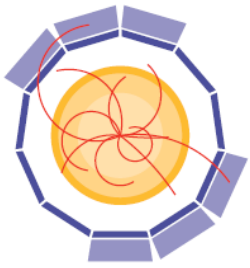
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Schedule of relevant Milestones

Milestone number ⁸⁹	Milestone name	Lead beneficiary number	Delivery date from Annex I ⁹⁰	Comments
MS18	Availability of wafers with ASIC	18	17	Layout of ASICs in MPW (Task 3.2)
MS19	Submission of dedicated sensors for 3D interconnection	11	17	Layout of sensors (Task 3.2)
MS20	Qualification of ASIC and sensors for 3D interconnection	18	25	Laboratory tests (Task 3.2)
MS21	Validation of first set of IP blocks	1	26	Laboratory tests and full documentation of functional blocks (Task 3.3)
MS22	3D interconnection processing accomplished	18	36	3D integrated devices available for technology assessment (Task 3.2)
MS23	Enable access to 3D interconnection technology	12	48	Laboratory tests for validation of 3D integration processes (Task 3.2)
MS24	Validation of second set of IP blocks	8	48	Laboratory tests and full documentation of

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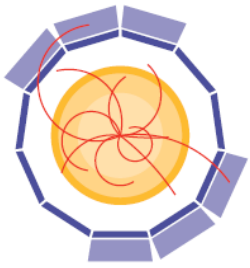
Deliverables

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List of deliverables

Deliverable Number ⁶¹	Deliverable Title	Lead beneficiary number	Estimated indicative person-months	Nature ⁶²	Dissemination level ⁶³	Delivery date ⁶⁴
D3.1	Organisation of the 3D production	18	20.00	R	PU	12
D3.2	Availability of wafers of ASIC electronics	18	30.00	R	PP	17
D3.3	Production of dedicated sensors	11	25.00	R	PP	17
D3.4	1st set of macro blocks	1	22.00	R	PU	22
D3.5	Wafer post processing (thinning, TSV)	12	24.00	D	PP	25
D3.6	Component processing	18	12.00	R	PU	29
D3.7	Test interconnection and evaluation	12	24.00	R	PP	36
D3.8	Detectors in 3D available for assessment	18	24.00	D	PP	40
D3.9	2nd set of macro blocks	8	22.00	R	PU	44
D3.10	Assessment of 3D integrated sensors	11	20.00	R	PU	48



Delivered (partially)

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D3.1 Organisation of 3D production (6 sub-projects defined)

- 1) Bonn/CPPM:
- 2) CERN:
- 3) INFN/IPHC-IRFU
- 4) LAL/LAPP/LPNHE/MPP
- 5) MPP/GLA/LAL/LIV/LPNHE
- 6) RAL/Uppsala

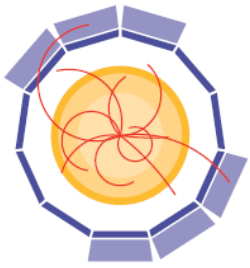
D3.2 Availability of wafers of ASICs electronics

Project name	ASIC	Availability status
Bonn/CPPM	FE-I4 (CMOS 130nm)	Available
CERN	MEDIPIX3 (CMOS 130nm)	Available
INFN/IPHC-IRFU	Superpix1 (3D CMOS 130nm)	4Q 2013
LAL/LAPP/LPNHE/MPP	Omegapix (CMOS 65 nm)	4Q 2013
MPP/GLA/LAL/LIV/LPNHE	FE-I4 (CMOS 130 nm)	Available
RAL/Uppsala	Hexitec (CMOS 350 nm)	Available

D3.3 Production of dedicated sensors

Project name	Sensors	Availability status
Bonn/CPPM	ATLAS pixel sensors	Available
CERN	VTT MEDIPIX3 sensors	Available
INFN/IPHC-IRFU	FBK planar sensors	4Q 2012
	FBK active edge sensors	4Q 2013
	CMOS sensors	4Q 2013
LAL/LAPP/LPNHE/MPP	150µm p-in-n	2Q 2014
MPP/GLA/LAL/LIV/LPNHE	CIS sensors	1Q 2013
	MPP sensors	3Q 2013
RAL/Uppsala	-	No sensors needed

Milestones and Deliverables in 2013



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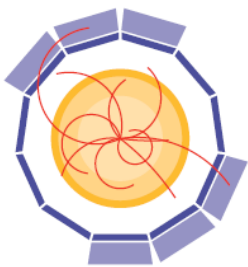
Milestones:

- 1) MS20 Qualification of ASICs and Sensors for 3D interconnection M25 (Feb 2013)
- 2) MS21 Validation of first set of IP blocks M26 (Mar 2013)
postponed till 65nm MPW available by CERN

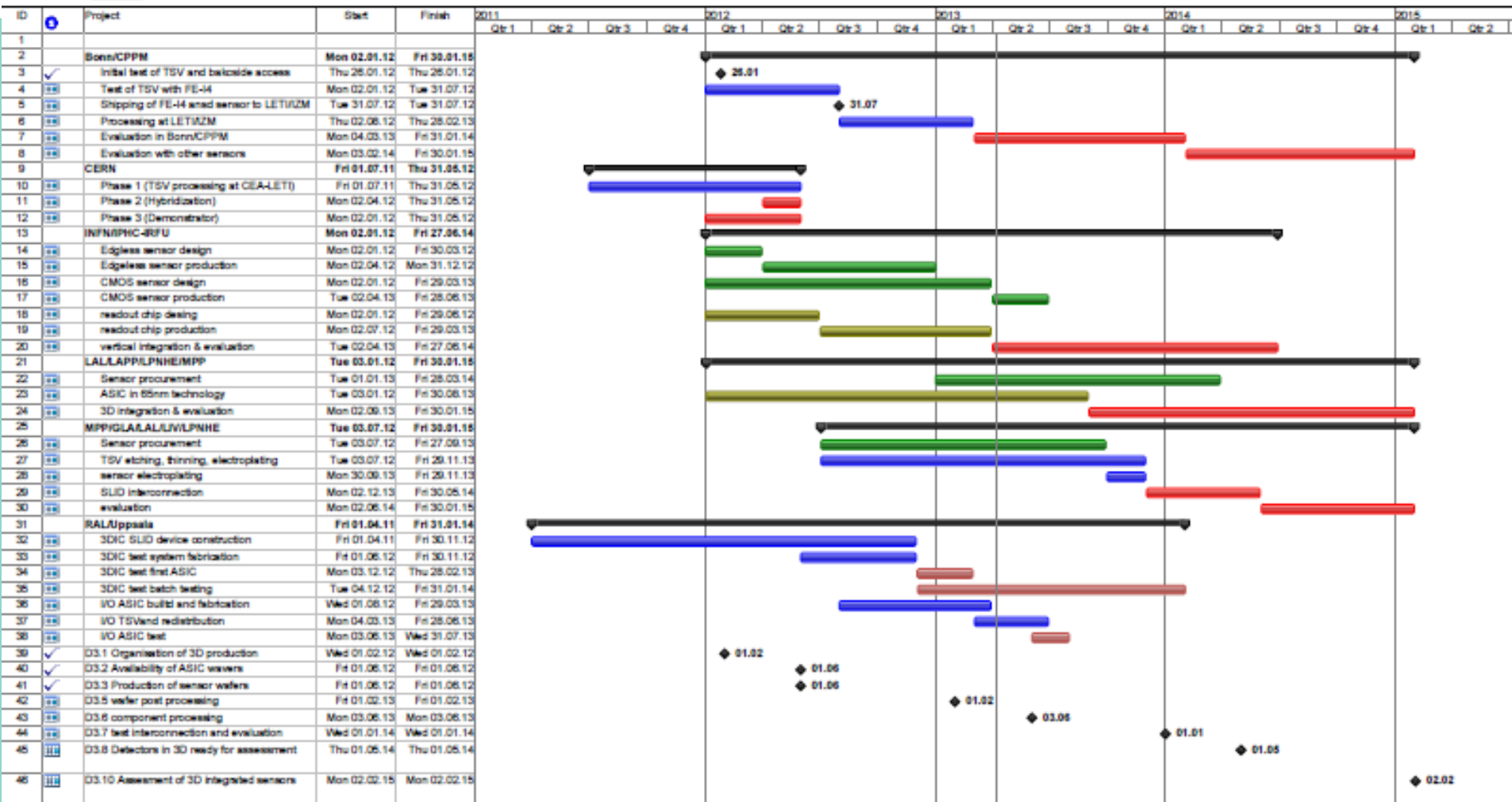
Deliverables:

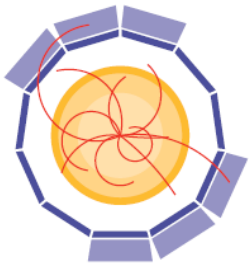
- 1) D3.4 First set of macro blocks M22 (Nov 2012)
postponed till 65nm MPW available by CERN
- 2) D3.5 Wafer post processing (thinning, TSV) M25 (Feb 2013)
- 3) D3.6 Component processing M29 (Jun 2013)

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Schedule





Bonn/CPPM Project

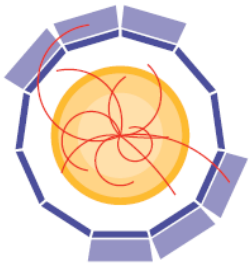
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Item	Start	Stop
Initial test of TSV process and backside access using “old” FE-I2 ICs (not part of AIDA WP3)		done
Test of TSV process with FE-I4A IC (not part of AIDA WP3)	In progress	Month 18
Shipping of FE-I4B and planar sensor wafers to LETI / IZM		Month 18
Processing at LETI / IZM	Month 19	Month 25
Process evaluation in Bonn / CPPM	Month 26	Month 36
possibly: Evaluation of prototypes with other sensors	Month 36	Month 48

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Wafers are at IZM for processing ? LETI?



CERN Project

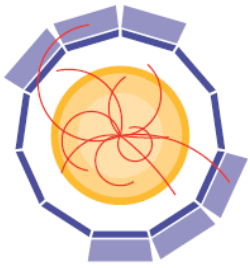
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Item	Start	Stop
Phase 1 (TSV processing of Medipix 3 wafers at CEA-LETI)	Month 6	Month 16
Phase 2 (Hybridization of the TSV processed read out chips)	Month 15	Month 17+
Phase 3 (Demonstrator module)	Month 12	Month 17+

Since Medipix chips with TSVs are available and have been tested. Phase 2 should be completed?

Next: interconnection to sensor



INFN/IPHC-IRFU Project

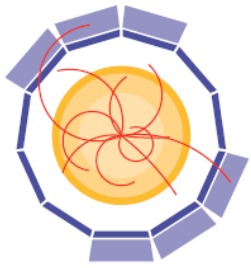
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Item	delivery
Edgeless sensor design	Month 14
Edgeless sensor production	Month 23
CMOS sensor design	Month 26
CMOS sensor production	Month 29
Readout chip design	Month 17
Readout chip production	Month 26
Readout chip-to-sensor vertical integration	Month 41

Planar sensors under test
Edgeless sensors designed and fabrication at FBK scheduled
Interconnection tests with T-MICRO (to be evaluated)
3D MAPS from Tezzaron under test

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LAL/LAPP/LPNHE/MPP PROJECT

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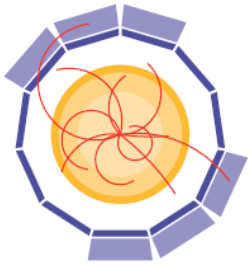
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Project	Start	Finish
Sensor procurement	Tue 01.01.13	Fri 28.03.14
ASIC in 65nm technology	Tue 03.01.12	Fri 30.08.13
3D integration & evaluation	Mon 02.09.13	Fri 30.01.15

CIS and VTT sensors delivered?

Status of 65nm ASIC: ready for submission? Wait for CERN MPW?

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MPP/GLA/LAL/LIV/LPNHE Project

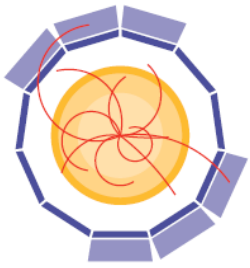
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Item	Start	Stop
Sensor procurement	Month 18	Month 32
TSV etching, ASIC wafer thinning and electroplating	Month 18	Month 34
Sensor wafer electroplating	Month 32	Month 34
SLID interconnection	Month 34	Month 40
Evaluation	Month 40	Month 48

CIS sensors expected in June 2013?
ASIC wafer processing: needs change of TSV etching,
In discussion with EMFT. Status?

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Item	Start	Stop
3DIC SLID Device construction	Apr 11	Nov 12
3DIC test system fabrication	June 12	Nov 12
3DIC test first ASIC	Dec 12	Feb 12
3DIC test batch testing	Dec 12	Jan 14
I/O ASIC build and fabrication	Aug 12	Mar 13
I/O TSV and redistribution	Mar 13	June 13
I/O ASIC test	June 13	July 13

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Now news !