Methods for architectural design methods of 3D-integrated systems

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Agenda

- Introduction
- Case study: interposer for Wide I/O memory – processor integration
- Chip-Package-Board-Co-design
- 3D-Floorplanner and Flow
- Conclusion

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Design Automation Division EAS

Profile

- One of the largest research institutions in the field of design automation in Europe
- Microelectronics and heterogeneous systems
- Focus on all aspects of functional design

Challenges

- Mastering the growing complexity of electronic systems
- Closing the gap between manufacturing and system design
- Comprehensive consideration of different physical domains

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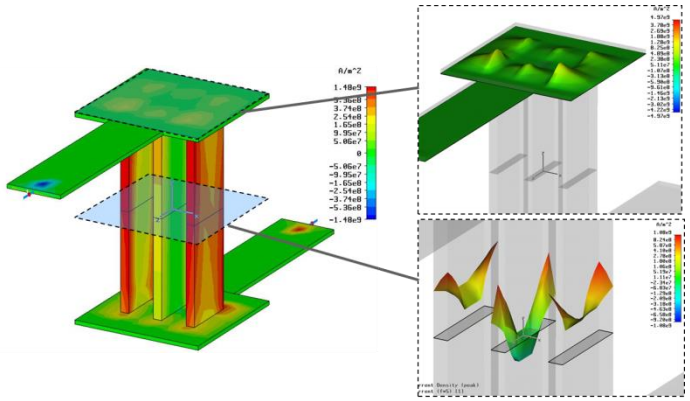
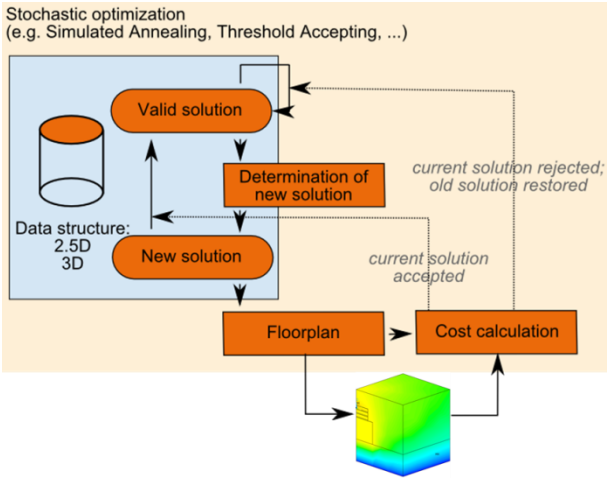
3D @ Fraunhofer IIS/EAS

History

- Involved in 3D projects for over 10 years
- Starting with electrical characterization of TSVs and thermal simulation
- Focused on technology improvement



Current density in via structure



Today

- Multi physics analysis for library development and design rules
- Integration into Design tools and flows
- Development of methods for design space exploration (aca path finding, scouting) and floorplanning
- Support of system design

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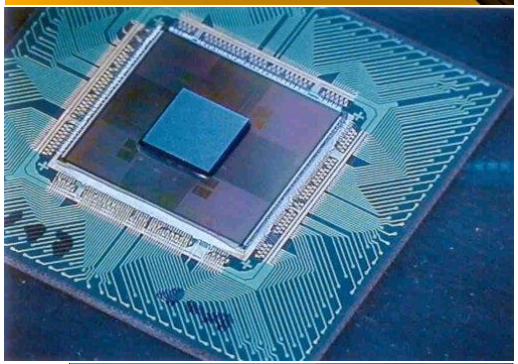
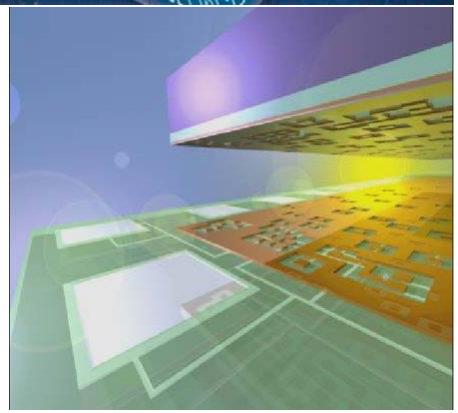
Why should the designer move from SoC to 3D Integration?

- Integration of mixed technologies
- Performance
  - Reduced interconnect length
  - Lower delay, higher speed
  - Reduced power consumption
- Form Factor
  - Reduced volume and weight
  - Reduced footprint
- Reduced Costs
  - Cost per transistor start to grow below 22-nm
  - Integration of heterogeneous technologies
  - Integration of dies from high volume production
  - Higher re-use rate (IP cores)





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What designers ask:

- What is the diameter of TSV? How big is the keep-out zone?
- How many TSV can I use?
- Who manufactures prototypes?
  - Who provides the interposer?
  - Who makes stacking and packaging?
  - How much costs this?
- Who manufactures products?
  - Production time?
  - Prizes?
  - Testability?
- How can I design this?
  - EDA-tool environment
  - Design Guidelines / Design-Kits

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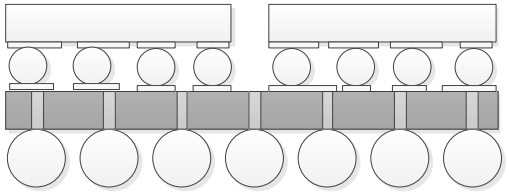
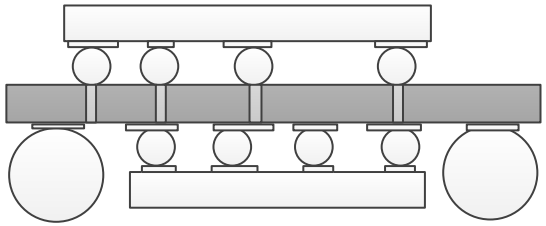
Evolution of advanced packaging

2.5D-integration with interposer

- Multiple IC are integrated at substrate or interposer
- Supports integration of existing IP
- Commercial application has been started
- **Reduced signal delay**



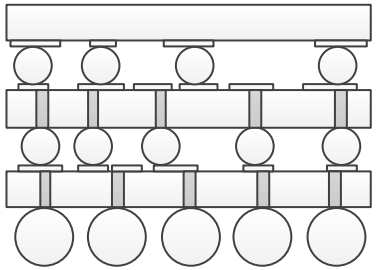
Side-by-side



Top-bottom

3D-integration

- System and individual dies are optimized for 3D
- Provides **highest performance** and integration level
- Co-design needed
- Still in development only few products on market (memory stacks, processor with memory)



Direct stacking

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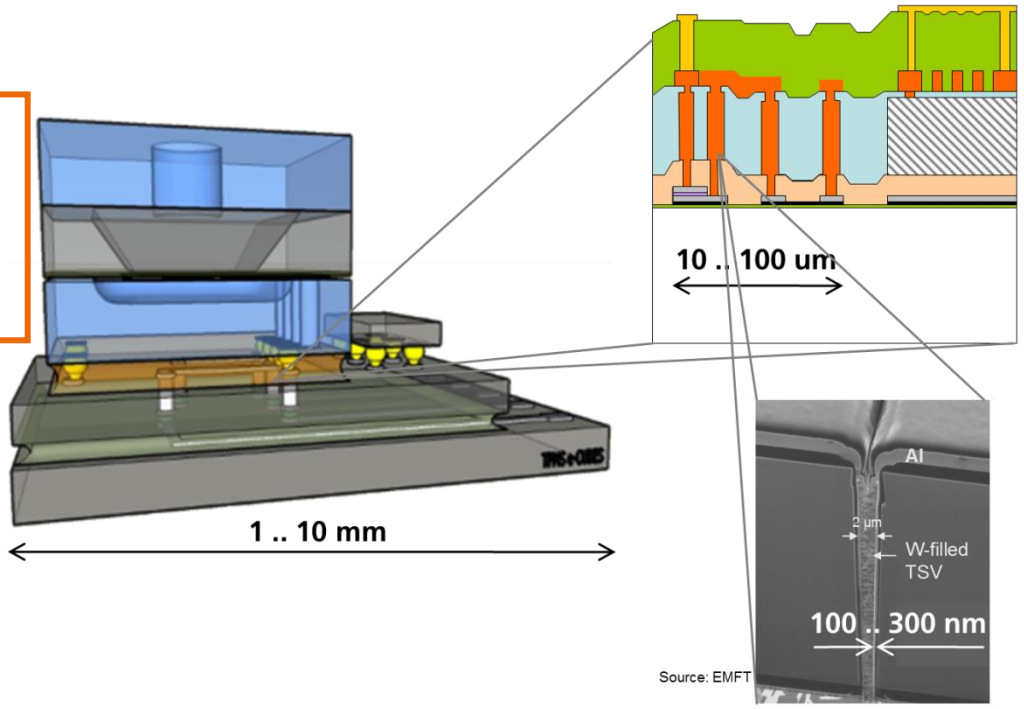
Challenges for 2.5D and 3D design

Top challenge for system design

- Early estimation of performance, cost, reliability and risks

Why is this so difficult?

- Design space complexity
- Structural complexity
  - Multi scale, multi physics
  - Exceeds capacity of current simulators
- Process complexity
- Collaboration complexity
  - System architect
  - Component Designers
  - IC manufactures
  - OSATs



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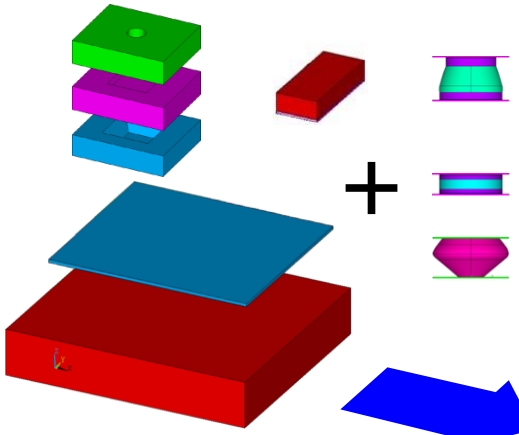
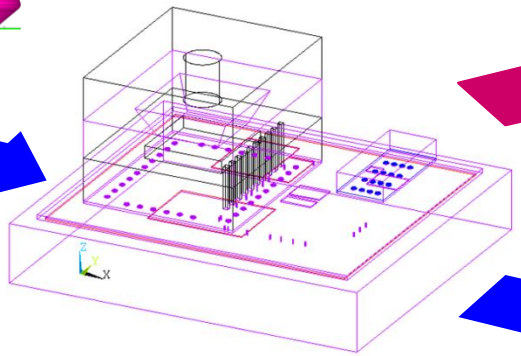
Modeling Concepts for Multi-Physics- Analysis

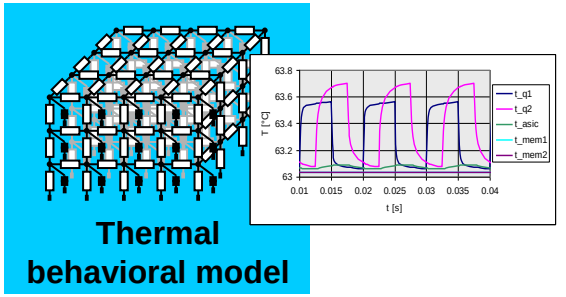


Modular building blocks

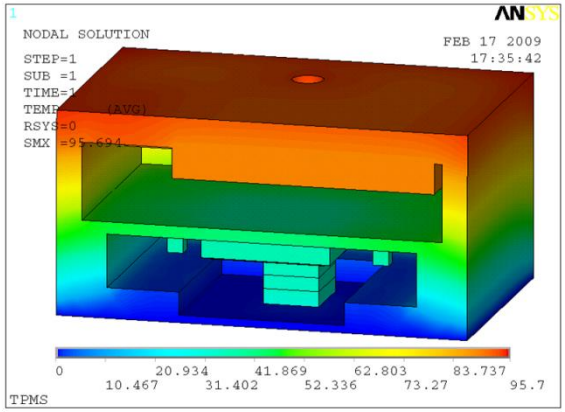


FE model (ANSYS)

Model order reduction



(Electro-)Thermal system simulation



Thermal simulation of entire 3D stack

- Detailed analysis of individual or critical parts with 3D-FEM analysis
- Development of models at higher abstraction levels to handle system complexity
- Interfaces between different tools

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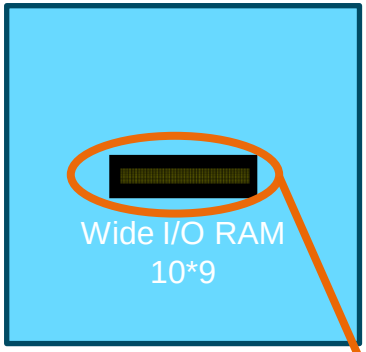
First Standard: JEDEC Wide I/O memory

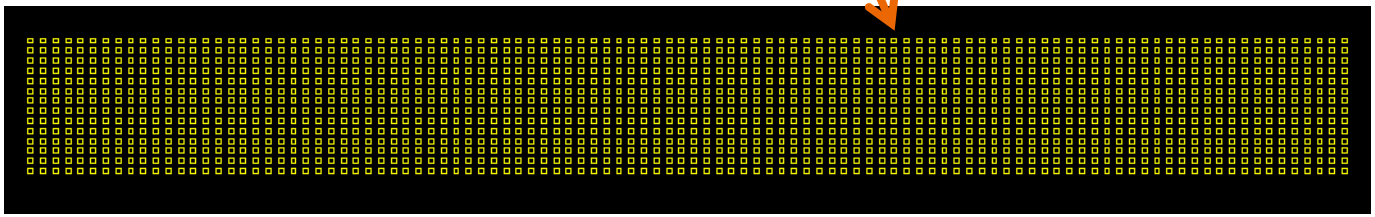
- Application: memory on memory, memory on processor stacking
- JEDEC wide I/O memory standard for 3D integration: JESD229



Very small size of pad area

- 100 * 12 field of pads
- With 50 * 40um Pitch

Pads are located in
the center of memory die



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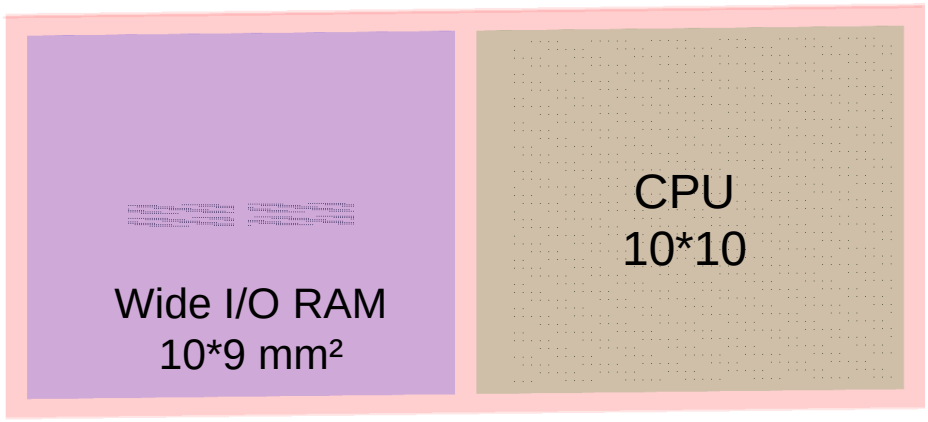
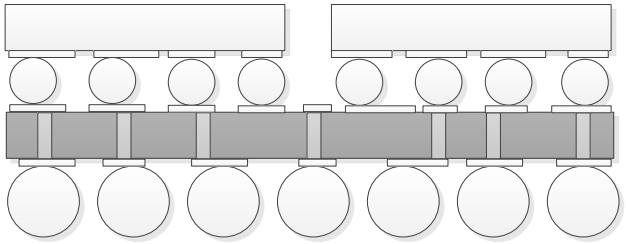
Case study: Side by side integration of JEDEC Wide I/O memory and processor





Pads are located in
the center of memory die

Requirements

- 2200 pins processor, 1200 pins memory, 1000 pins external
- Side by side integration to avoid thermal and other problems
- Optimized for mass production

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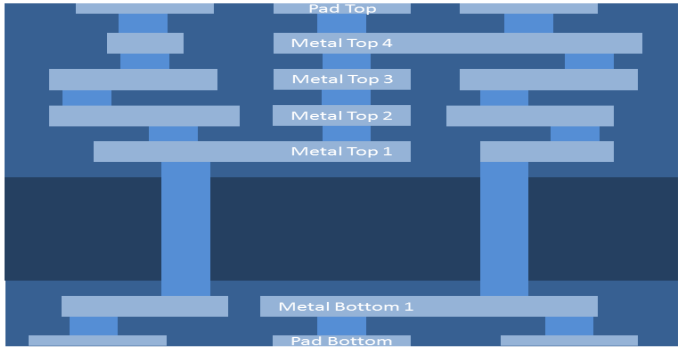
2.5D interposer for JEDEC Wide I/O memory

Initial Configuration



Technology Parameters:

- 10um metal width
- 10um metal space
- 10um TSV

- Top of interposer
  - 4 metal layers for signal routing
  - 1 additional metal layer for pads
- Bottom of interposer
  - 1 metal layer for signal routing
  - 1 additional metal layer for pads
- As both active IC placed on top, signals will be mainly routed on top of interposer -> less TSV needed

But 5 metal on top and only 2 at bottom is not a good choice …

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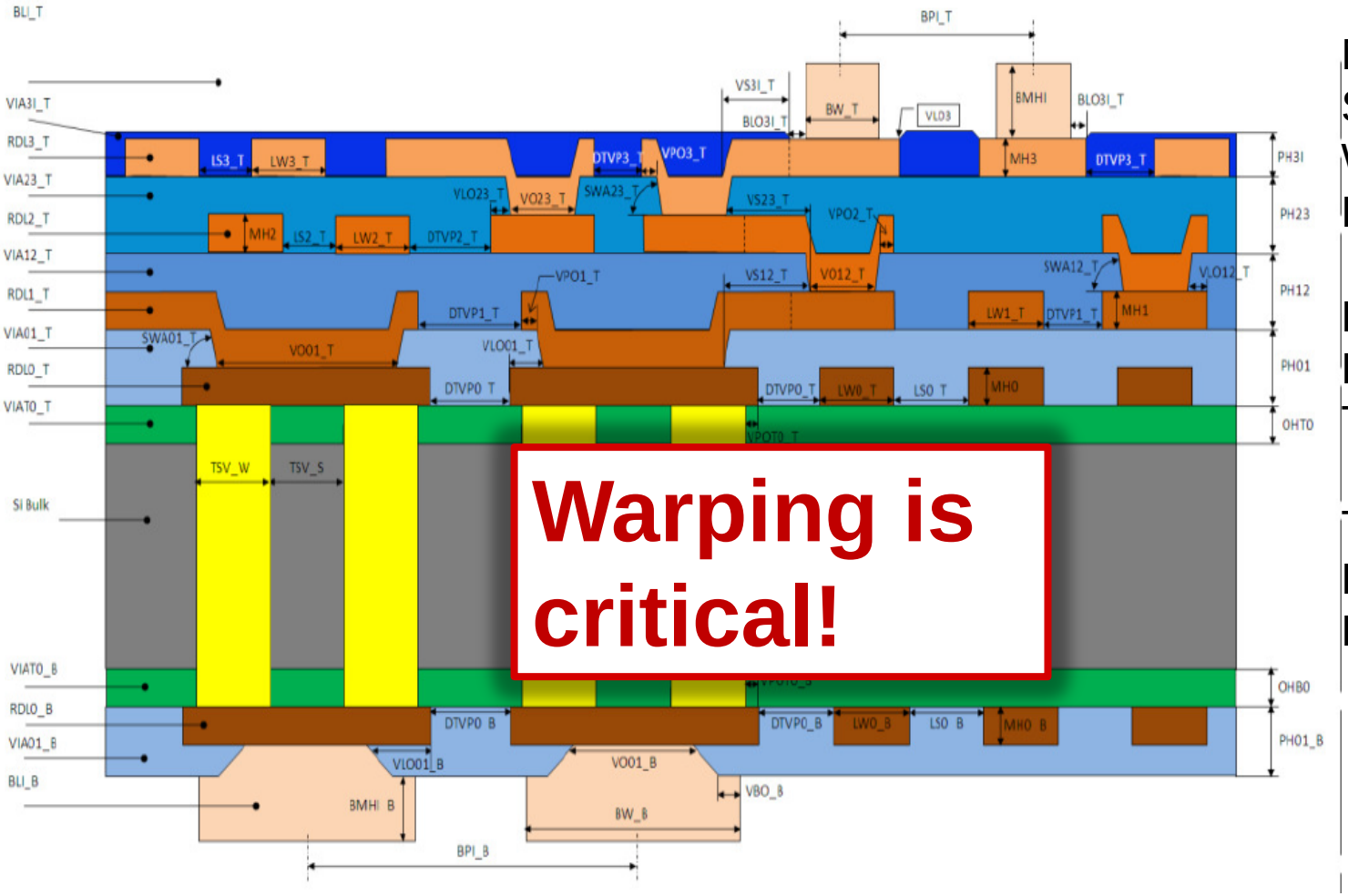
Technology Design Guide Lines



Warping is critical!

Metal:
Space 8µm
Width 8µm
Height 3µm

Dielectric:
Polymer e_r 2.9
Thickness 5µm

TSV:
Diameter 10µm
Depth 120µm

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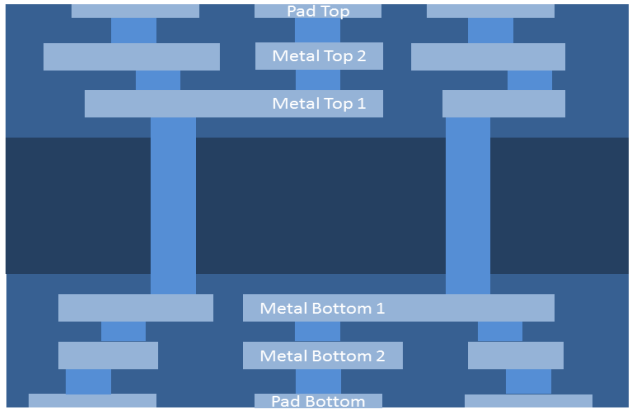
2.5D interposer for JEDEC Wide I/O memory

Second configuration



Technology Parameters:

- 10um metal width
- 10um metal space
- 10um TSV

- Top of interposer
  - 2 metal layers for signal routing
  - 1 additional metal layer for pads
- Bottom of interposer
  - 2 metal layer for signal routing
  - 1 additional metal layer for pads
- Number of metal layers balanced between top and bottom
- More TSV needed (also for connections between processor and memory)
- Simultions shows that timing constraints can be achieved with routing via TSV

The warping can be avoided,
but we can additionally save costs …

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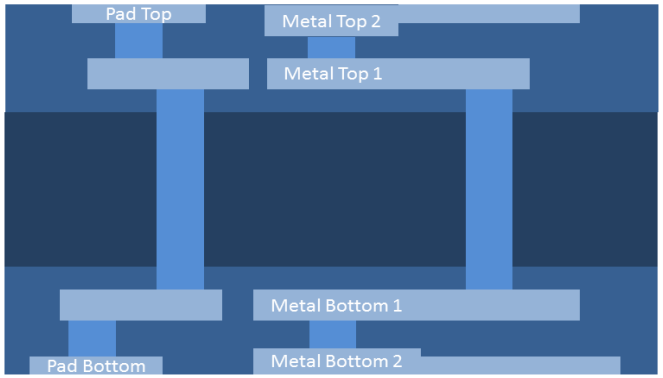
2.5D interposer for JEDEC Wide I/O memory

Cost optimized configuration



Technology Parameters:

- 10um metal width
- 10um metal space
- 10um TSV

- Top of interposer
  - 1 metal layer for signal routing
  - 1 metal layer for routing and pads
- Bottom of interposer
  - 1 metal layer for signal routing
  - 1 metal layer for routing and pads
- Number of metal layers balanced
- Only two metal layers on each side!

Challenge:

- Very high density of wires at interposer
- Standard routing algorithms need more metal layers
- Optimized interposer was routed by our inhouse algorithms

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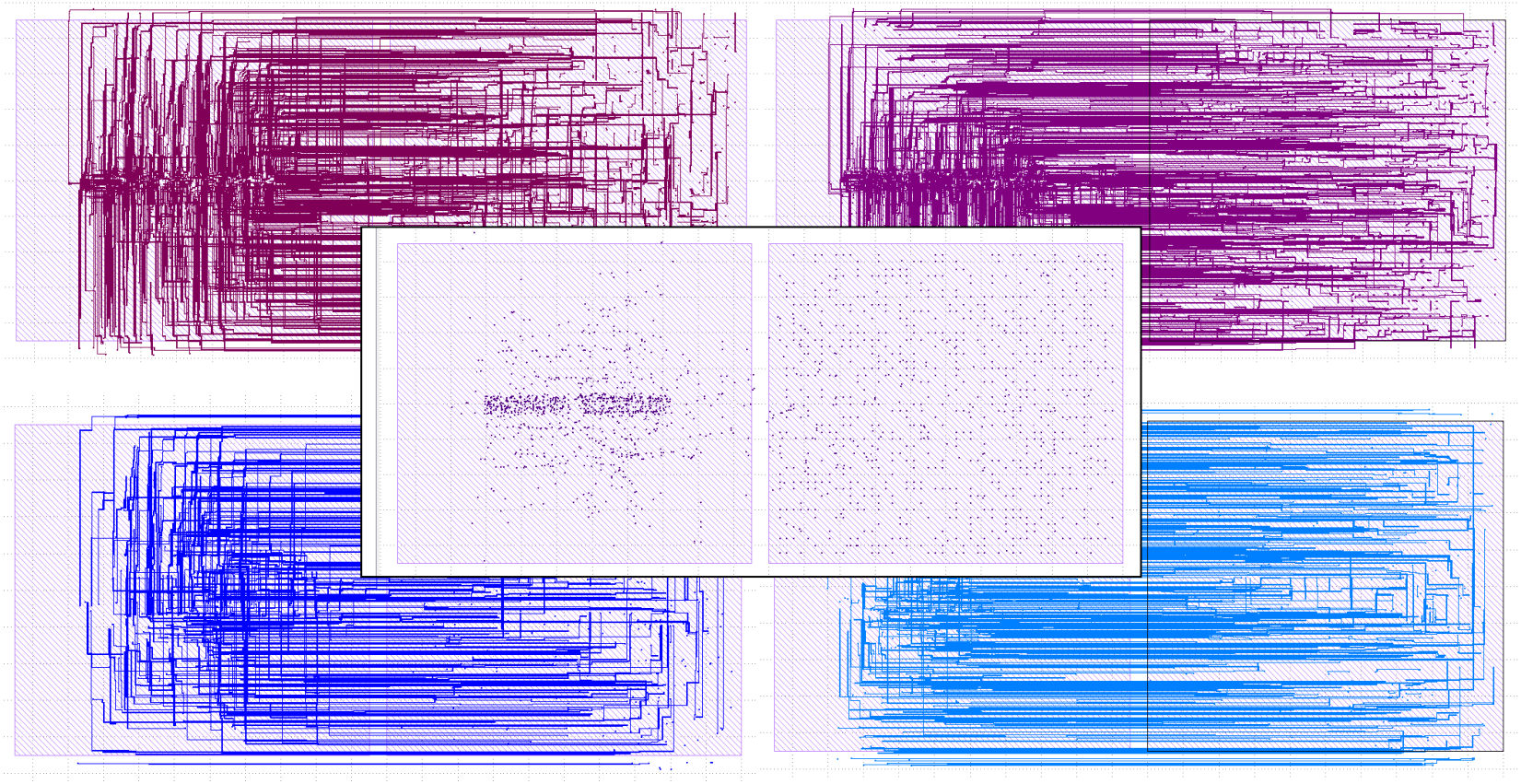
Interposer for Processor and JEDEC Wide IO Memory

Cost optimized configuration – Interposer layers and TSV



Manufacturing of wide-I/O demonstrator is ongoing at our colleagues from Fraunhofer IZM/ASSID.

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Chip-Package-Board-Co-design (1)

Requirements

- Evaluation of different packages
- Evaluation of different stacking technologies
  - Side-by-side in package (e.g. SiP, eWLB)
  - Side-by-side at interposer
  - 3D stacking
- Evaluation of different assembly technologies
  - Ball, bumps, bonding
  - Die to wafer, wafer to wafer
- Embedding of passives
- Evaluation of PCB technology (routability around device)
- Considering performances
  - e.g. timing, temperature
- Consideration of production cost demands

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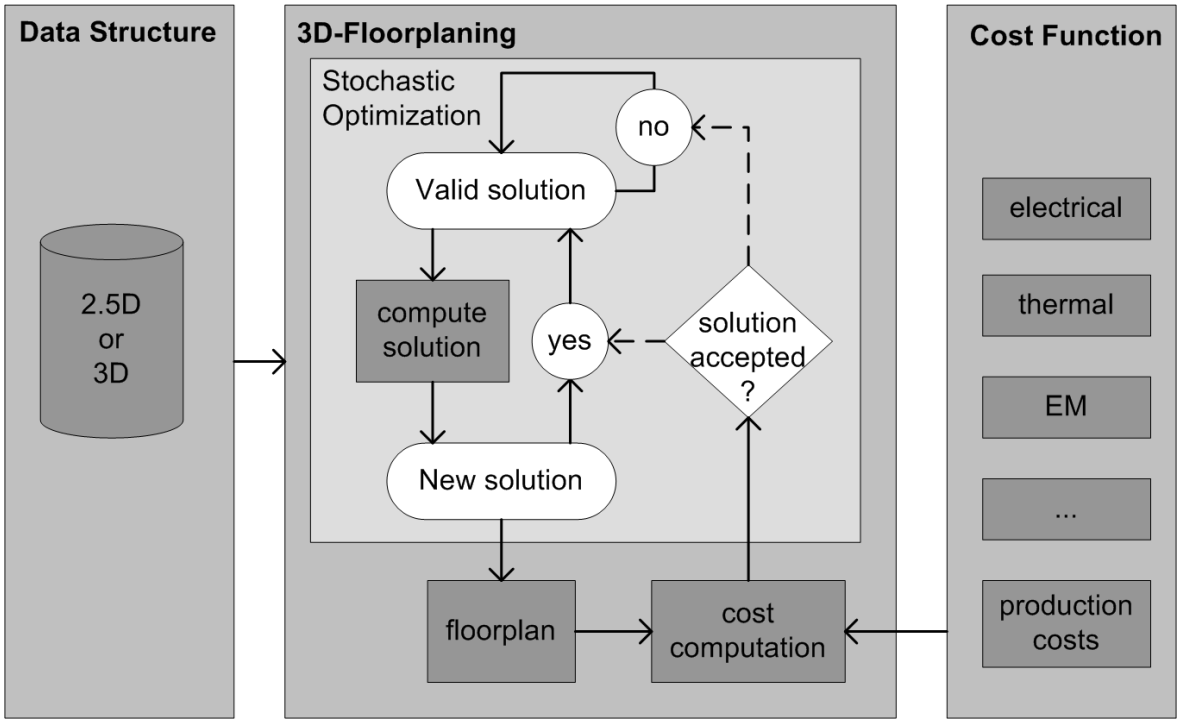
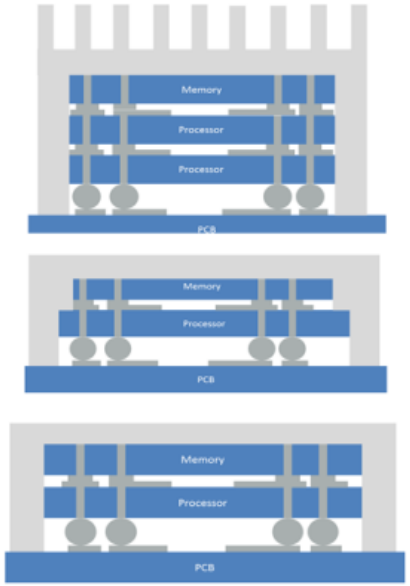
Chip-Package-Board-Co-design (2)

Goal: Guide the system designer to find the best suited solution.





- Optimization goal is production cost under consideration of performance requirements
- First generic cost function available, extension to company specific functions is ongoing

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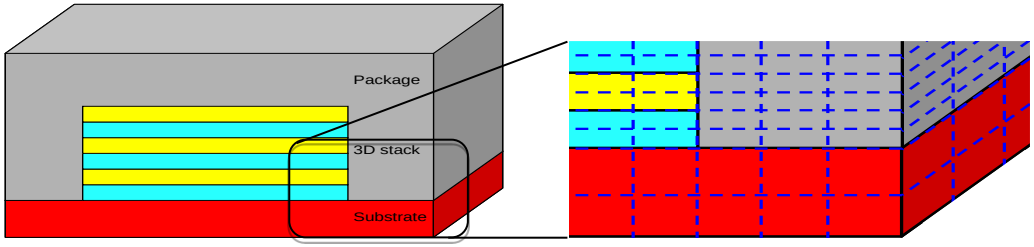
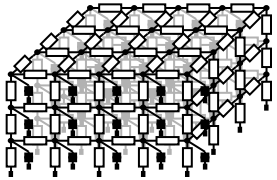
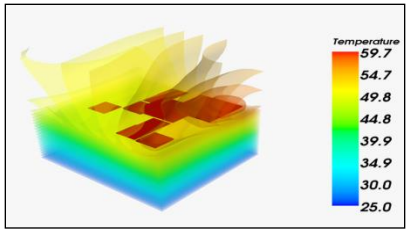
Thermal aware design space exploration

- Estimation of heat distribution in a stack
- evaluation of thermal constraints during design space exploration
- further research on package modeling ongoing

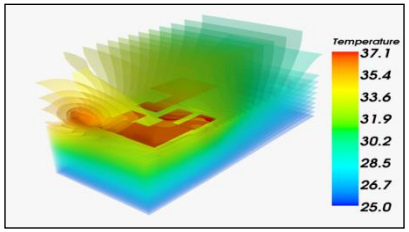




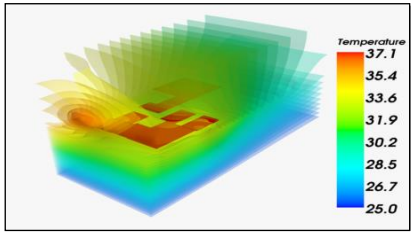
Thermal behavioral model



Initial floor plan



After thermal optimization



Final result (heat transfer and die size optimized)

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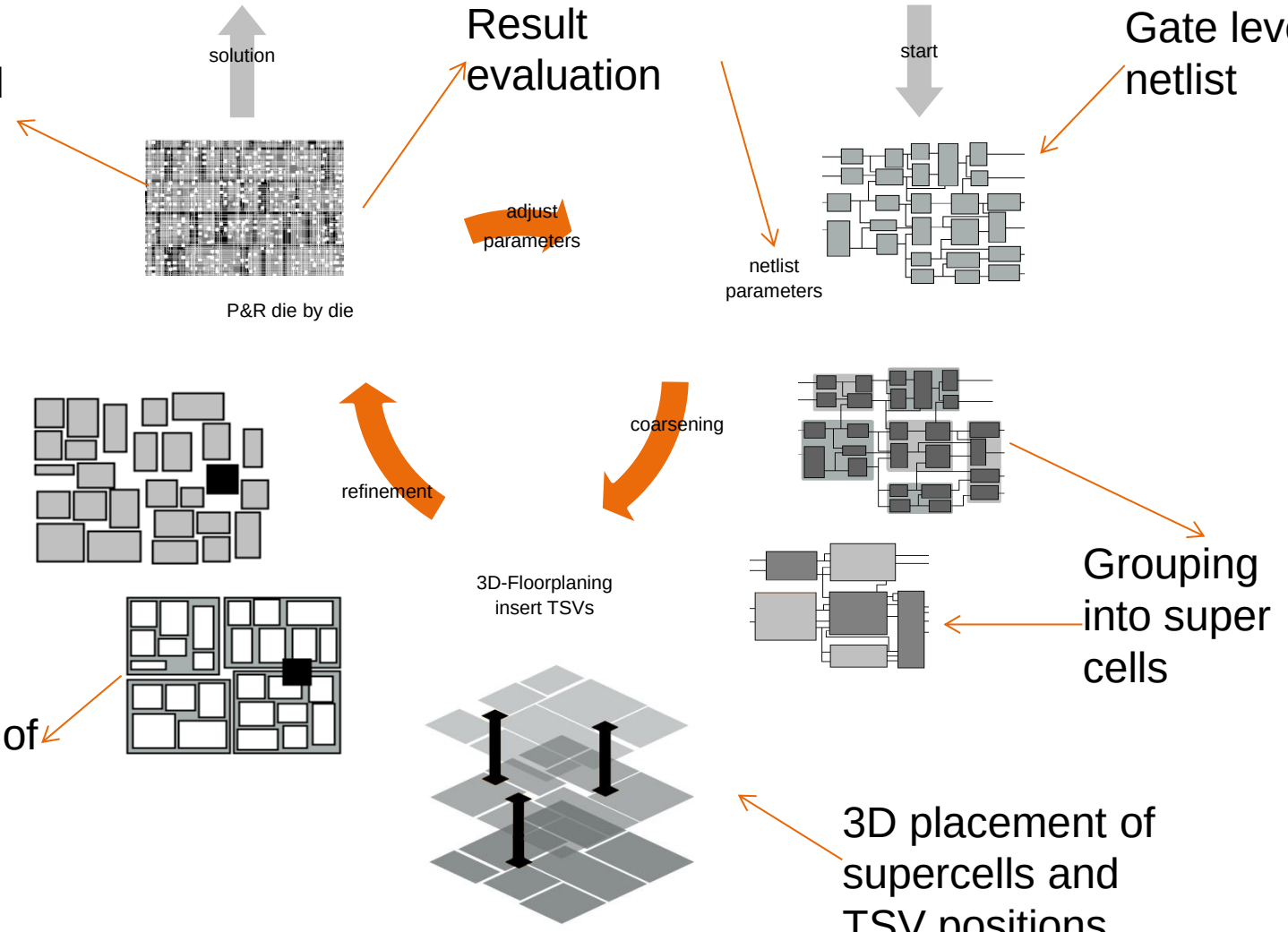
3D- chip-stack co-design flow @ Fraunhofer EAS



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3D Integration – Summary

- 3D-integration technologies offer
  - A wide design space for system realization
  - Increased system performance and higher integration level

- 3D-integration is still a new technology
  - Only few reference projects exist
  - Commercial products starts with 2.5D at interposer
  - Yield of 3D-manufacturing is increasing continuously

- Broader application of TSV-based products needs better ecosystem
  - EDA tools need to be enhanced or developed
  - Design-kits, design-rules and cost models are required
  - Standardization of design and manufacturing processes is ongoing, (IEEE, JEDEC, Semi Si2)

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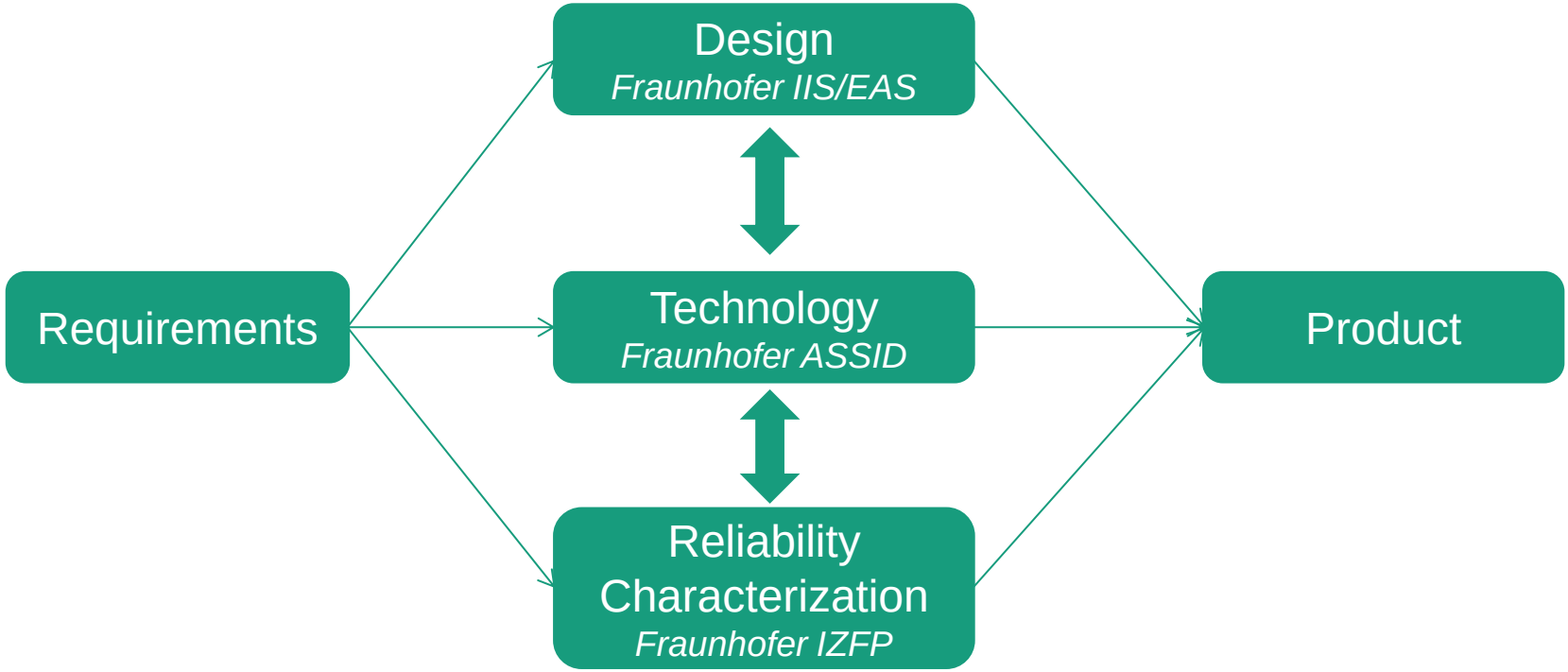
2.5 and 3D Design and Technology @ Dresden

- Strong dependency between design and technology (manufacturability, reliability, and yield)
- Fraunhofer offers technology/manufacturing and design support at their institutes in Dresden



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