SiPM Interconnections to 3D electronics

- SiMPs basics
- Why do we need 3D interconnections
- Concept of SiPMs with Bulk Integrated Quench Resistors – SiPMl concept
- What we want to do

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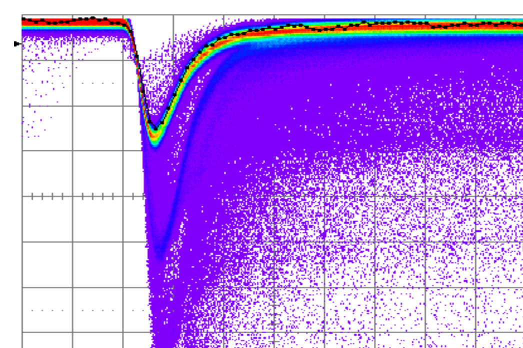
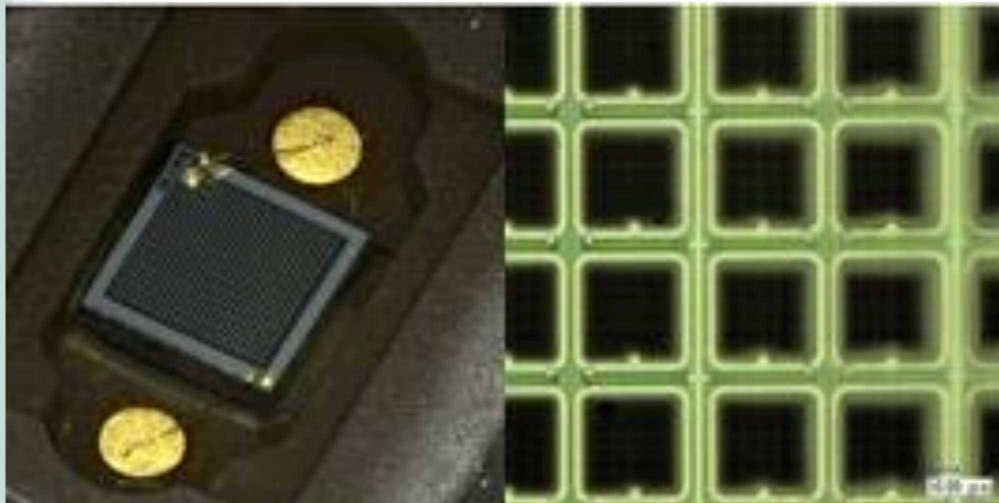
What is a Silicon Photomultiplier - SiPM

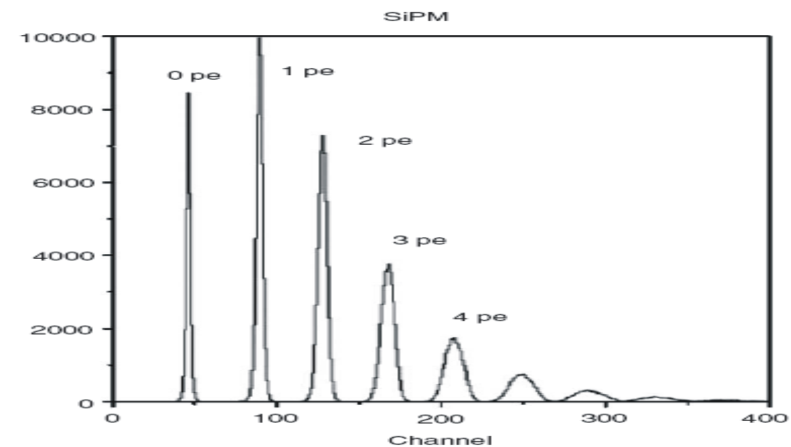
mpi halbleiterlabor

•An array of avalanche photodiodes

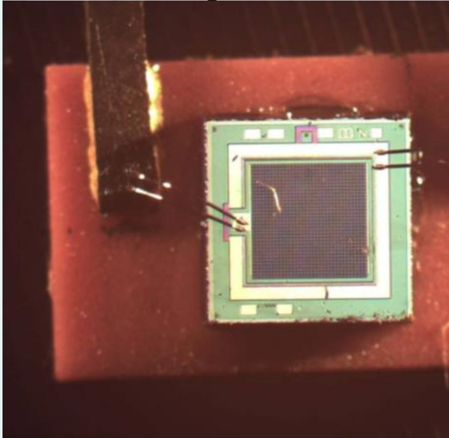
- operated in Geiger mode → binary device
- passive quenching by integrated resistor
- read out in parallel → signal is sum of all fired cells

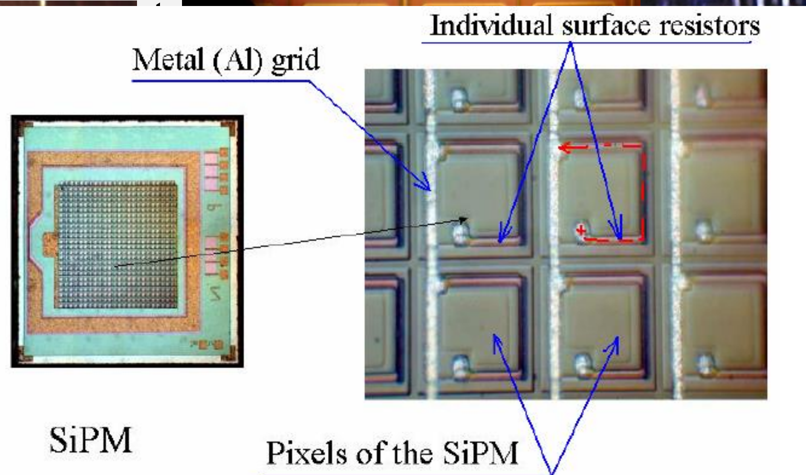


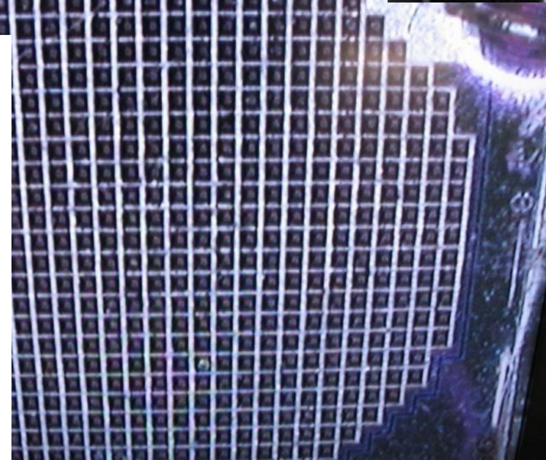




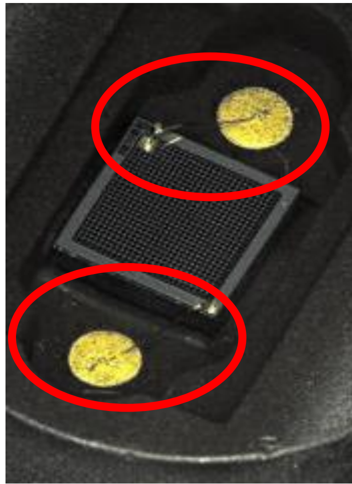
What is available?

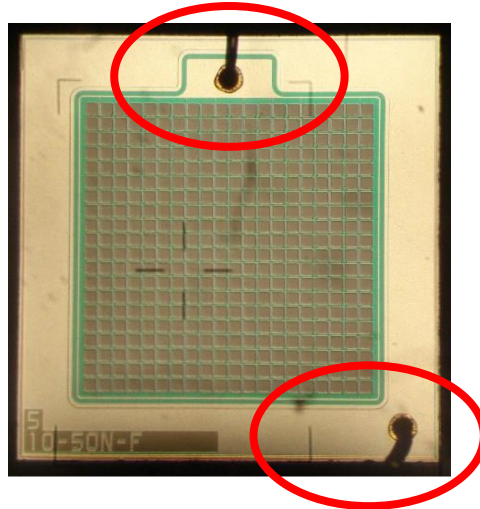


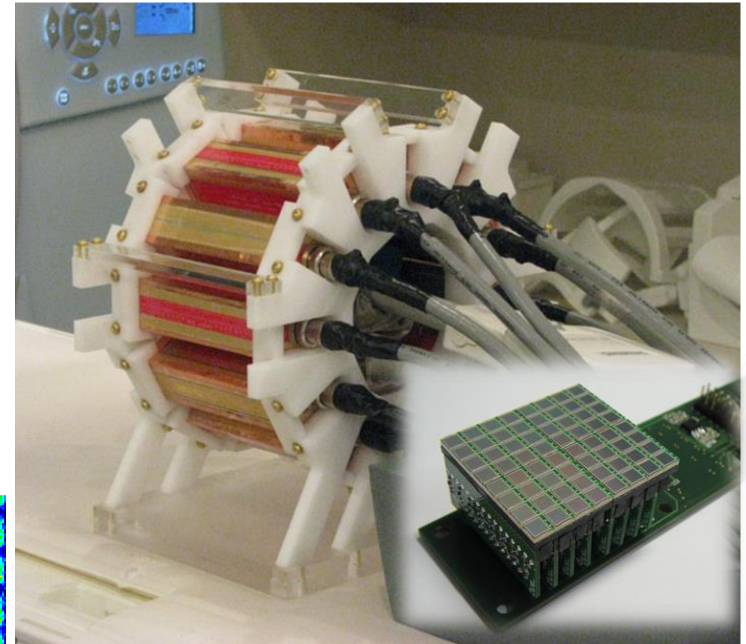


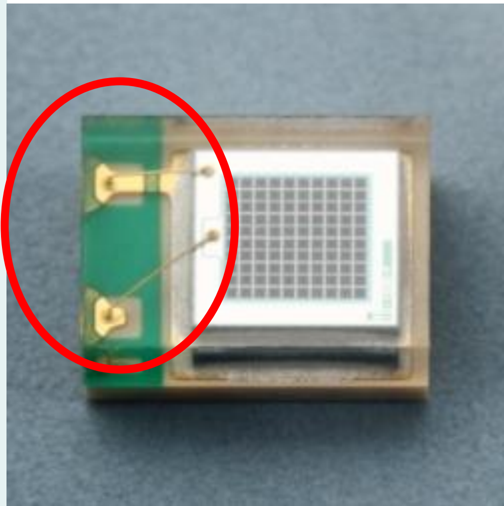


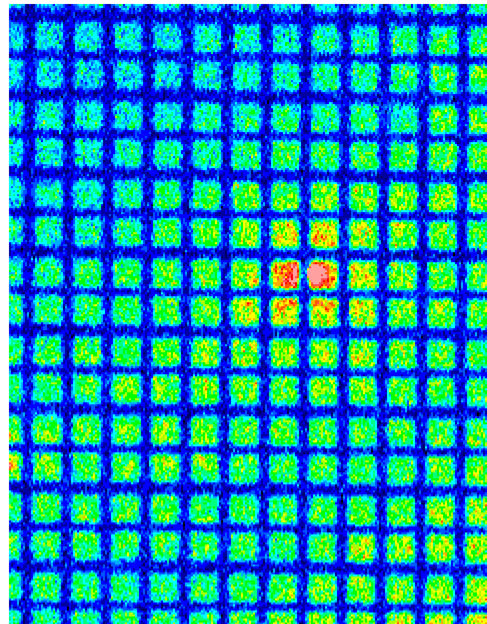
Why do we need 3D integration?



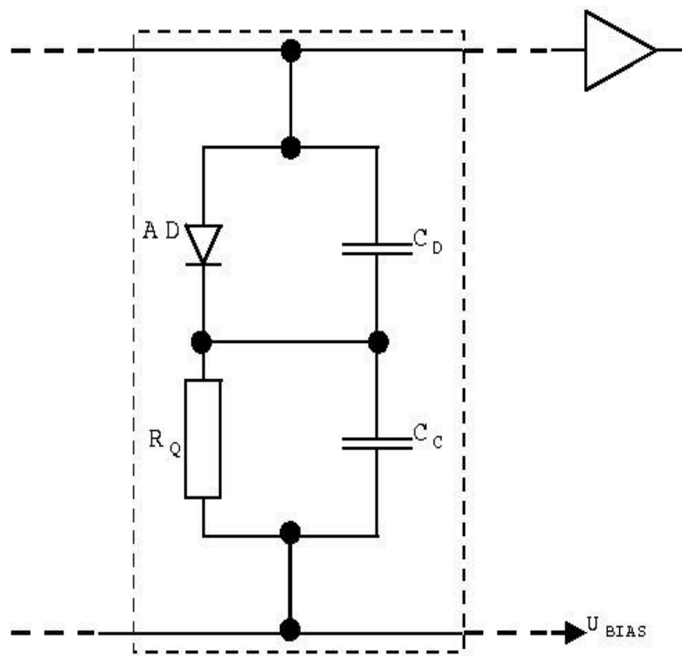


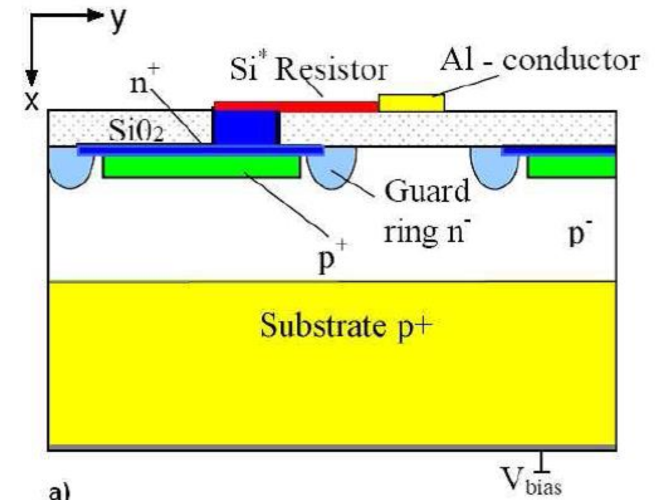


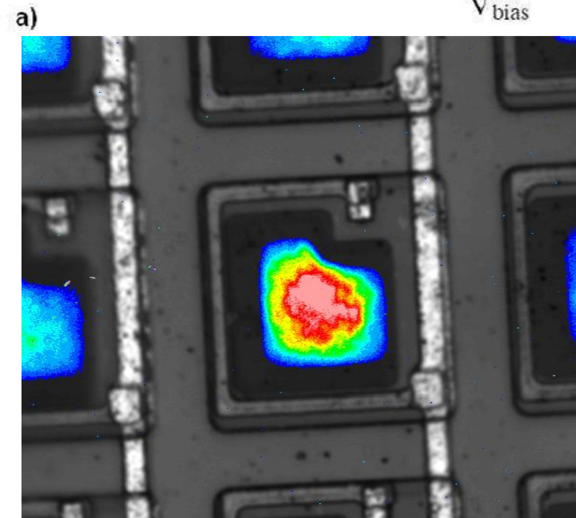




Components of a SiPM cell







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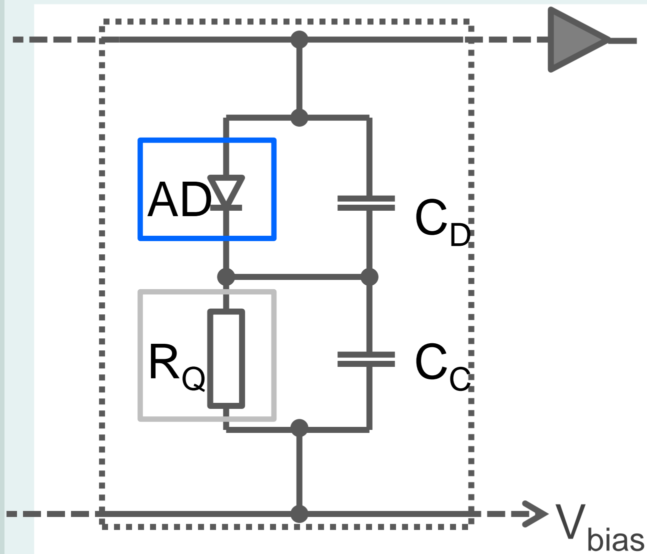
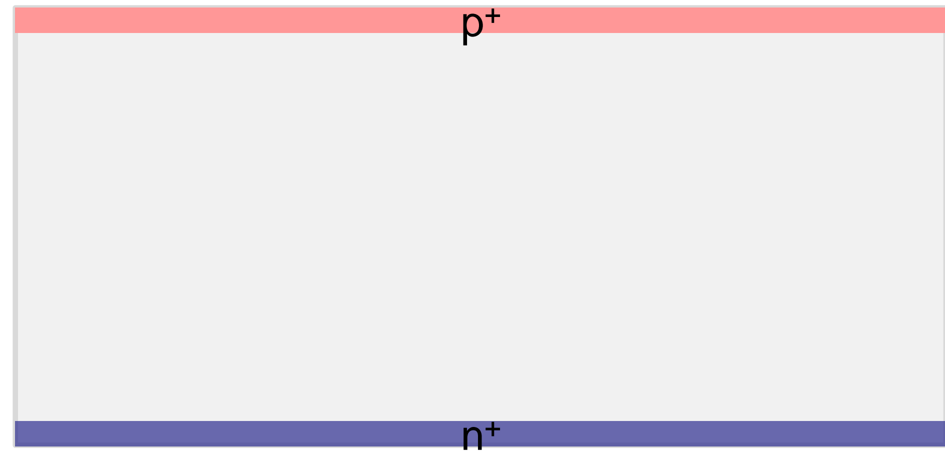
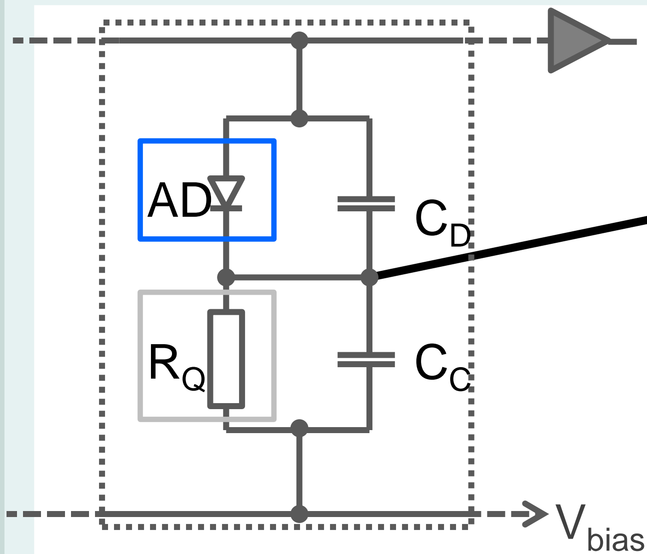
SiPM cell components → SiMPI approach

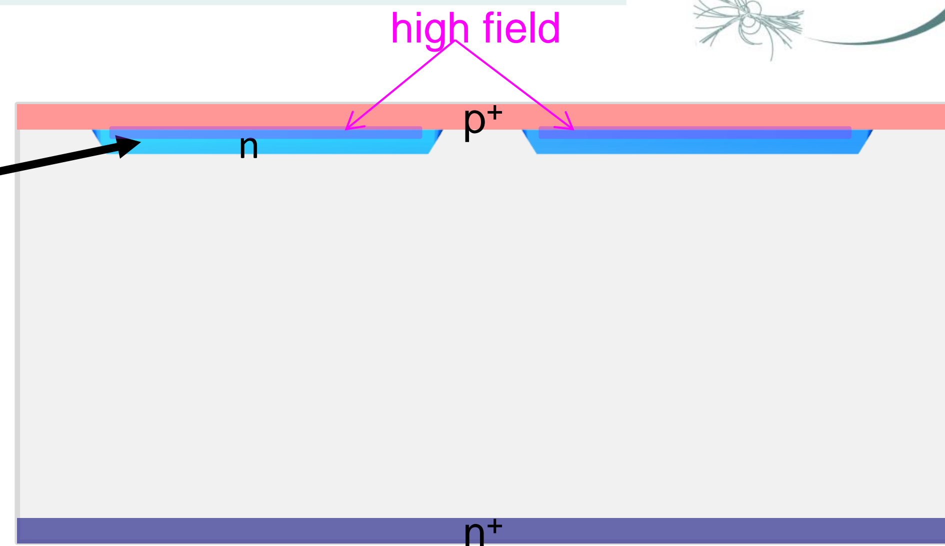




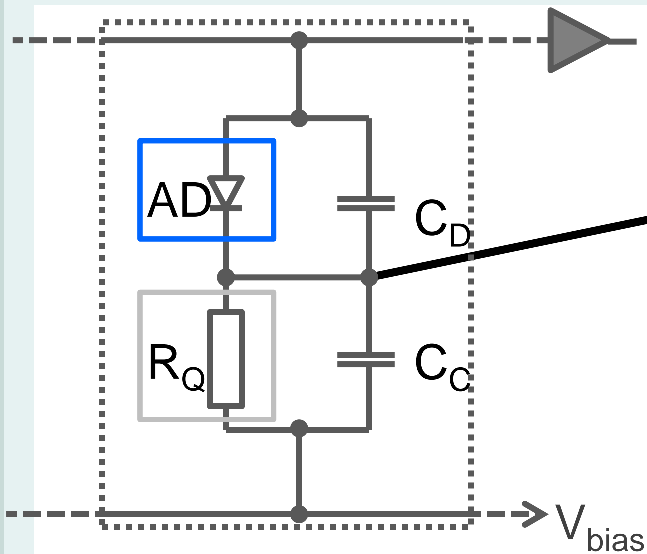
Concept developed
at
Max-Planck-Society Semiconductor Laboratory

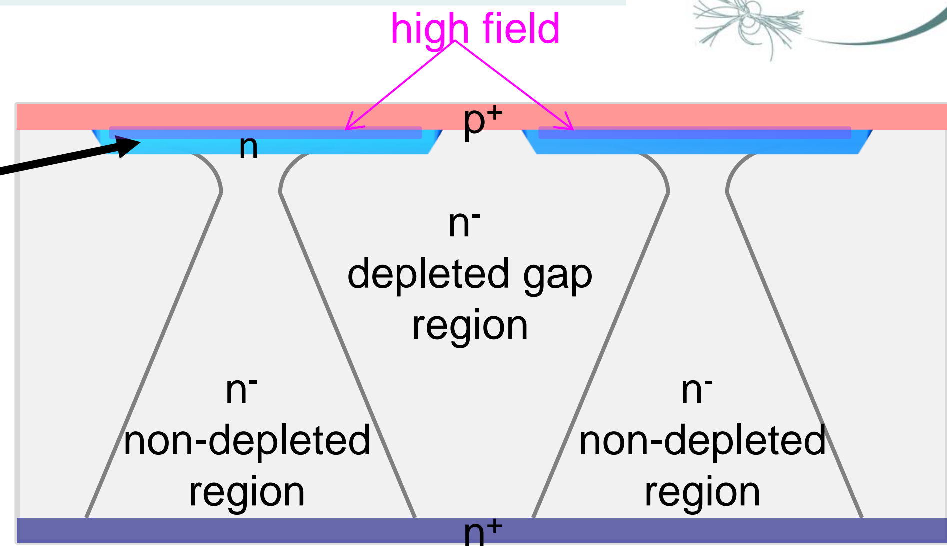
SiPM cell components → SiMPI approach



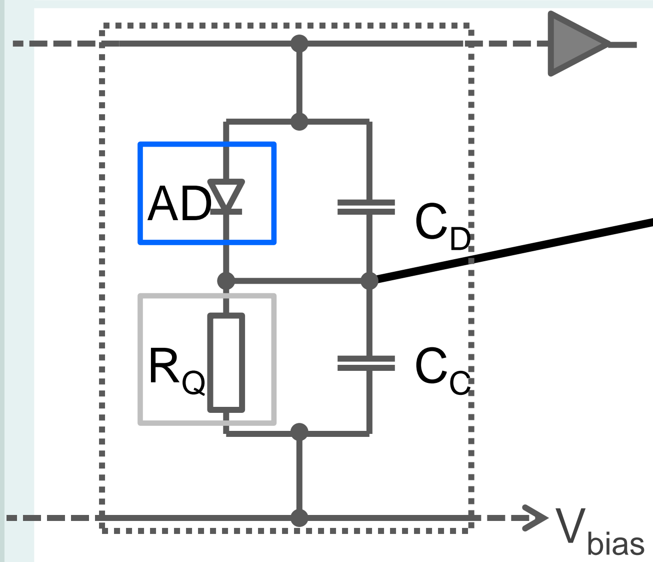


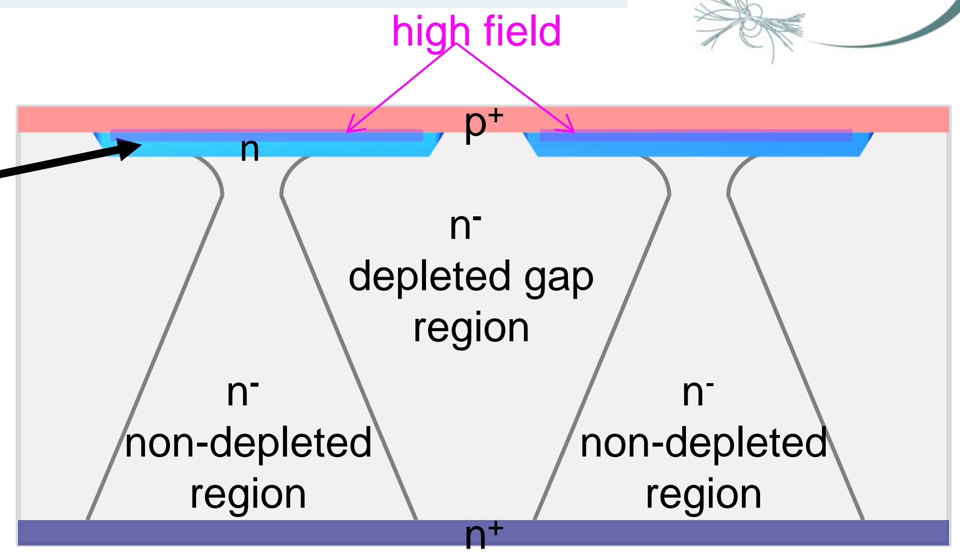
SiPM cell components → SiMPI approach



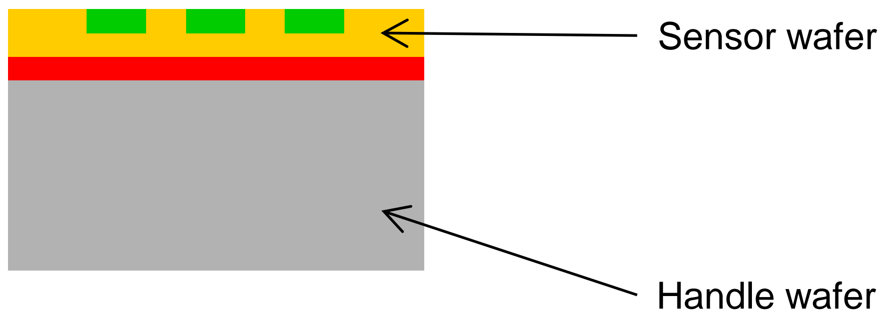


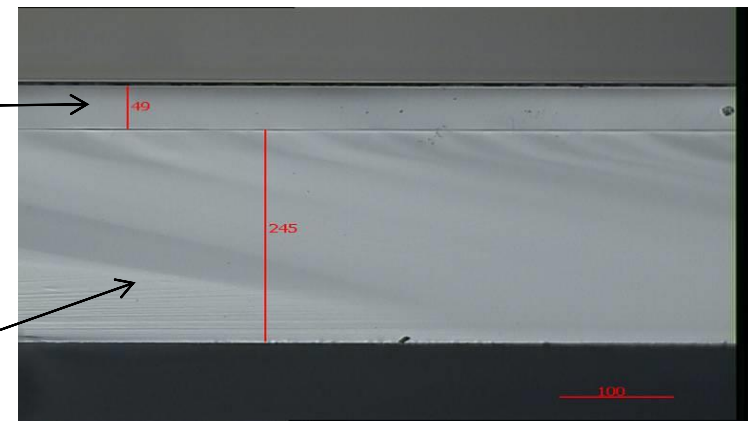
SiPM cell components → SiMPI approach





SOI wafers





Advantages and Disadvantages

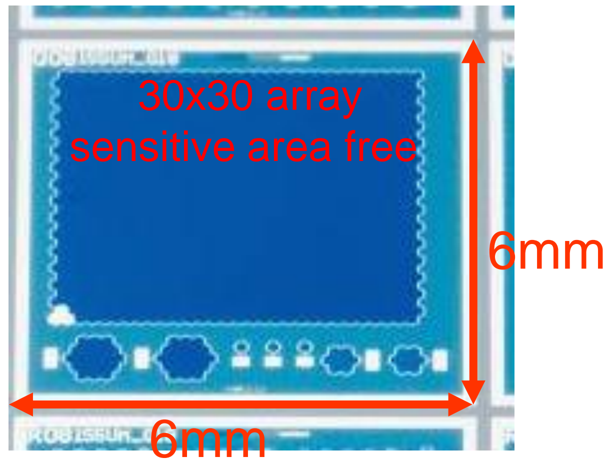
Advantages:

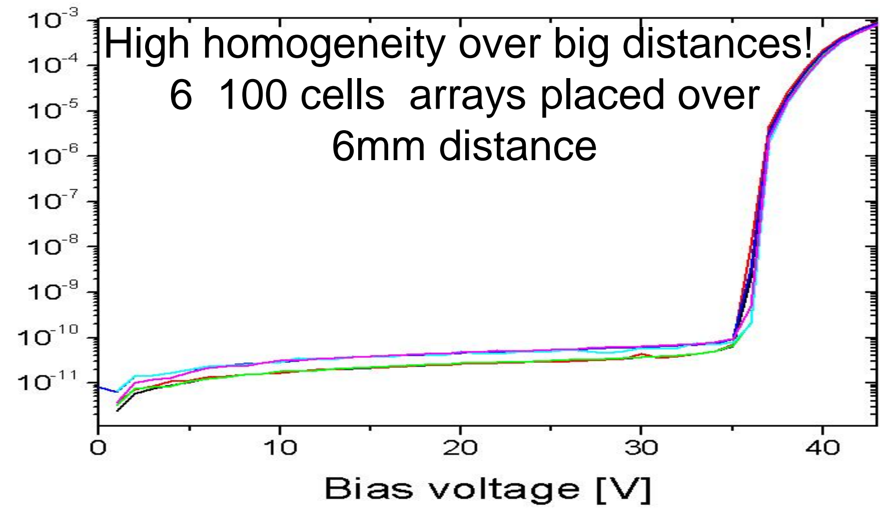
- no need of polysilicon
- free entrance window for light, no metal necessary within the array
- coarse lithographic level
- simple technology
- inherent diffusion barrier against minorities in the bulk -> less optical cross talk

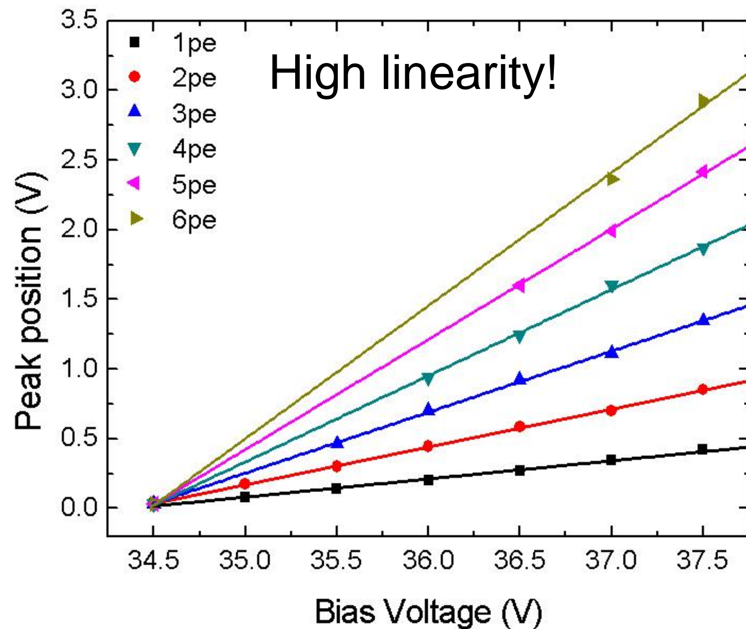
Drawbacks:

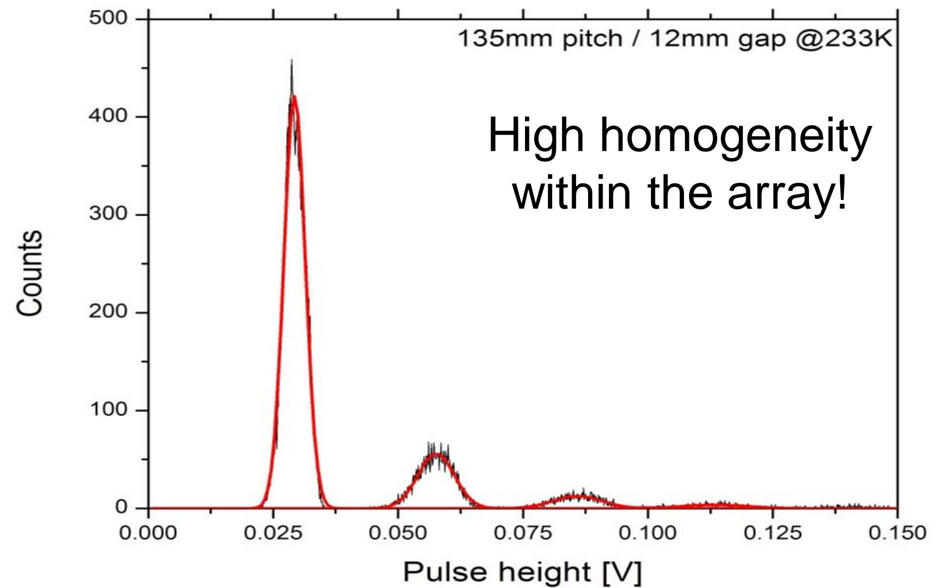
- required depth for vertical resistors does not match wafer thickness
- wafer bonding is necessary for big pixel sizes
- significant changes of cell size requires change of the material
- vertical ‘resistor‘ is a JFET -> parabolic IV -> longer recovery times

Prototype production







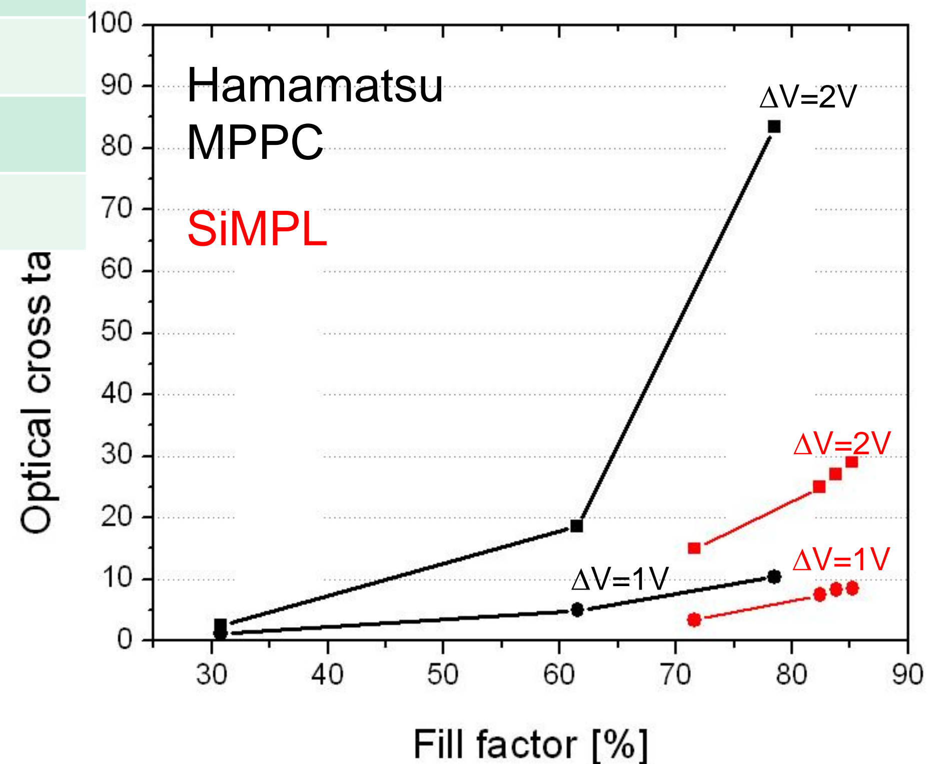


Fill factor & Cross Talk

Fill factor limited only by the cross talk suppression need!

Pitch / Gap	Fill factor	Cross talk meas. (ΔV=2V)
130μm / 10μm	85.2%	29%
130μm / 11μm	83.8%	27%
130μm / 12μm	82.4%	25%
130μm / 20μm	71.6%	15%

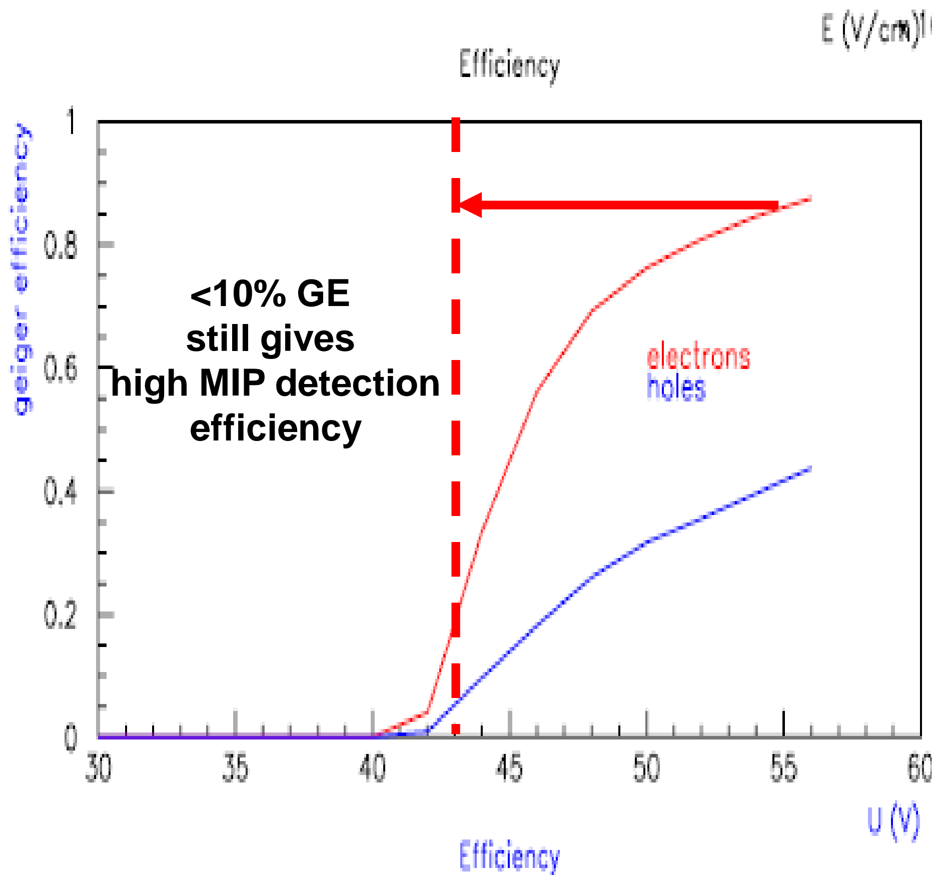
No special cross talk suppression technology applied just intrinsic property of SiMPl devices

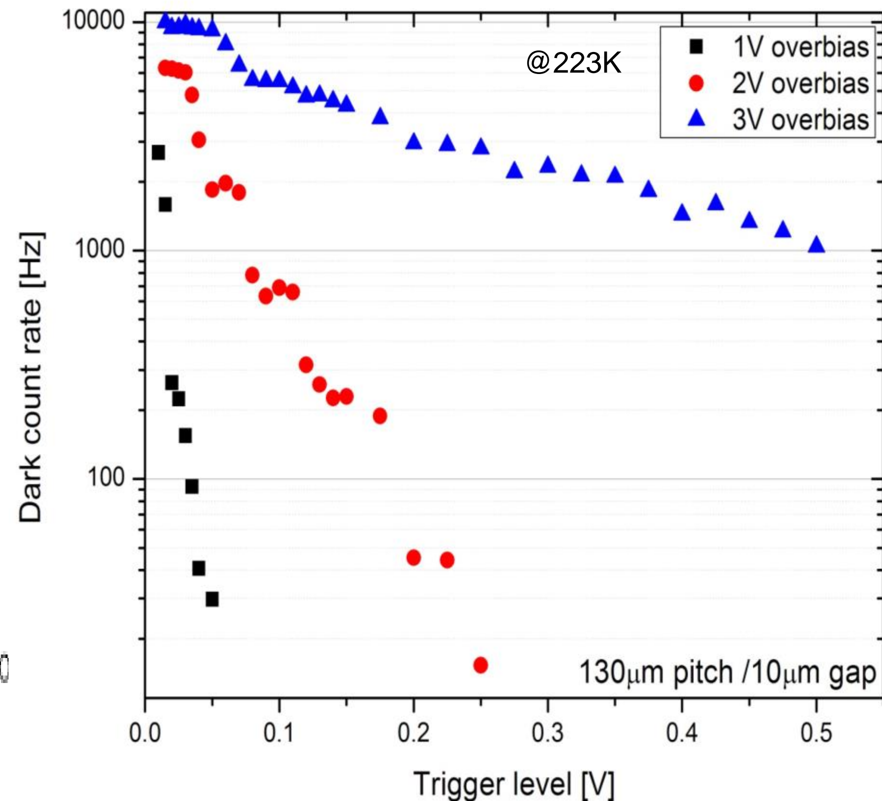


Detection of particles

Excellent time stamping due to the fast avalanche process (<1ns)

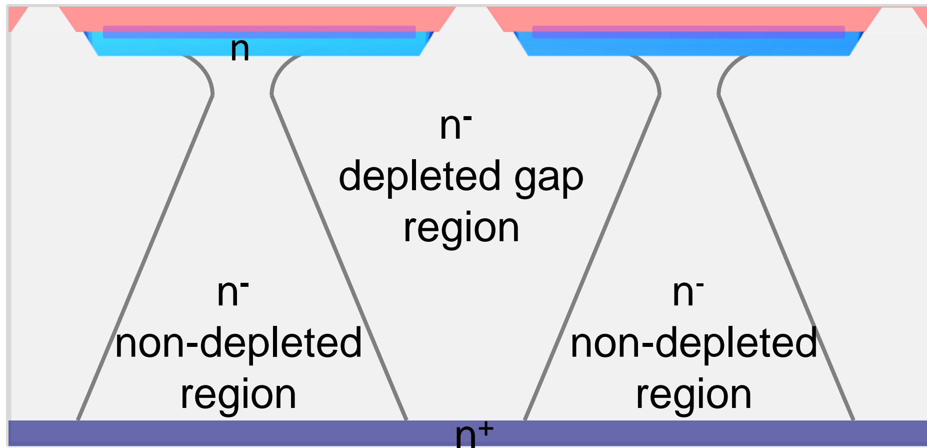
MIP gives about 80pairs/μm → huge signal in SiPM→ allows operation at small ΔV



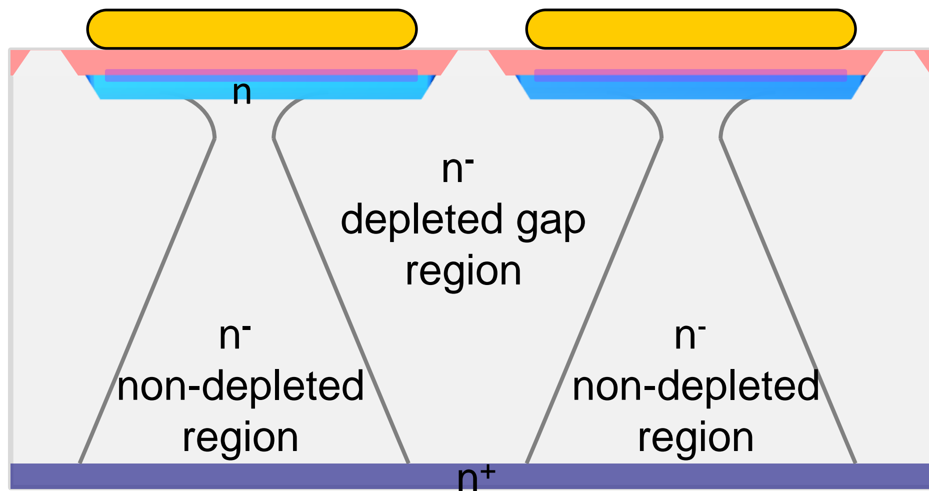


Reduction of dark rate and cross talk by at least an order of magnitude

Next generation SiMPI devices



Next generation SiMPI devices



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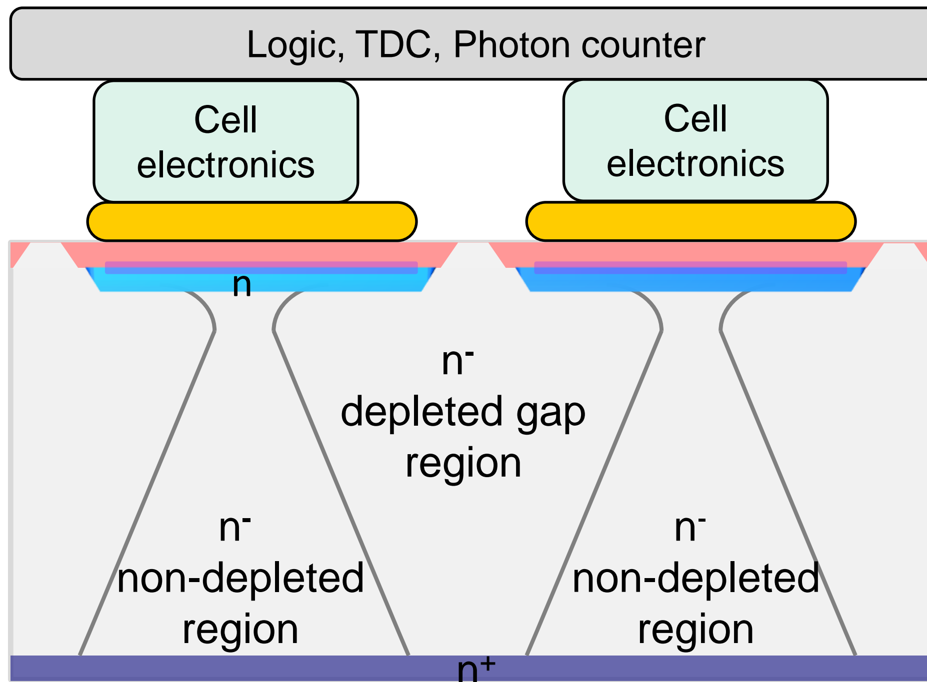


Cell electronics: Active quenching,
Bias control,
Cell activity,
Digital output

Topologically flat surface

High fill factor

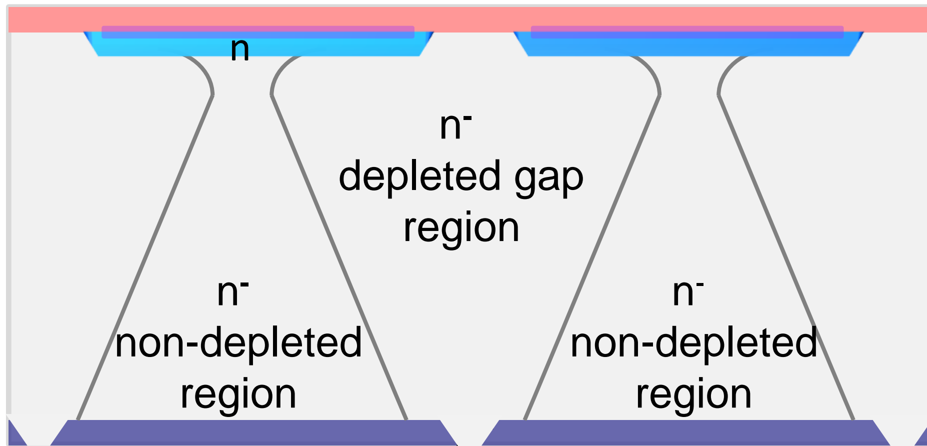
Adjustable resistor value
Low RC -> very fast

Active recharge

Ability to turn off noisy pixels

Pitch limited by the bump bonding

Next generation SiMPI devices

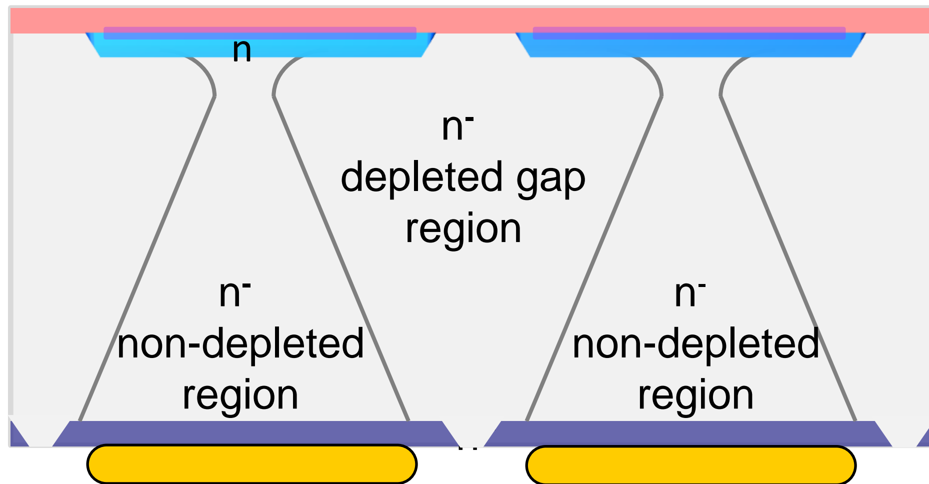


Topologically flat and free surface

High fill factor

Sensitive to light

Next generation SiMPI devices



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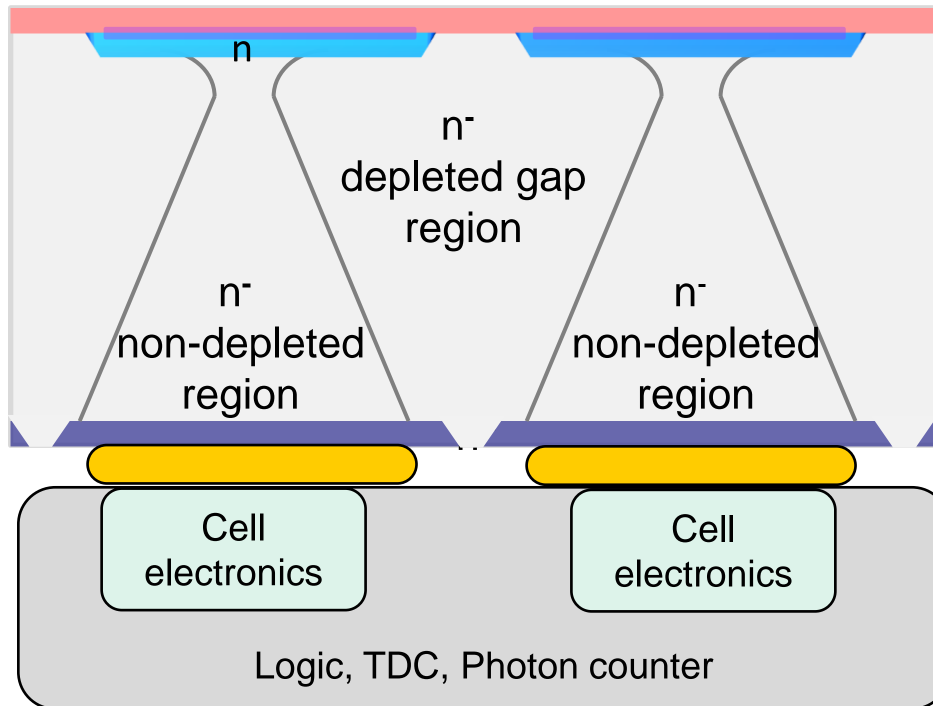

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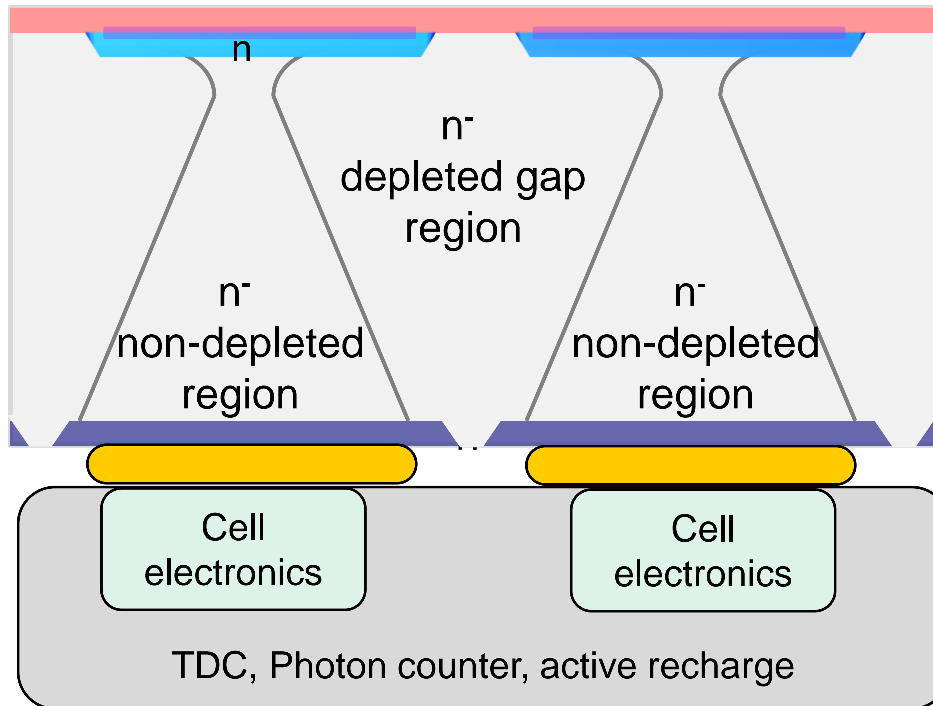


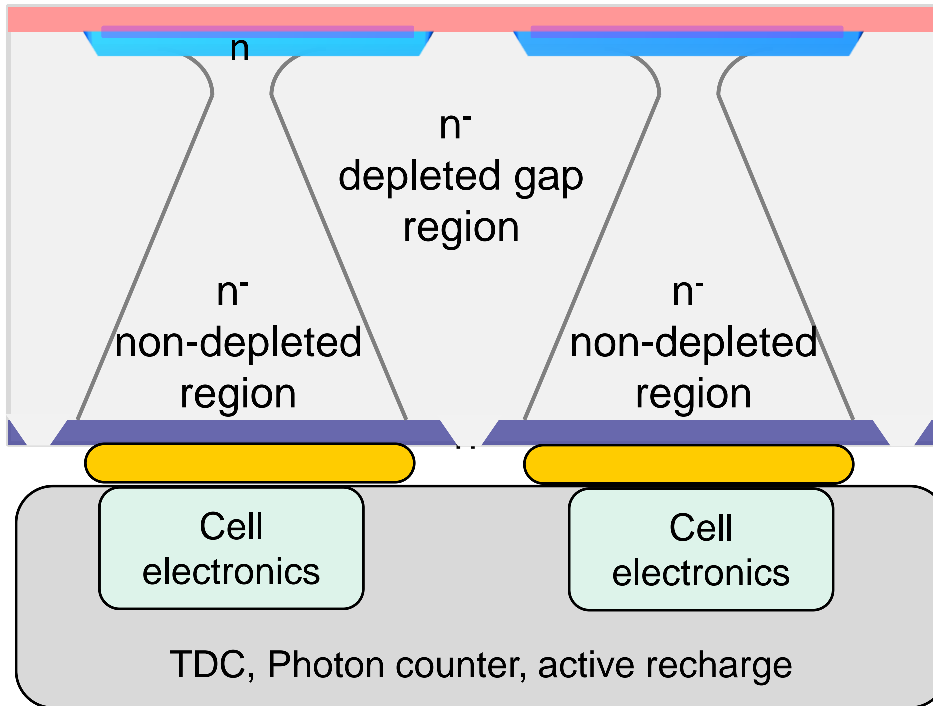
Topologically flat and free surface

High fill factor

Sensitive to light

1. Structured implant on backside on sensor wafer
2. bond sensor wafer to handle wafer
3. thin sensor side to desired thickness
4. process SiMPI arrays on top side

Next generation SiMPI devices



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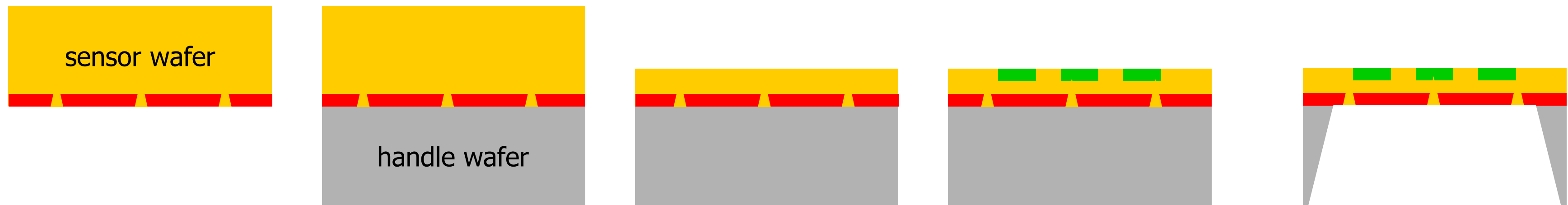

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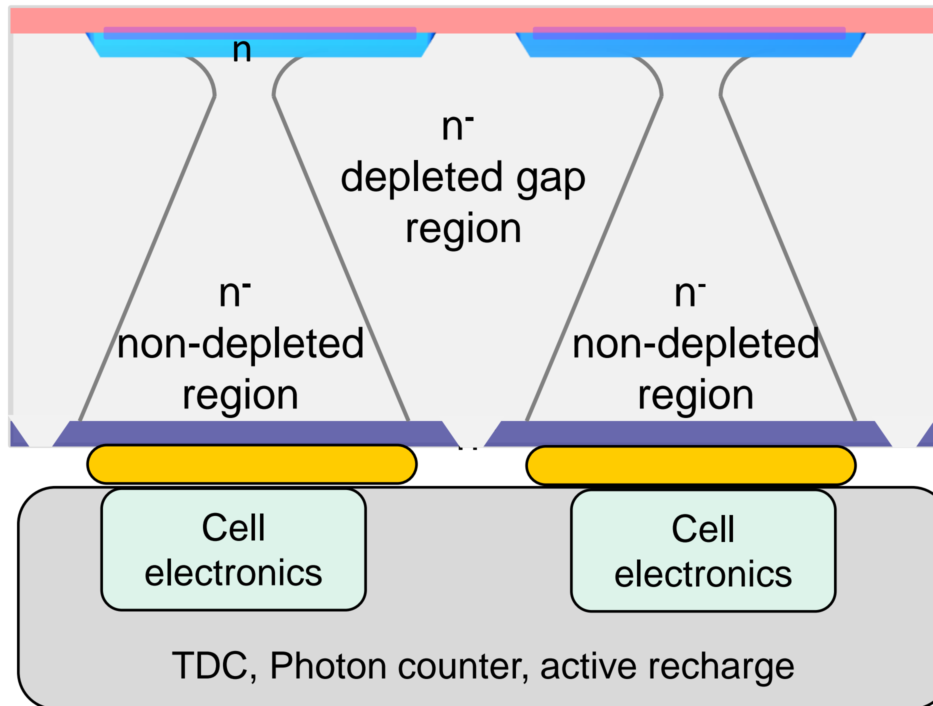

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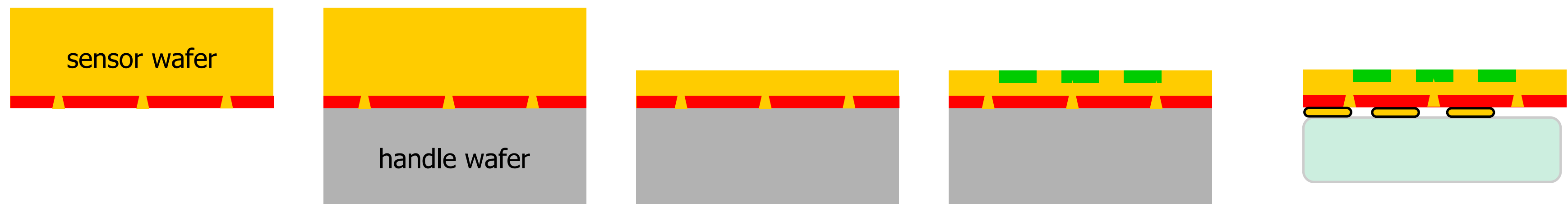

Thanks for the attention!!