Shrinking 3D ICs – Capabilities and Frontiers of Through Silicon Via Technologies

Peter Ramm

Fraunhofer Research Institution for Modular Solid State Technologies EMFT Hansastrasse 27d, 80686 Munich

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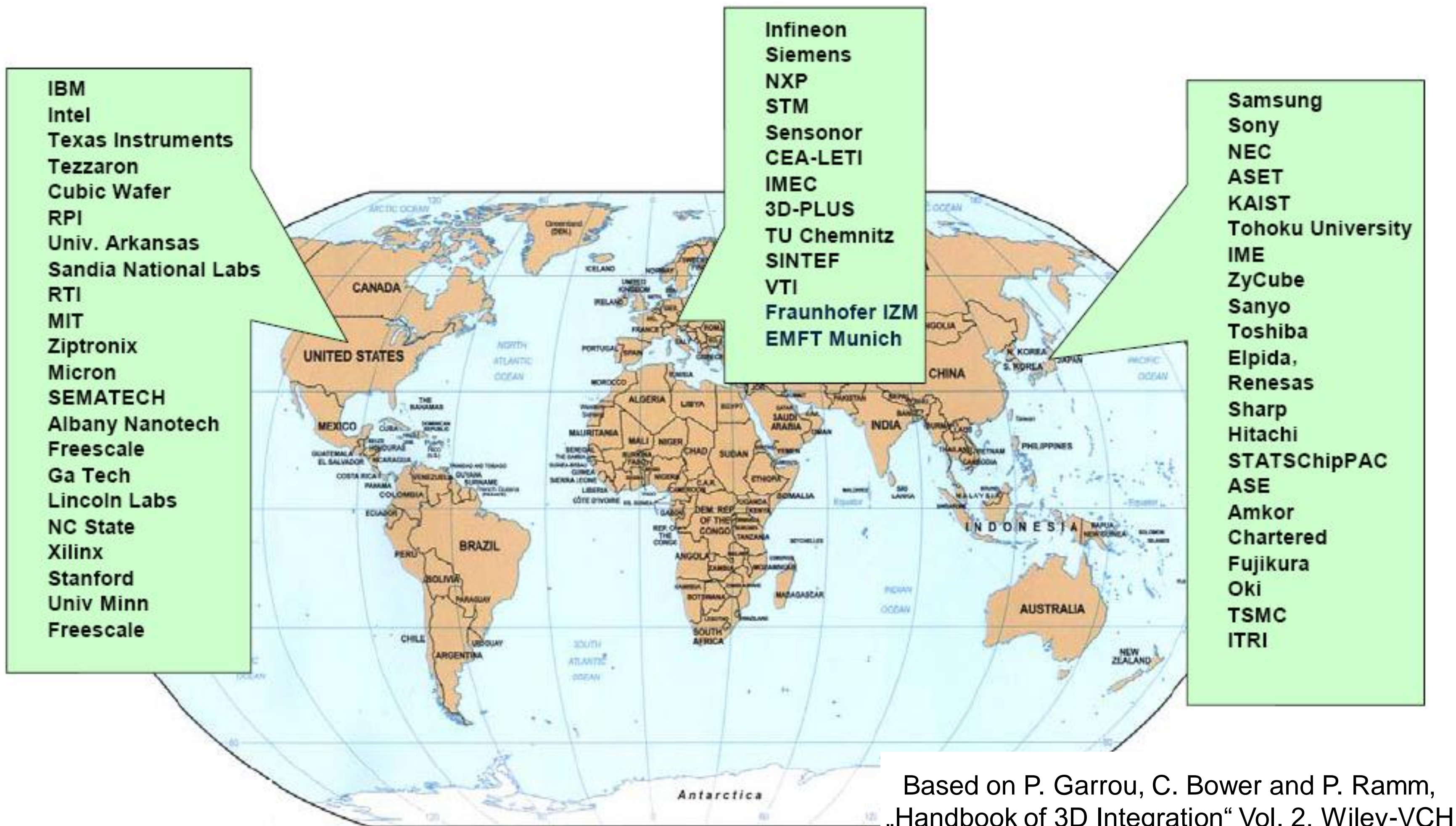
Global Activities in 3D Integration Technology



Based on P. Garrou, C. Bower and P. Ramm, „Handbook of 3D Integration“ Vol. 2, Wiley-VCH

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3D Integration

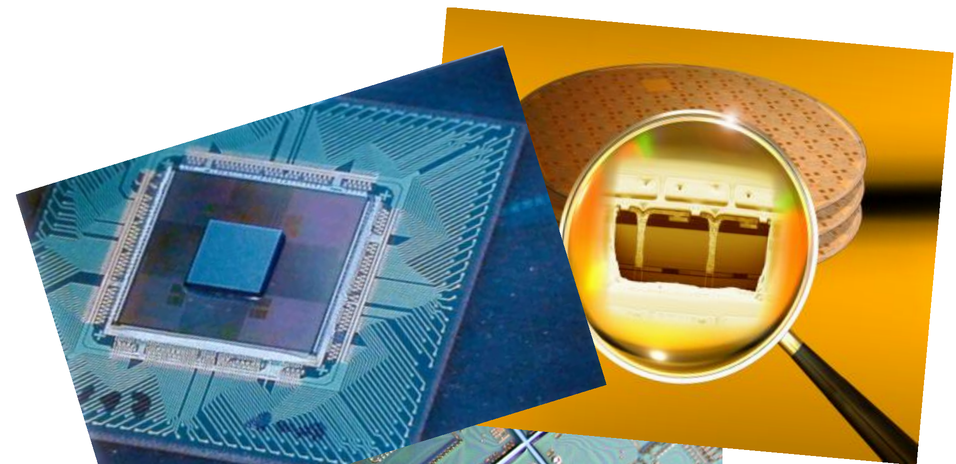
Definition:

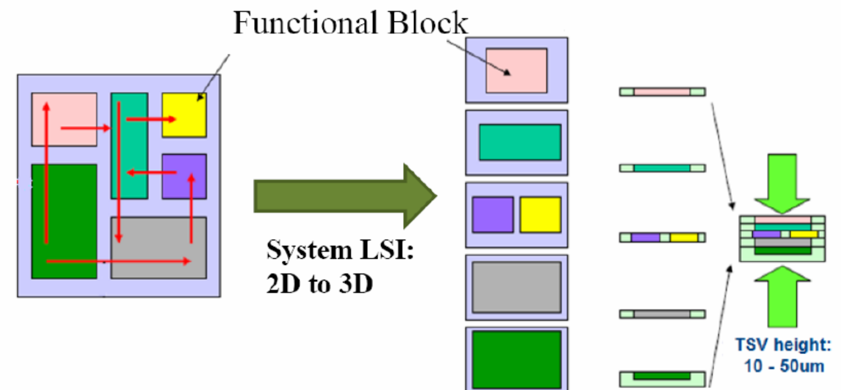
Fabrication of
stacked and vertically interconnected device layers

Motivations:

Form Factor
- Reduced volume and weight
- Reduced footprint

Performance
- Improved integration density
- Reduced interconnect length
- Improved transmission speed
- Reduced power consumption





The Ultimate Goal:
Repartitioning of Integrated Circuits

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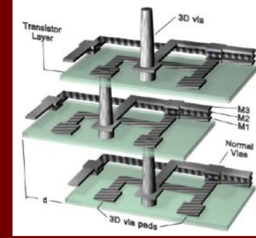
MCNC

Applications



2008 → 2010 → 2012 → 2014

→ BSI → Stacking of ROIC, DSP

CMOS Image Sensor
50 μm TSV / 50-100 μm Si

→ →

DRAM
35 μm TSV / 50 μm Si
Vias last

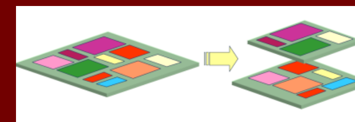
FLASH

DRAM & FLASH
< 5 μm TSV / < 20 μm Si
Vias middle

→ →

Memory on Logic
CoC no TSV / 50 -100 μm Si

Memory on Logic
5 μm TSV / 10 – 20 μm Si

→ 

Repartitioning

Ref: PFTLE 10/2008
revised 01/2010

3D Repartitioning of Logic

Main Driver: High Performance

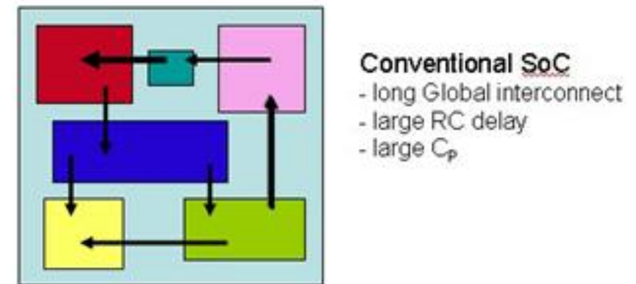
Requirements:

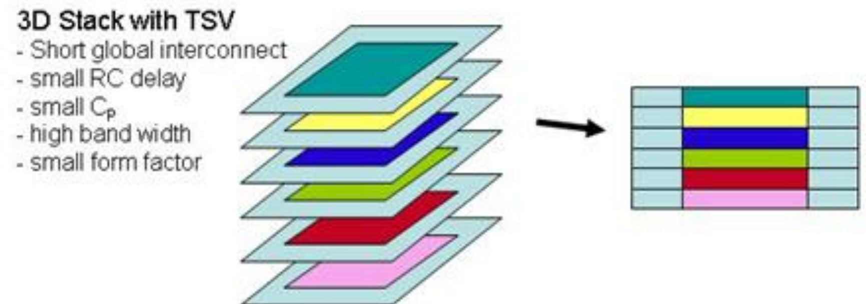
– very high density of TSVs

→ yield and cost issues

– significant advances of current design and modeling tools

– significant advances of thermal management (e.g. heat removal)





Source: P. Garrou and P. Ramm to be published in „Handbook of 3D Integration“ Vol. 3, Wiley-VCH

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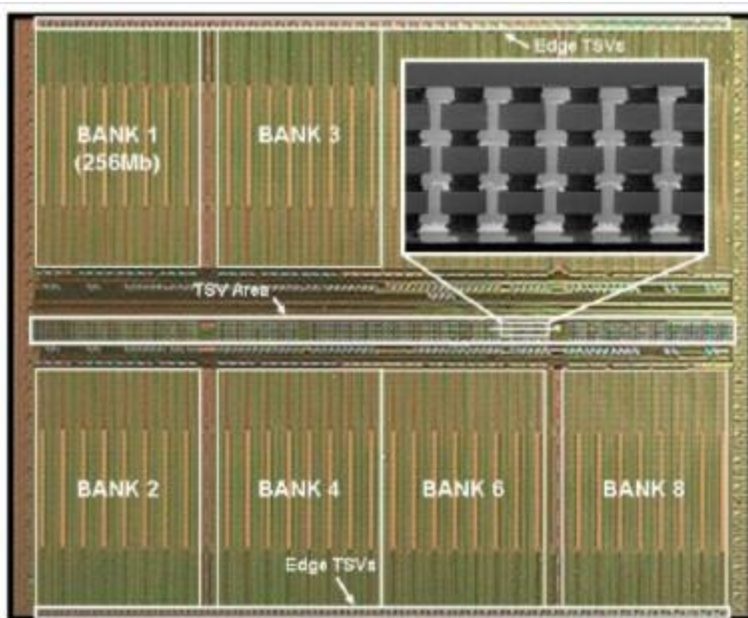
TSV Developments for Memory Stacks

Main Driver: High Performance

Shorter interconnect paths:

– higher speed

– less power consumption



Samsung:
Development of 4-die 8Gb DRAM stack
• 20-30 µm thinned dies
• 20 µm TSV diameter

Optical Micrograph of Samsung 1600 Mb/sec DDR3

Source: U. Kang, ISSCC 2009

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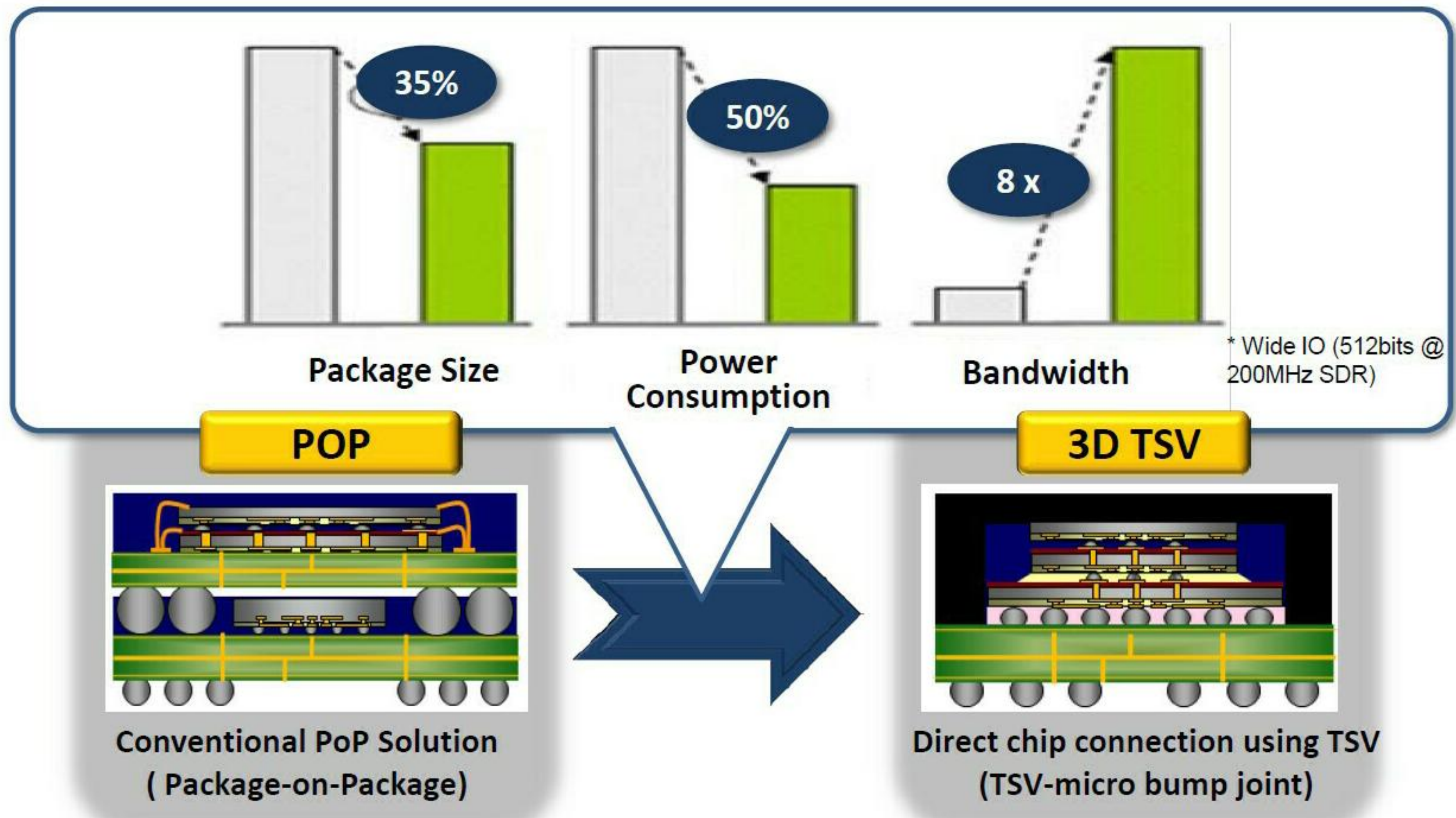
Memory on Logic for e.g. Mobile Devices



Source: Samsung "3D TSV Technology & Wide IO Memory Solutions"
Design Automation Conference, 2012

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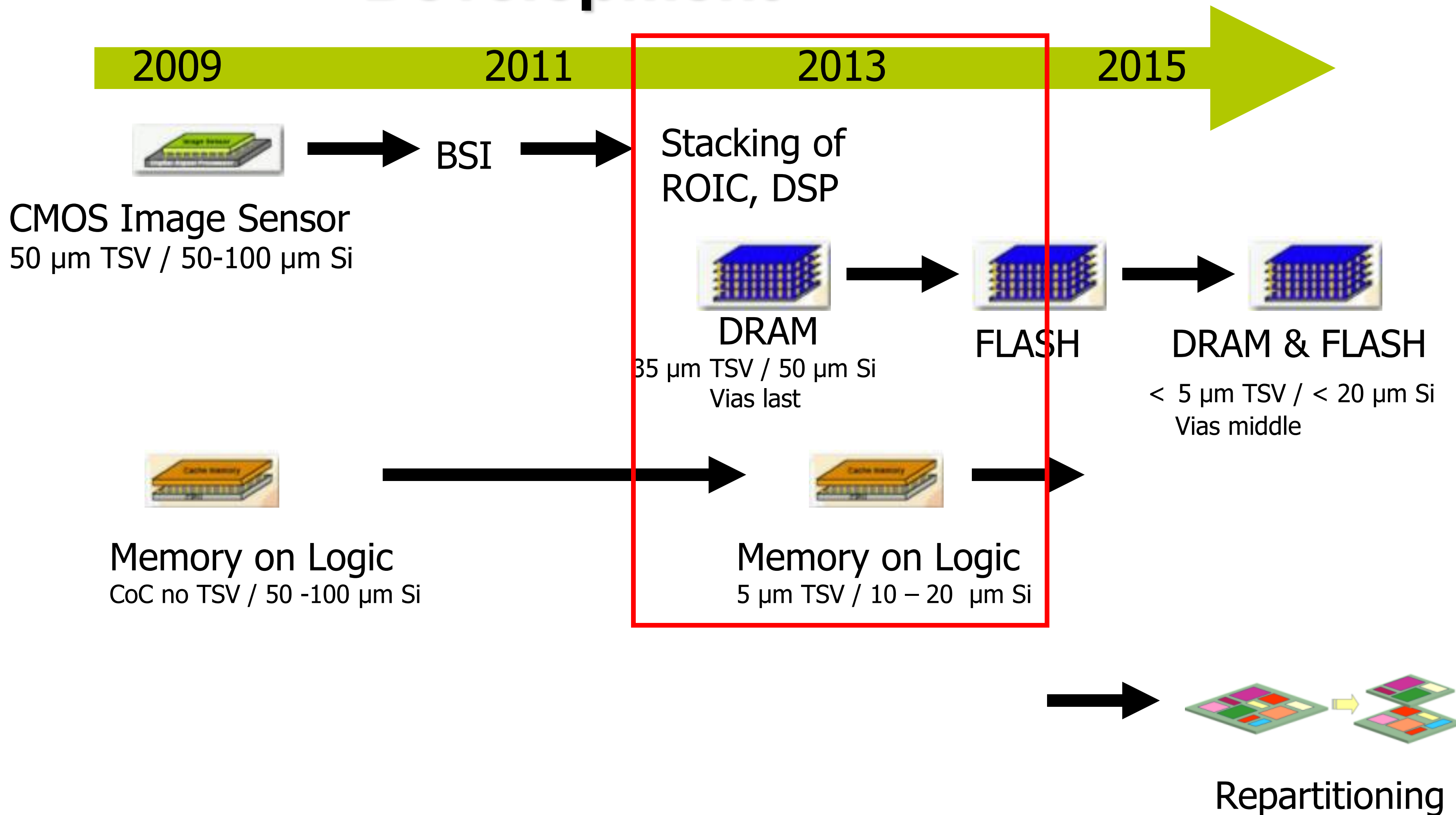
Application Development



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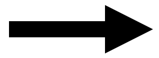
Application Development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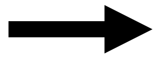
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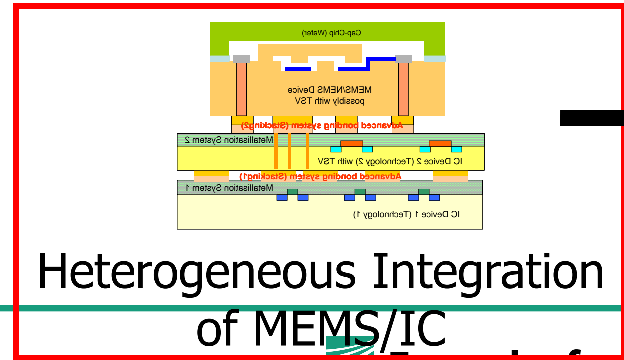

Heterogeneous Integration of MEMS/IC

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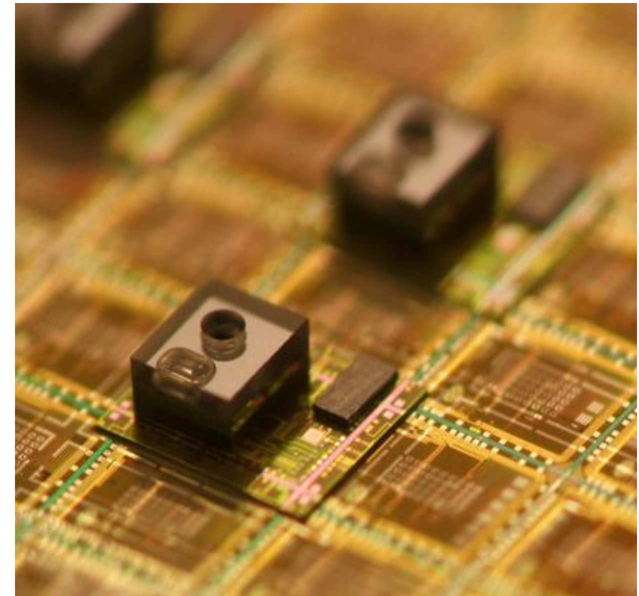
“More than Moore” Applications
- Integration of heterogeneous technologies



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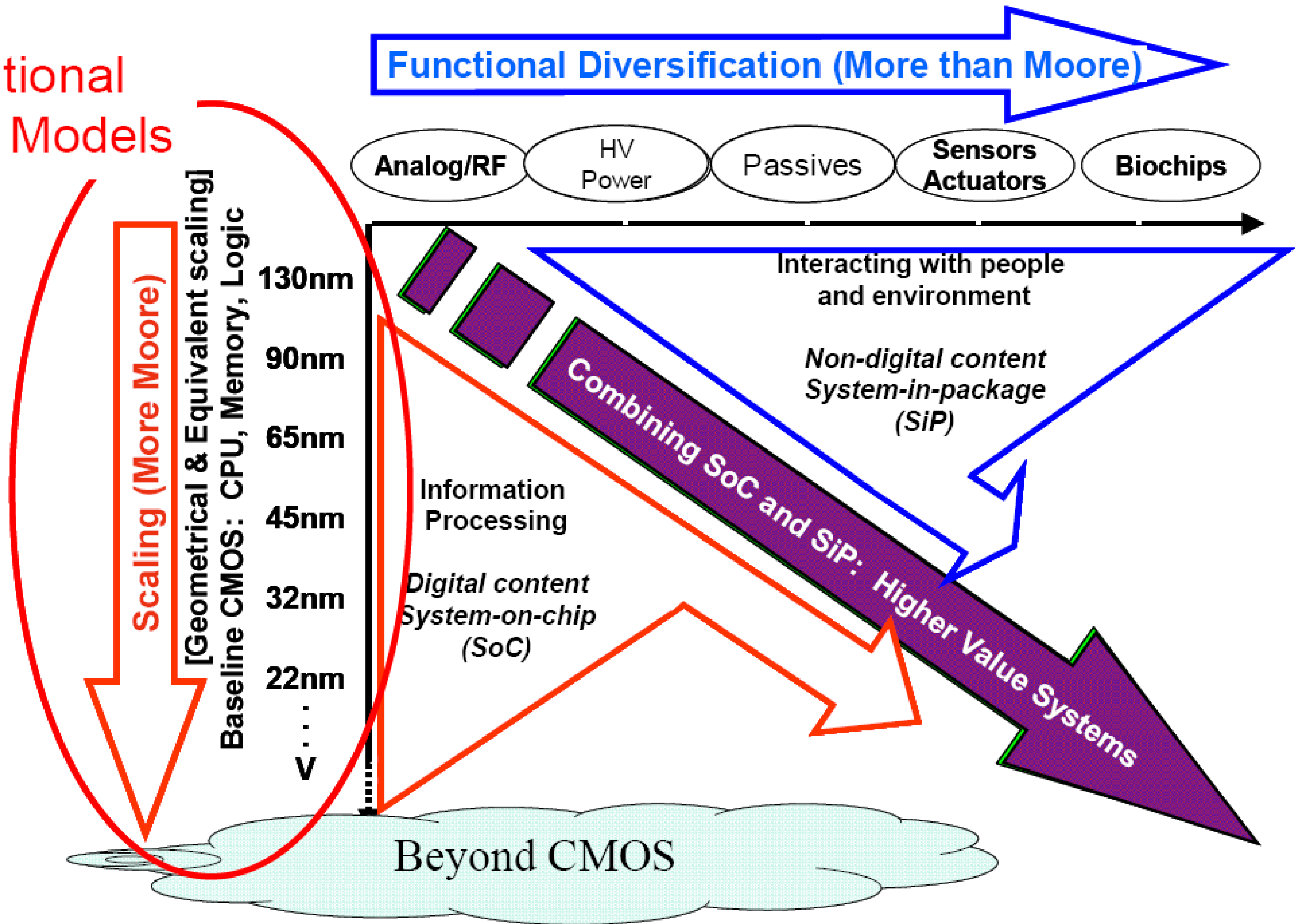
Moore's Law & More



Dr. Peter Ramm, Fraunhofer EMFT Munich

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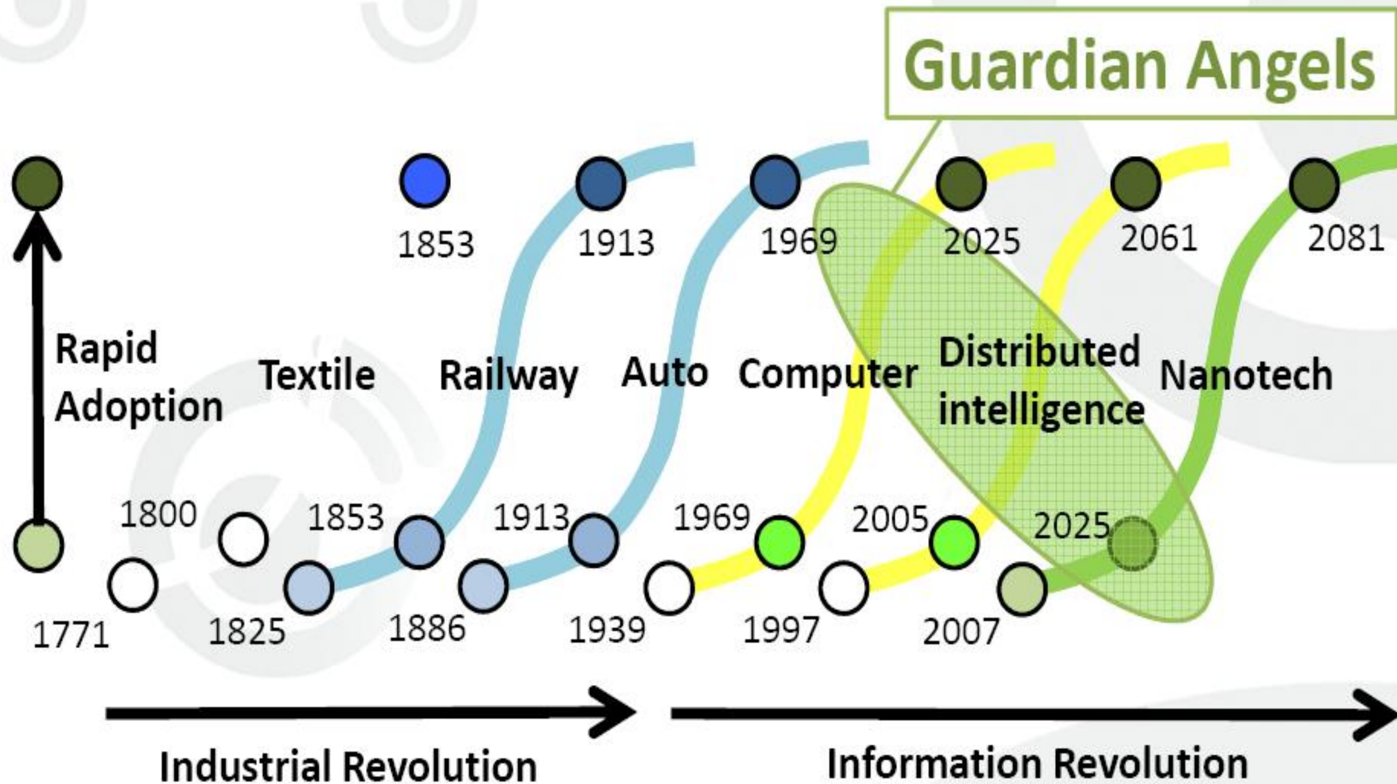
Innovation semantic waves



Guardian Angels
for a smarter life

Source: A. Ionescu, EPFL Lausanne

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3D Integration – Definitions

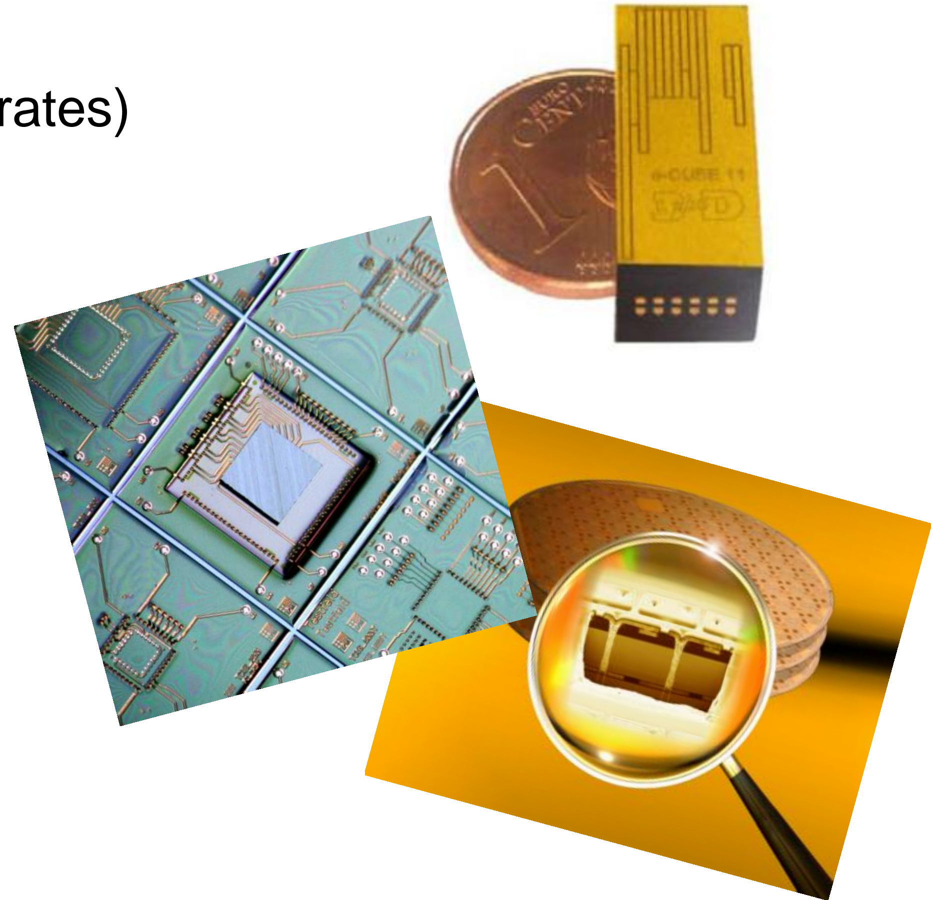
Concept Categories:

- **Stacking of packages** (or substrates) **(eq. to 3D-SIP)**

- **Stacking of embedded dies without TSVs (eq. to 3D-WLP)**

- **3D TSV Technology**

  various classifications
  - TSVs prior / post stacking
  - “via first”, “via middle”, “via last” FEOL, BEOL, post BEOL TSVs



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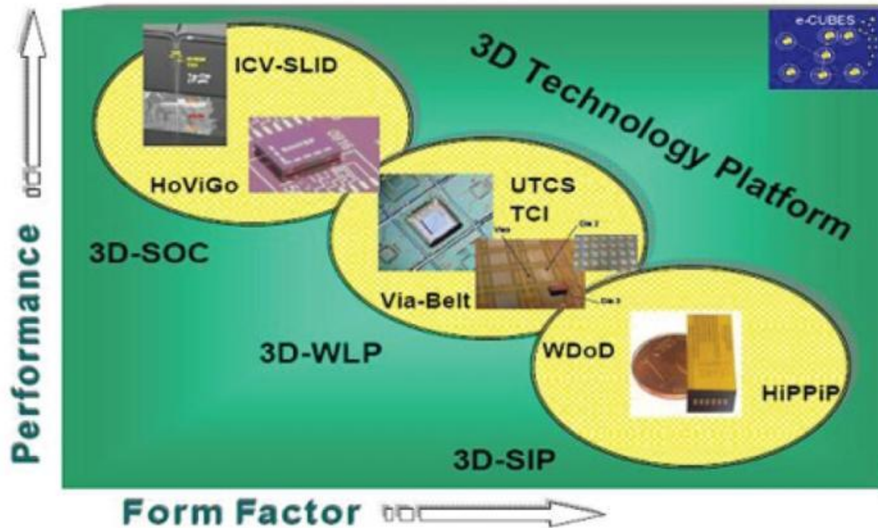
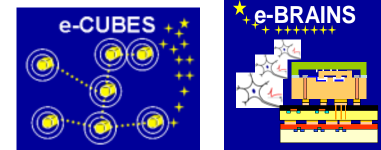
European 3D Technology Platform



Technology	e-CUBES Partner
3D-SOC	
Through Silicon Via (TSV) Technology (ICV-SLID)	Fraunhofer EMFT (formerly IZM-M)
Hollow Via & Gold Stud Bump Bonding (HoViGo)	SINTEF
3D-WLP	
Thin Chip Integration (TCI/UTCS)	Imec and Fraunhofer IZM & EMFT
Via Belt Technology Chip-in-Polymer and µInsert)	CEA-Leti
3D-SIP	
High Performance Package-in-Package Technology (HiPPiP)	3D-PLUS
Wirefree Die-on-Die Technology (WDoD)	3D-PLUS
Submicron Wire Anisotropic Conductive Film Assembly (SW-ACF)	Tyndall

Futue Fab International, Issue 34 (July 2010)
“The European 3D Technology Platform (e-CUBES)”
P. Ramm, A. Klumpp, J. Weber, M. Taklo, N. Lietaer, W. De Raedt, T. Fritzsch,
T. Hilt, P. Couderc, C. Val, A. Mathewson, K. M. Razeeb, F. Stam



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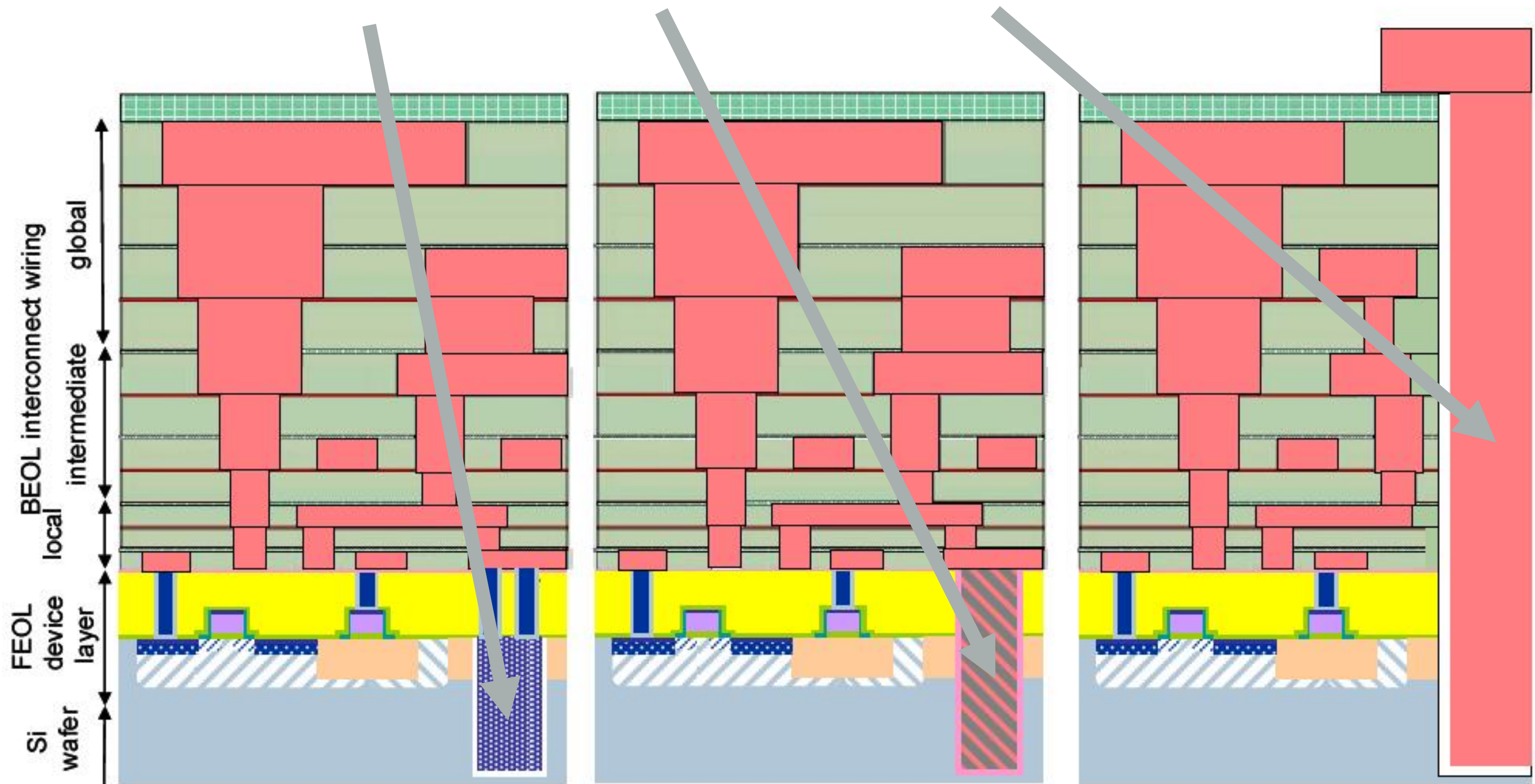
Via First, Middle and Last Process Flows



Semiconductor Industry Association,
"The International Technology Roadmap for Semiconductors",
2011 Edition.SEMATECH:Austin, TX, 2011

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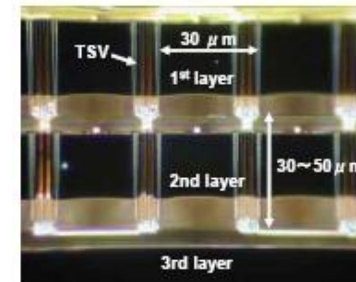
3D Integration – Definitions (ITRS)

3D TSV Technology

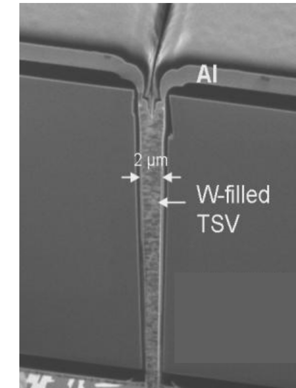
- **3D-IC**

  3D Integrated **C**ircuit: stacking of transistor layers
  (3D connections at density level of local interconnects)

Source: Honda



Source: EMFT



- **3D-SIC**

  3D Stacked **I**ntegrated **C**ircuit
  (very high TSV densities)

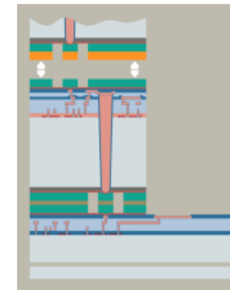
Table INTC8 Intermediate Interconnect Level 3D-SIC Roadmap

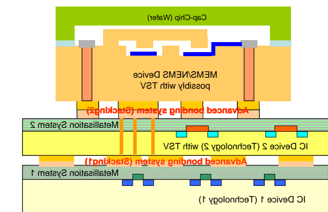
Intermediate Level, W2W 3D-stacking	*2011-2014*	*2015-2018*
Minimum TSV diameter	1-2 µm	0.8-1.5µm
Minimum TSV pitch	2-4 µm	1.6-3.0 µm
Minimum TSV depth	6-10 µm	6-10 µm
Maximum TSV aspect ratio	5:1 – 10:1	10:1 – 20:1
Bonding overlay accuracy	1.0-1.5 µm	0.5-1.0 µm
Minimum contact pitch	2-3 µm	2-3 µm
Number of tiers	2-3	8-16 (DRAM)

Source: ITRS 2011 Edition

- **3D-SOC**

  3D System-**O**n-**C**hip: stacking of devices or large IC blocks (global level)
  - ➢ **Fabrication of Heterogeneous Systems**





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Source: ITRS 2011 Edition

CVD of
- **Cu**
- **W**
- TiN

PVD of Seedlayer
- Ti:W / Cu

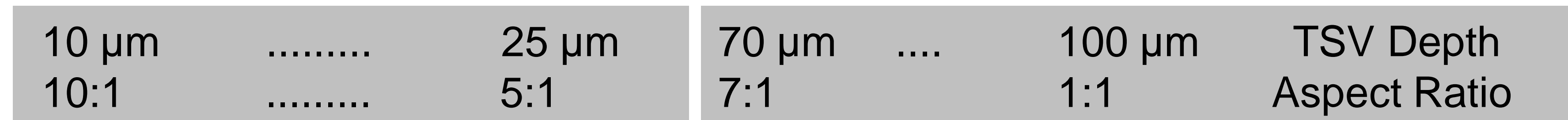
& **Electroplating of**
- **Cu**

PVD Barrier & Cu Liner-ECD

CVD of Seedlayer
- tungsten

& **Electroplating of**
- **Cu**

Polymer Isolation & Paste Fillling



electroless Seedlayer & Cu-ECD

Based on: Handbook of 3D Integration, Wiley edited by P. Garrou, C. Bower and P. Ramm

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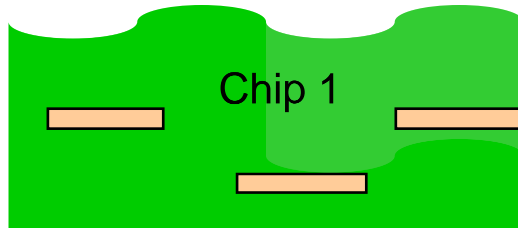
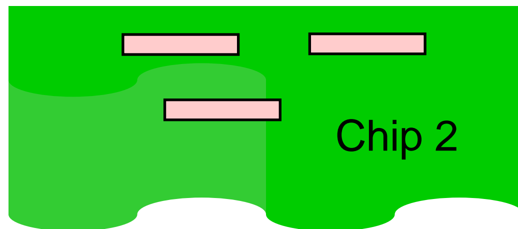
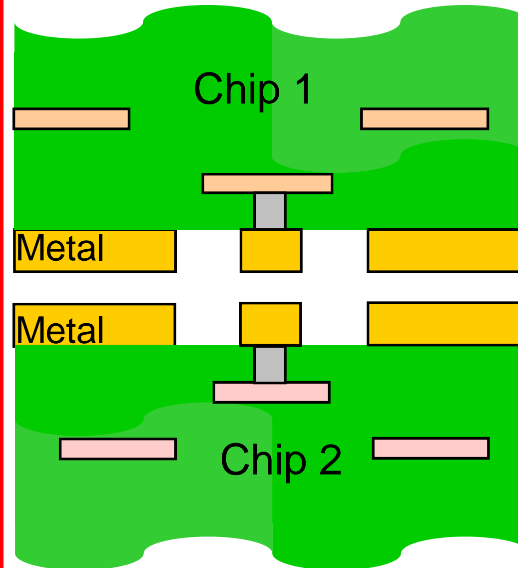
Permanent Bond Technologies for 3D Integration

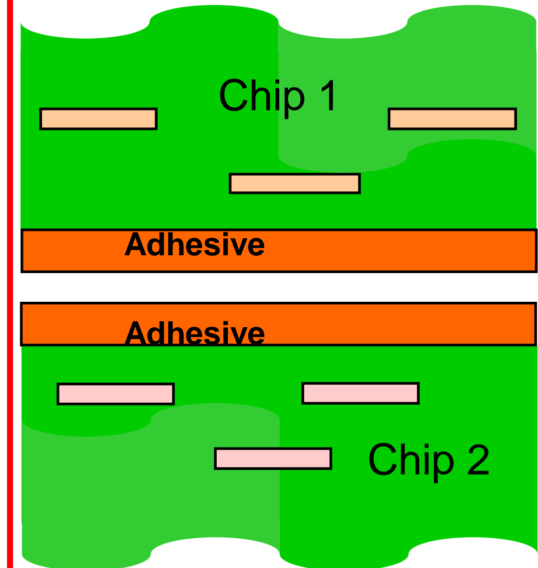




Direct Oxide Bonding



Direct Metal Bonding



Adhesive Bonding

Via Last
Low temperature/pressure
High sensitivity to defects
High flatness/roughness requirements

Via First and Via Last

Cu–Cu, Au–Au, …
Intermetallic Compounds (IMC)

Via Last
Medium temperature/pressure
Defect tolerant
Low flatness/roughness requirements

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Cu - Cu Fusion Bonding: Ziptronix

Roughness (RMS < 1.0 nm)

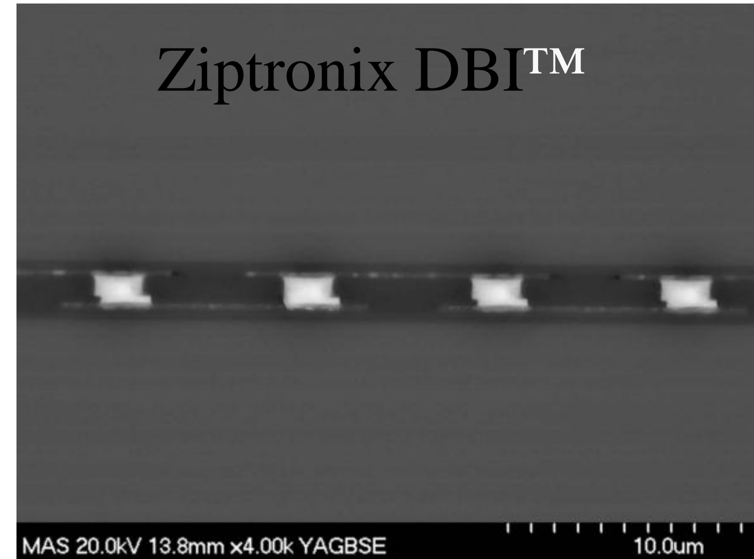
Cleanliness (no particulate)

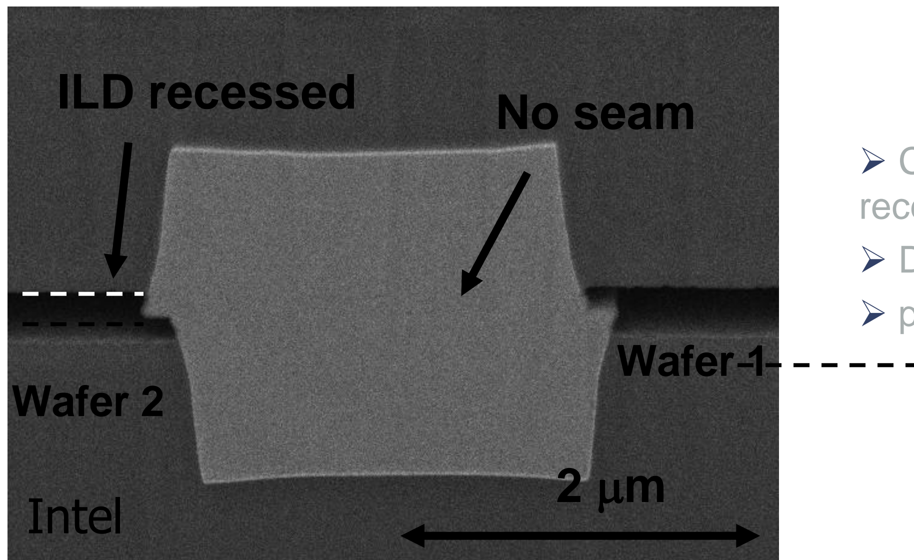
Flatness (< 4 µm / 200 mm wafer)

Bonding Conditions = 400 °C / 30 min

Contact Pressure = 4000 mBar

Post-Bonding Anneal: 400°C / 30 min





- CMP simultaneously polishes metal and SiO2 - no ILD recess
- D2W or W2W oxide (ZiBond®) bond at ambient T & P
- post-bond Cu-Cu bond formation in oven anneal

Source: P. Garrou / MCNC

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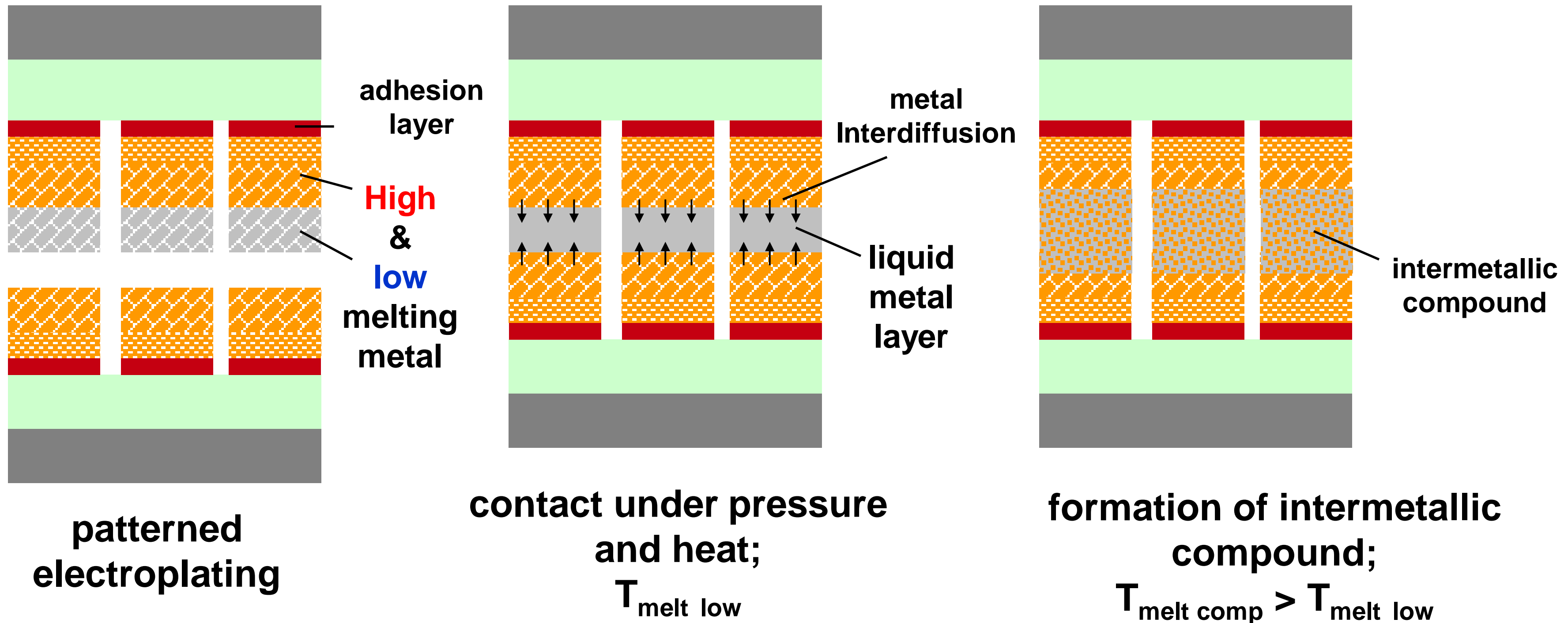
SLID Bonding (Solid Liquid Interdiffusion)

Thermal management of dissipated power -> no polymeric underfiller



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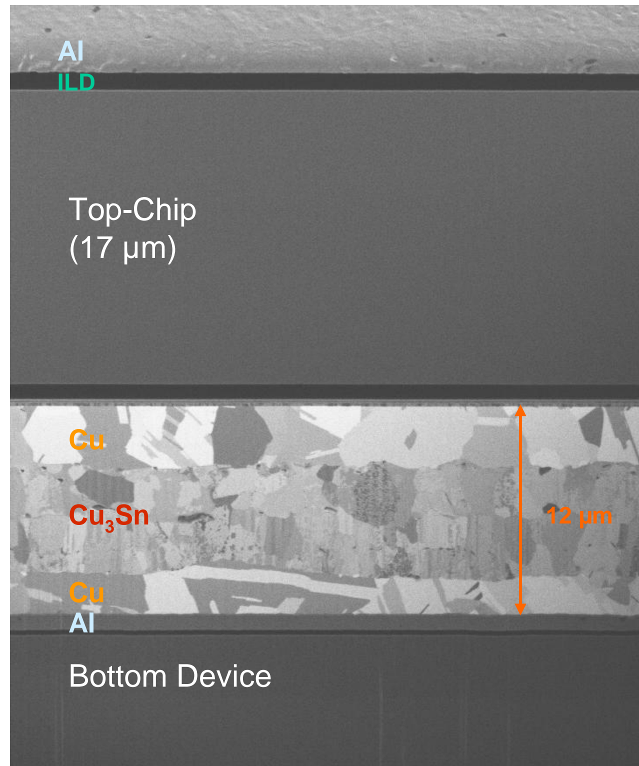

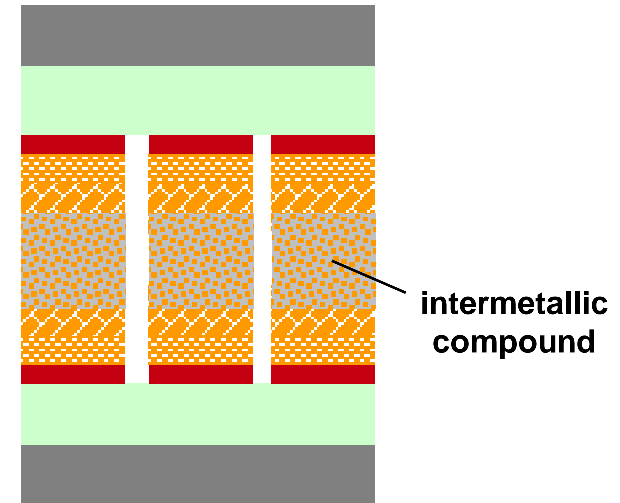

formation of intermetallic compound;
$T_{melt\ comp} > T_{melt\ low}$

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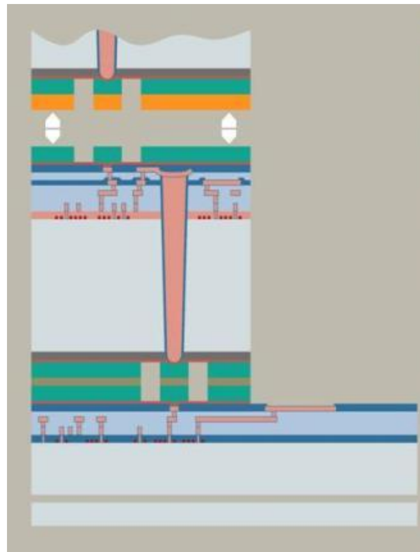
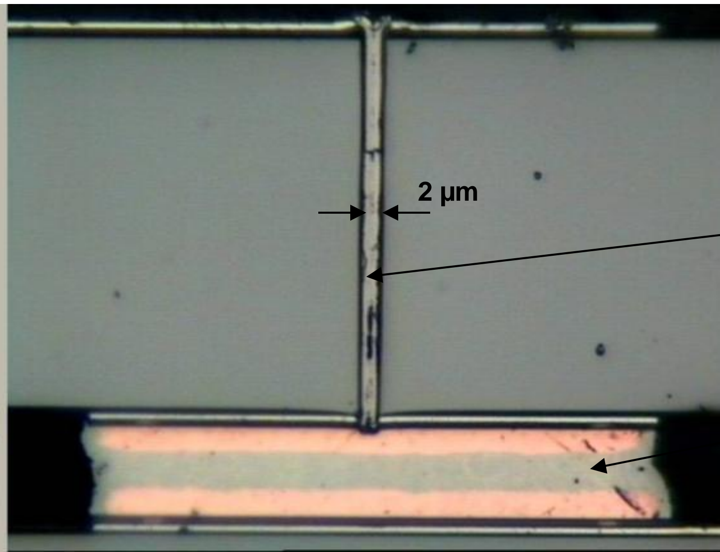
TSV-SLID – a robust 3D TSV Technology





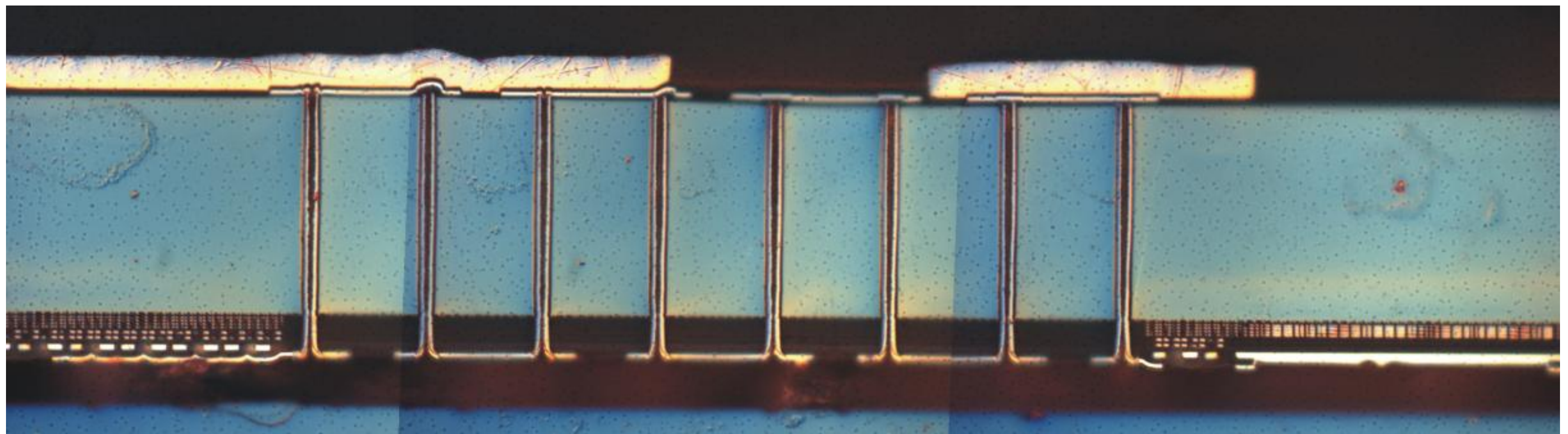
Source: Fraunhofer EMFT Munich

CVD-W

Cu_3Sn SLID

ASIC (7-level metallization)
Process control module (PCM)

Daisy chains in PCM



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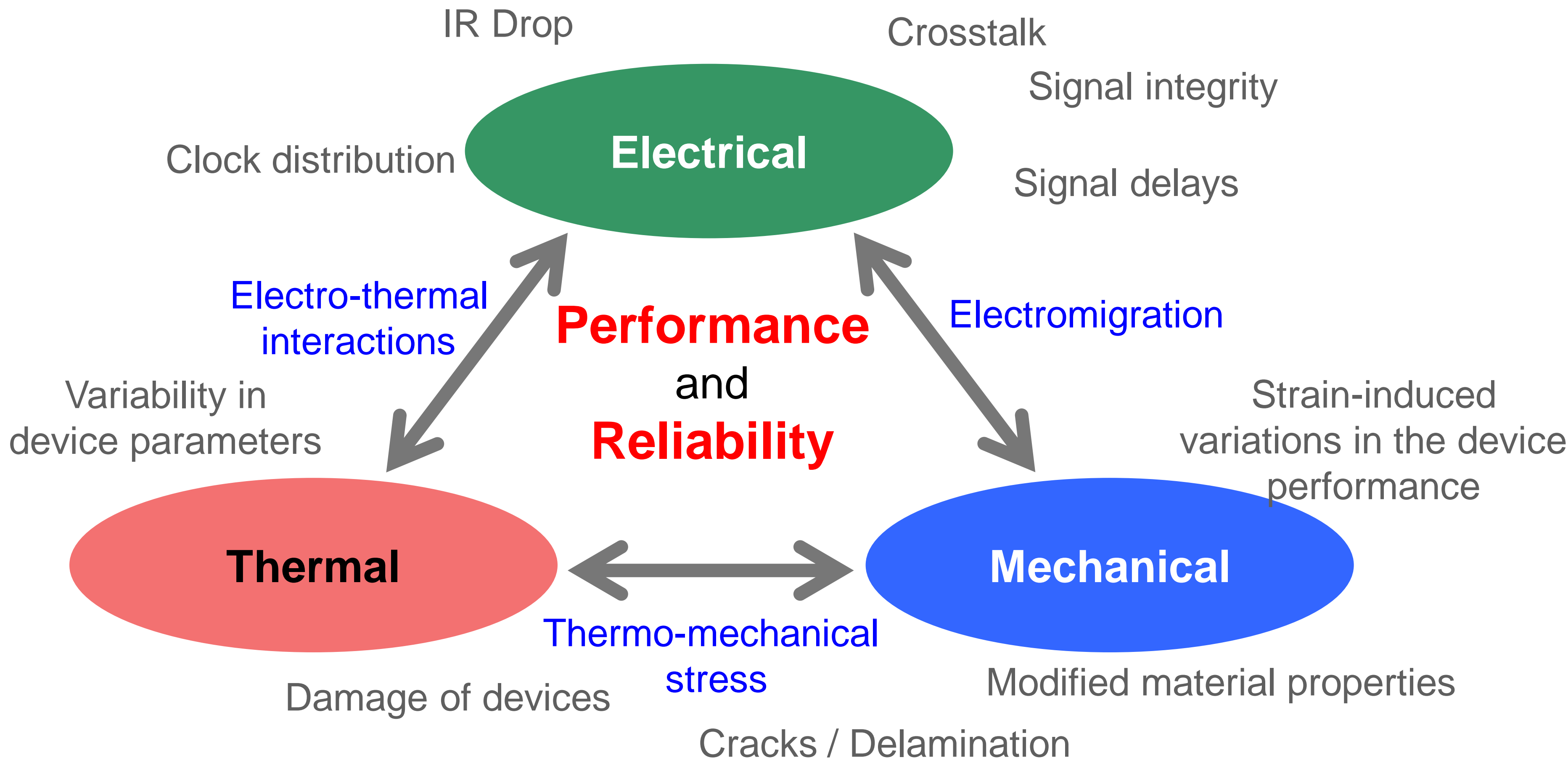
3D Integration – Impact on System



Based on: A. Wilde, P. Schneider, P. Ramm, DTC 2010

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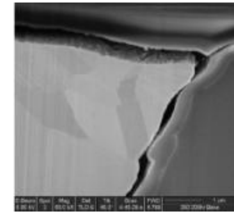
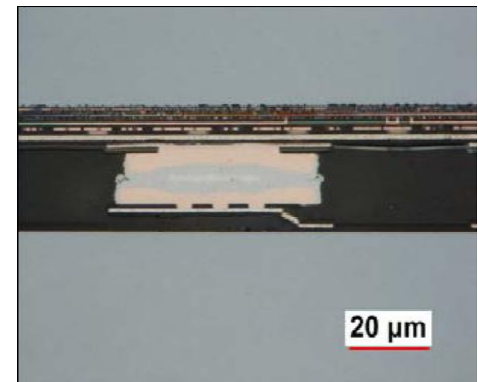
3D TSV Fabrication Issues

- IC degradation caused by TSV technology
  - Stress induced
  - Contamination induced (TSV, backside RDL)

- Electrical behavior and reliability of TSV
  - Electromigration
  - Damage / delamination



- Reliability of interconnect pads & RDL
  - Stress caused by device fabrication
  - Stress caused by assembly / bonding process
  - …



- Thermal management
- Testability of subsystems

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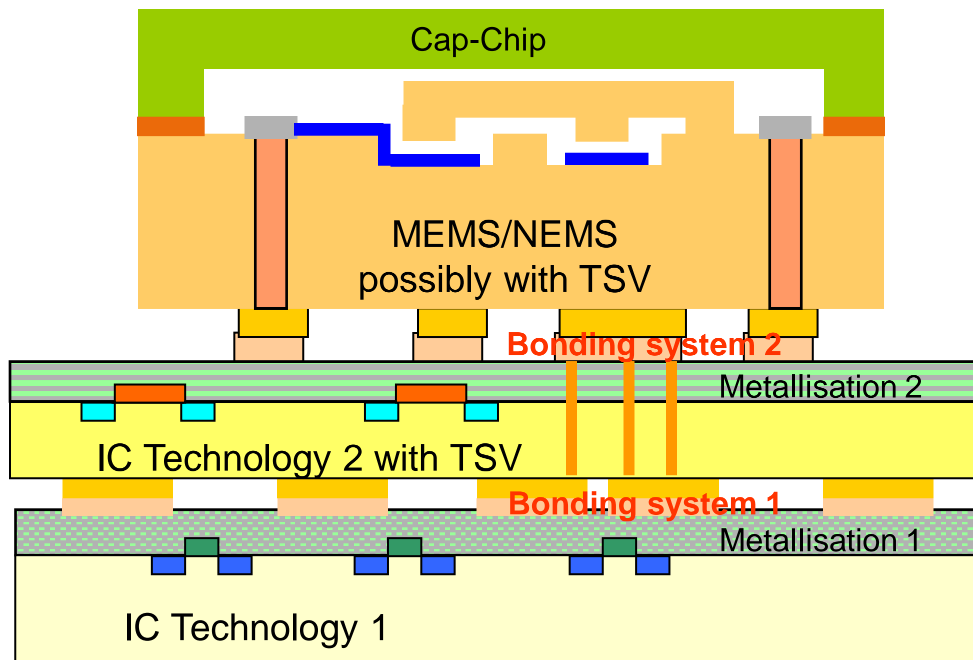
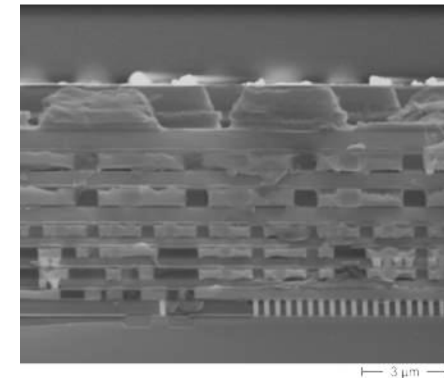
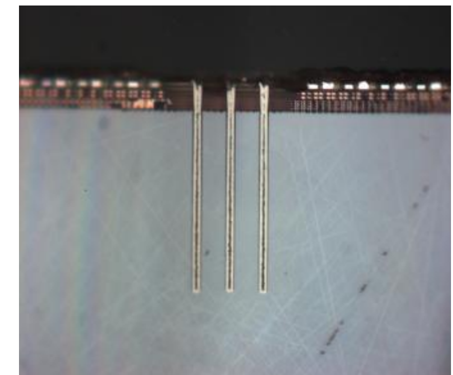
3D MEMS/NEMS & IC Integration – a Challenge!

Heterogeneous integration partly based on completely fabricated devices
→ Application of **post-BeoL TSV technology** ?
→ Data on ILD and passivation layers required







Issues for **reproducibility and reliability:**
- Fragile mechanical structures in MEMS/NEMS devices
- Stress induced by **TSVs** and **bonding system** of thin devices

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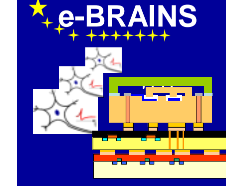


European Integrated Project e-BRAINS

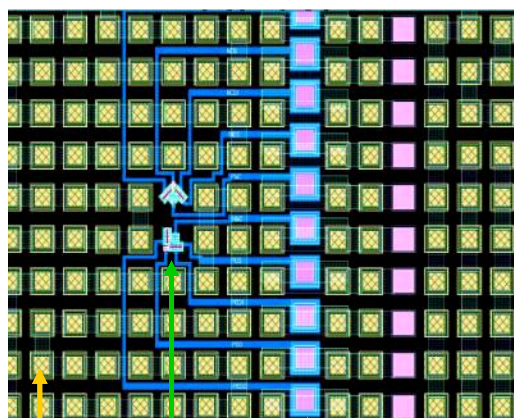
Best Reliable Ambient Intelligent Nanosensor Systems

supported by the European Commission under support-no. ICT-257488

Main objectives of e-BRAINS:

- Highly **reliable heterogeneous systems**
- **Robust 3D integration** processes
- Efficient **system simulation & design** support

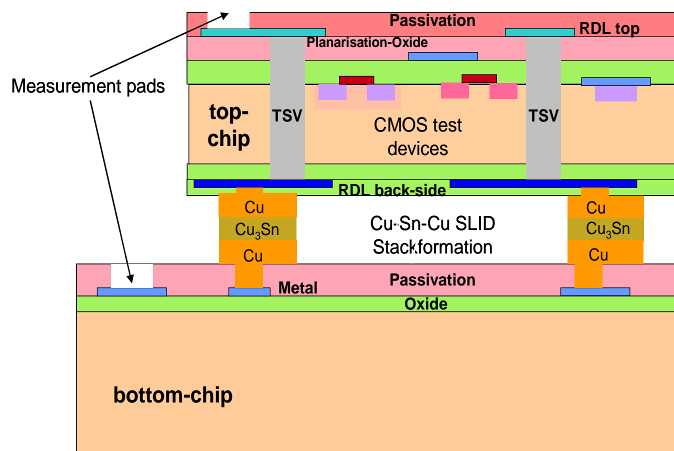
➢ EMFT´s reliability test chip for 3D TSV technologies



TSV connected to daisy-chains

CMOS stress sensor

Measurement pads for back-to-face or face-to-face stacks



www.e-brains.org

Dr. Peter Ramm, Fraunhofer EMFT Munich

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Technology Platforms and Applications in e-BRAINS

Applications

Smart Biosensor Grain (MAGNA, Infineon)

Infrared Imager (Sensonor)

Active Medical Implant (Sorin ELA)

Air Quality System (Siemens)

Smart Ultra-Sound Imaging Probe (VERMON)

Heterogeneous Integration Technologies

TSV-SLID Low-Temperature IMC- Bonding (Fraunhofer EMFT, Infineon)

Layer Transfer Bonding (SINTEF, Sensonor)

TSV-SWACF Sub-µm Wire ACF Bonding (Tyndall, Fraunhofer EMFT)

WDoD Through Polymer Via; Wire-free Die on Die (3D-Plus)

PAECE & Liquid Fill High-Perform. Interposer & 1step wiring (Siemens, Fraunhofer EMFT)

Reliability
(Infineon, TUC, Fraunhofer, Siemens, ITE, IMEC)

Technology Components

High-performance Communicatio n and Antennae (Infineon Austria, IMEC, Fraunhofer, EPFL)

Nano Structures Functionalized for sensing (EPFL, Siemens, Tyndall, SINTEF, IQE, CEA) For optical field manipulation (SINTEF, Siemens)

High-efficient Energy Management (Infineon Austria, DMCE, TUG)

General technological inputs to applications
Heterogeneous integration technology inputs to applications
Heterogeneous integration technology inputs to general technologies

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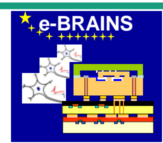

3D Technology is now entering a main stream

End Users

Requirements
Roadmaps
Specifications

Chip Sets
Chips

Requirements
Roadmaps
Specifications

Chip Set/Fabless

IDMs

Requirements
Roadmaps
Specifications

Chips

Requirements
Roadmaps
Specifications

Chips

Tools
Materials

Requirements
Roadmaps
Specifications

Foundries/OSATs

Tools

Requirements
Roadmaps
Specifications

Tools
Materials

Requirements
Roadmaps
Specifications

EDA/Test Suppliers

Equipment/Materials Suppliers

Ecosystem needs

Standards

Infrastructure

Robust tooling

Interoperability

Cost models

Supply chain coordination

Ref.: S. Arkalgud, Future Fab Int., Issue 38, July 2011

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Supply Chain Alignment

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Ecosystem needs

- Standards
- Infrastructure
- Robust tooling
- Interoperability
- Cost models
- Supply chain coordination

Reliability !

Who is reponsible ?

Based on: S. Arkalgud, Future Fab Int., Issue 38, July 2011

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Summary

- 3D Technology is now entering a main stream
- Promising future applications
  - Memory stacks, memory/logic, … (high density TSVs)
  - Heterogeneous MEMS/IC integration (medium density TSVs)
- Choice of 3D process depends on
  - Performance, TSV/pad pitch requirements
  - Reliability requirements
- Reliability issues – related to TSV and the entire 3D TSV flow
- Process reliability, yield and thermal management are basic

requirements under 3D manufacturability

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Thank You For Your Attention !

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