



IMEC ACTIVITIES IN IMAGERS AND IMAGER STACKING

PIET DE MOOR

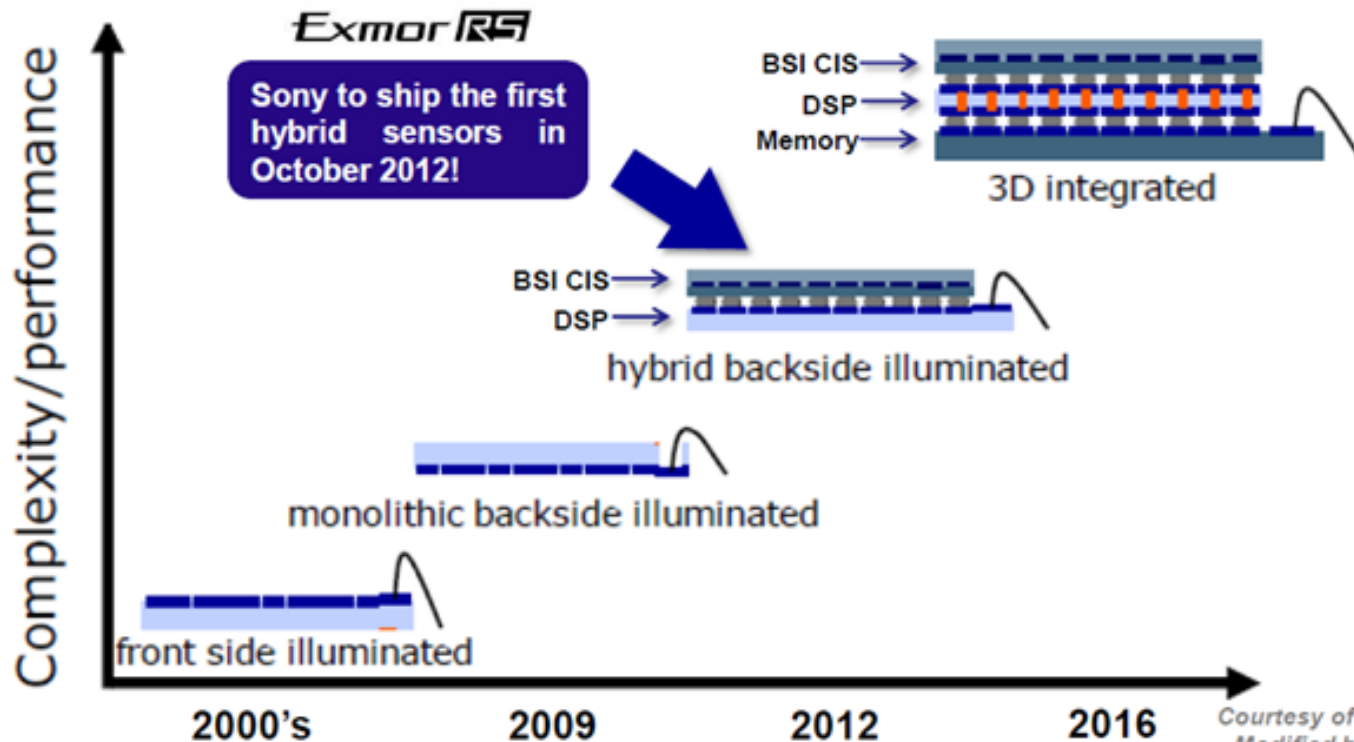


ISSUES WITH 3D STACKING

- 3D stacked imagers are nice ... on paper
- issues:
 - (compound) yield
 - cost
- solution:
 - use available/mature technologies
 - limit excess processing

YOLE/IMEC IMAGER ROADMAP

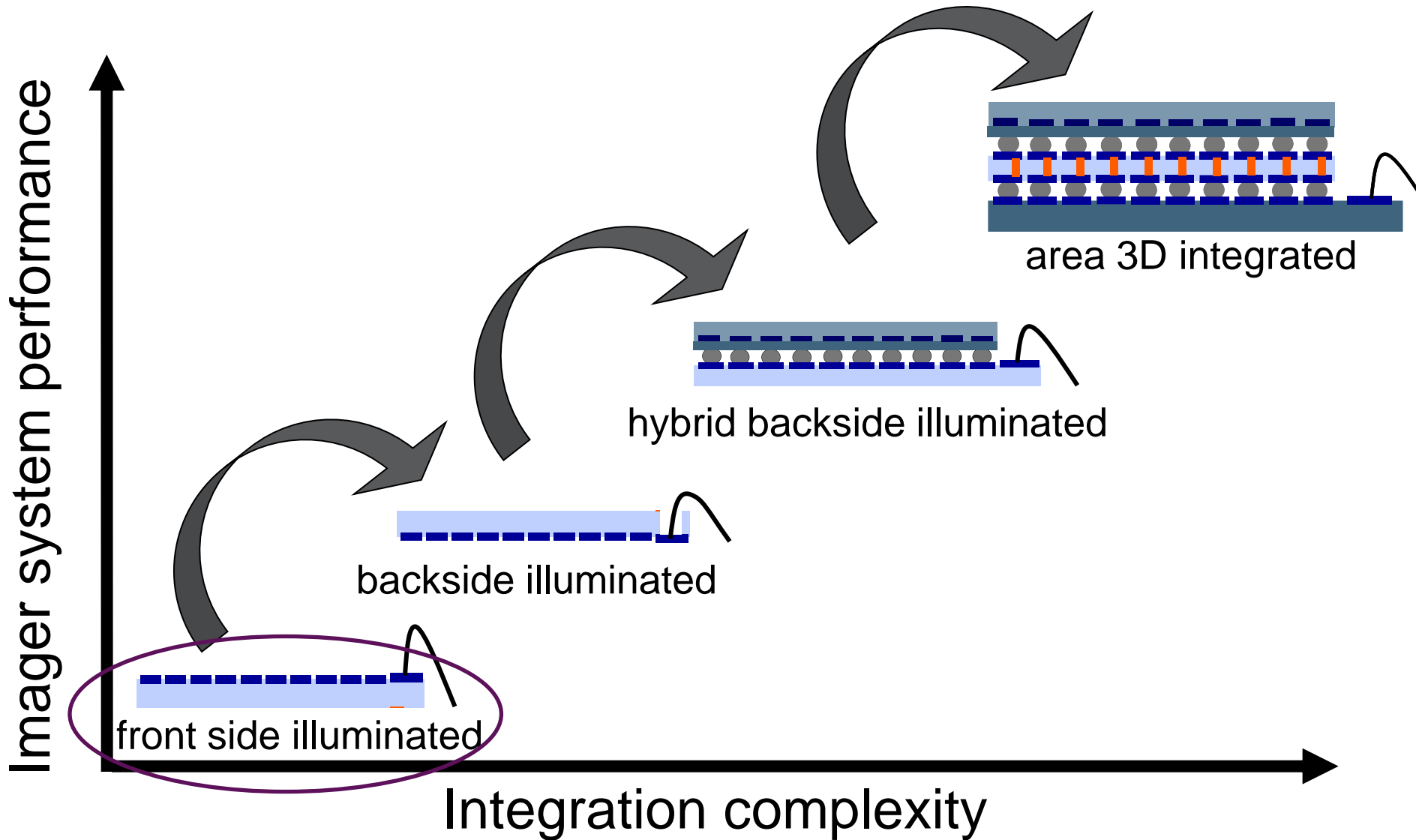
BSI: Key to 3D Integration



Courtesy of IMEC.
Modified by Yole

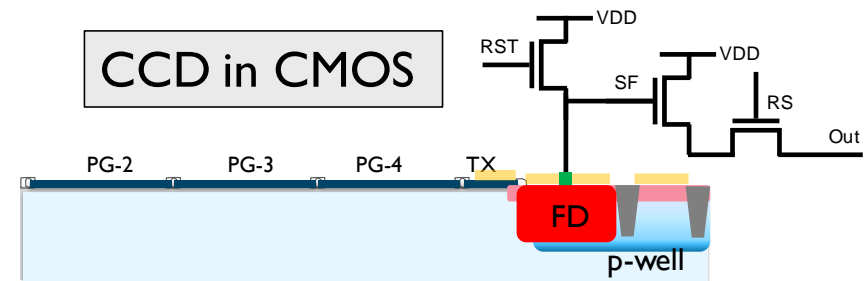
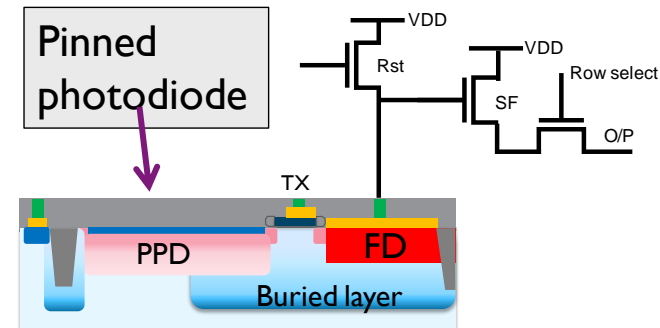


ADVANCED IMAGER INTEGRATION



SYSTEM ON A CHIP IMAGERS

- **Imec solution: CMOS based imager technology:**
 - 0.13 μm CMOS platform
 - + CIS (CMOS imager sensor) module: 4T pixel
 - + high end add-on's and custom process development:
 - Backside illumination
 - Embedded CCD
 - Hyperspectral filters



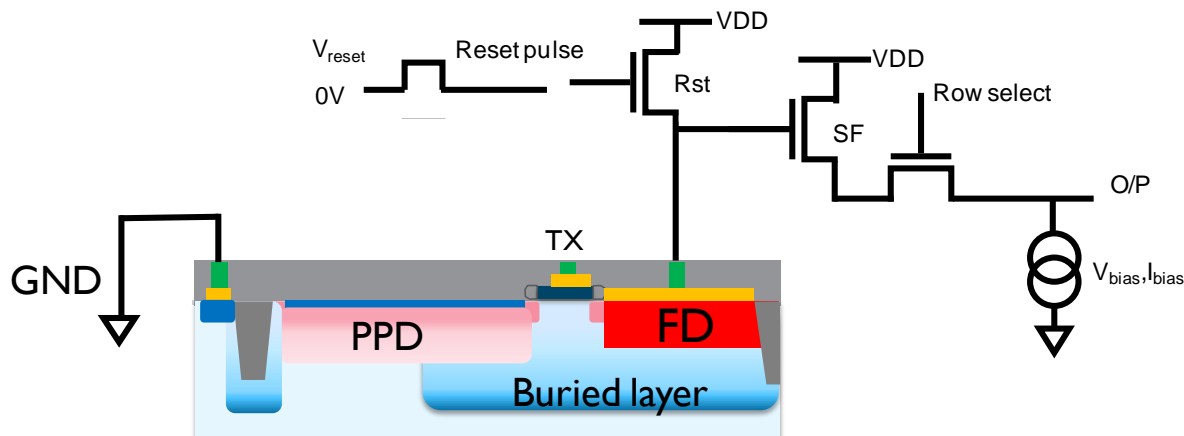
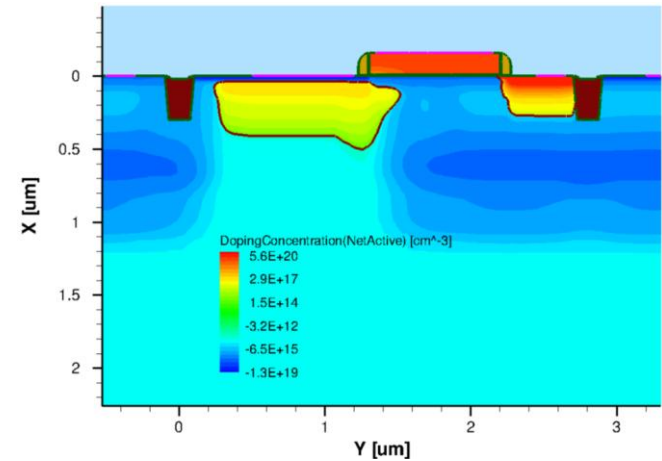
PCIS PIXEL DESIGN: IMEC

4 Transistor pixel with pinned photodiode:

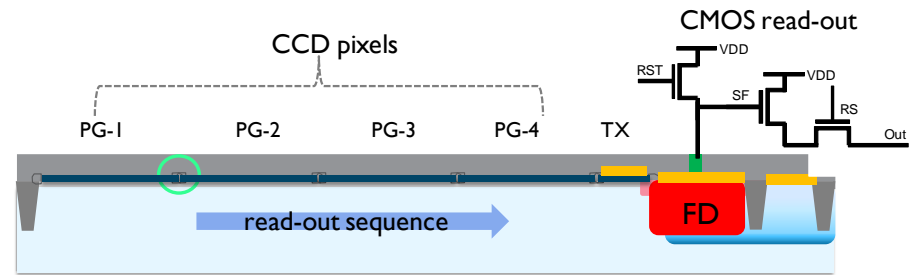
- ✓ low noise
- ✓ low dark current
- ✓ correlated double sampling compatible
- ✓ shared floating diffusion node

Key technology:

- ✓ custom design and process for:
 - photodiode
 - transfer gate
 - reset and source follower transistors



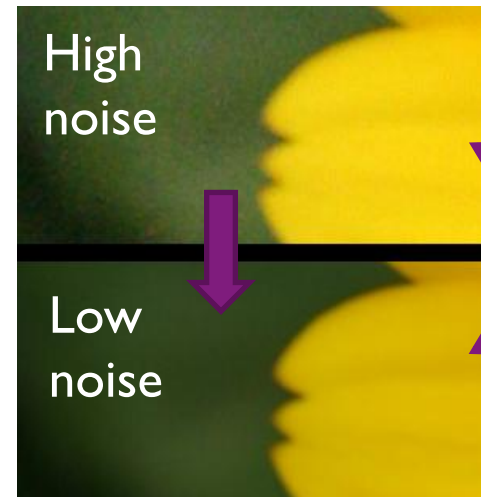
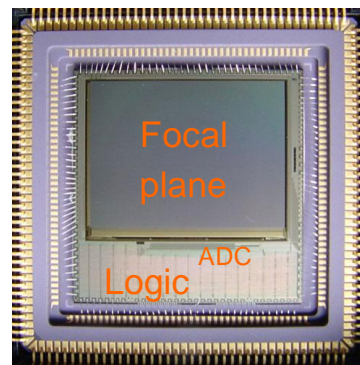
EMBEDDED CCD IN CMOS



■ embedded CCD = combination of CCD and CMOS enables:

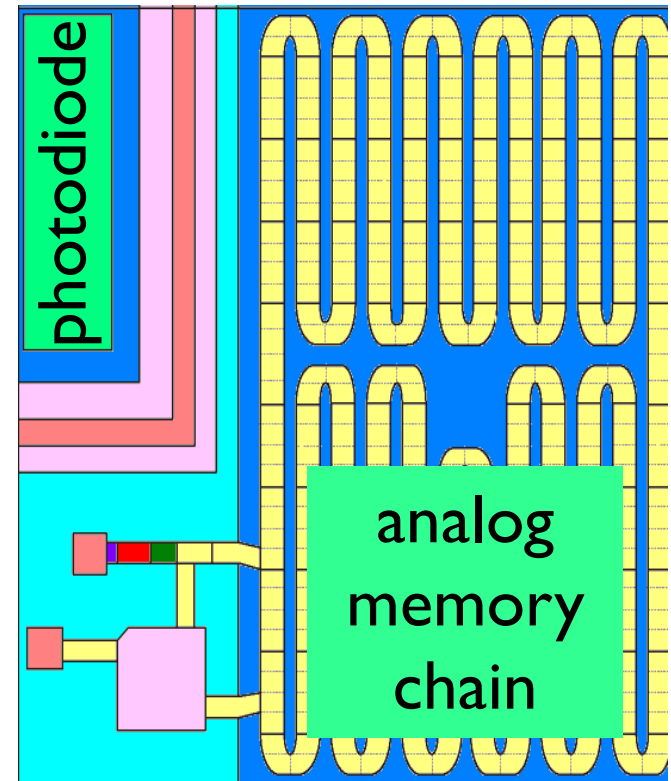
- ultimate low noise & dark current ←
- system on a chip integration

CCD
CMOS

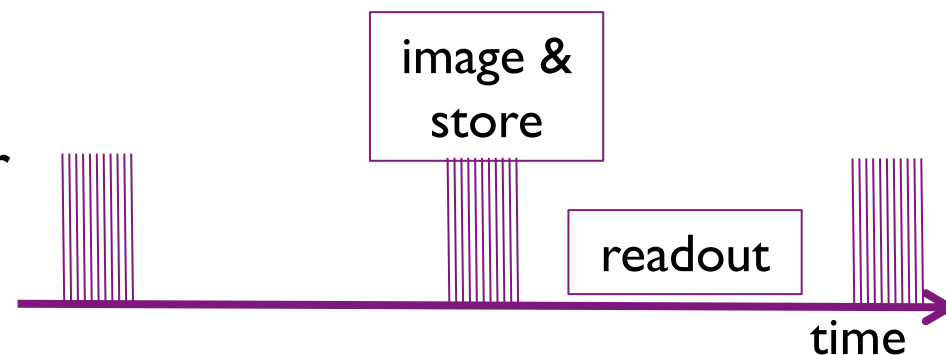


ULTRA FAST IMAGING: USING ECCD

- Design solution:
 - in pixel memories
 - = store a (limited) number of frames inside pixel
 - readout at lower speed
 - allows burst mode of imaging
- embedded CCD in CMOS technology:
 - noiseless storage and transfer



Source: G. Etoh

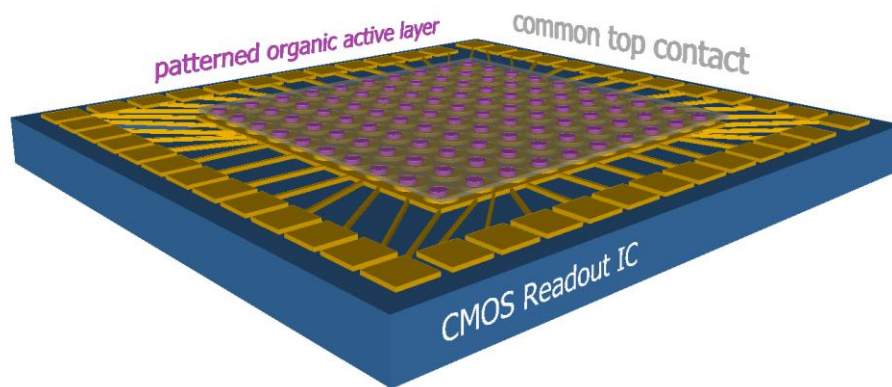


ORGANIC IMAGERS

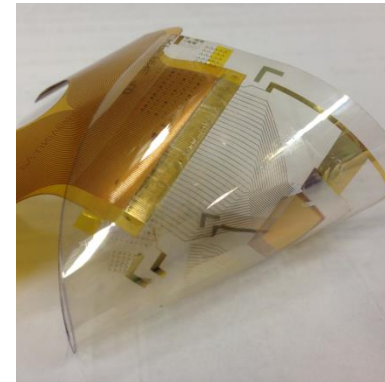
■ Concept:

- Manufacturing of photodiodes based on organic materials (i.e. non-Si)
- Two possible routes for integration:

organic imager on Si readout



organic imager on foil



■ Challenges:

- Process development
- Outgassing, temperature behavior, radiation hardness, dark current, ...

RADIATION HARD DESIGN @ IMEC

- DARE: Radiation-hardened-by-design libraries in standard commercial technology:
 - Developed & enhanced in ESA projects
 - Use = free for European space industry & institutes
 - Library of mixed signal & digital design blocks:
 - DARE180 well supported (UMC 0.18 um CMOS)
 - DARE90 small core & IO library available (UMC 90nm CMOS)
 - XFAB .18 XH started
 - On Semi I3T80RH tanner kit for RH HV transistors

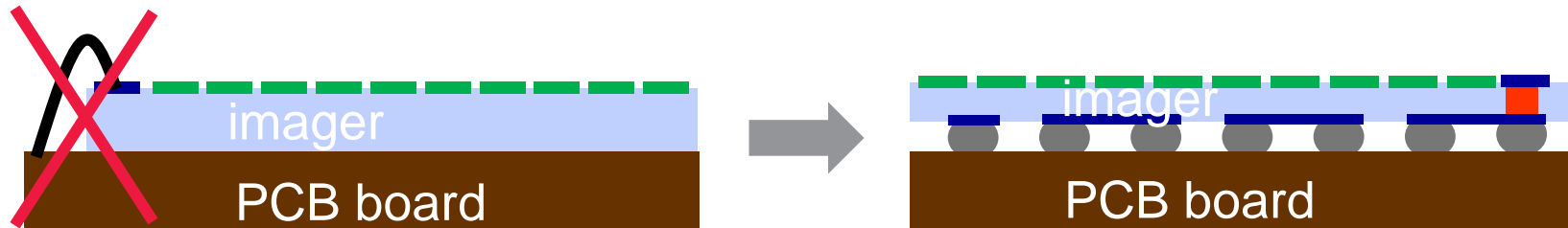


***D**esign
Against
Radiation
Effects*



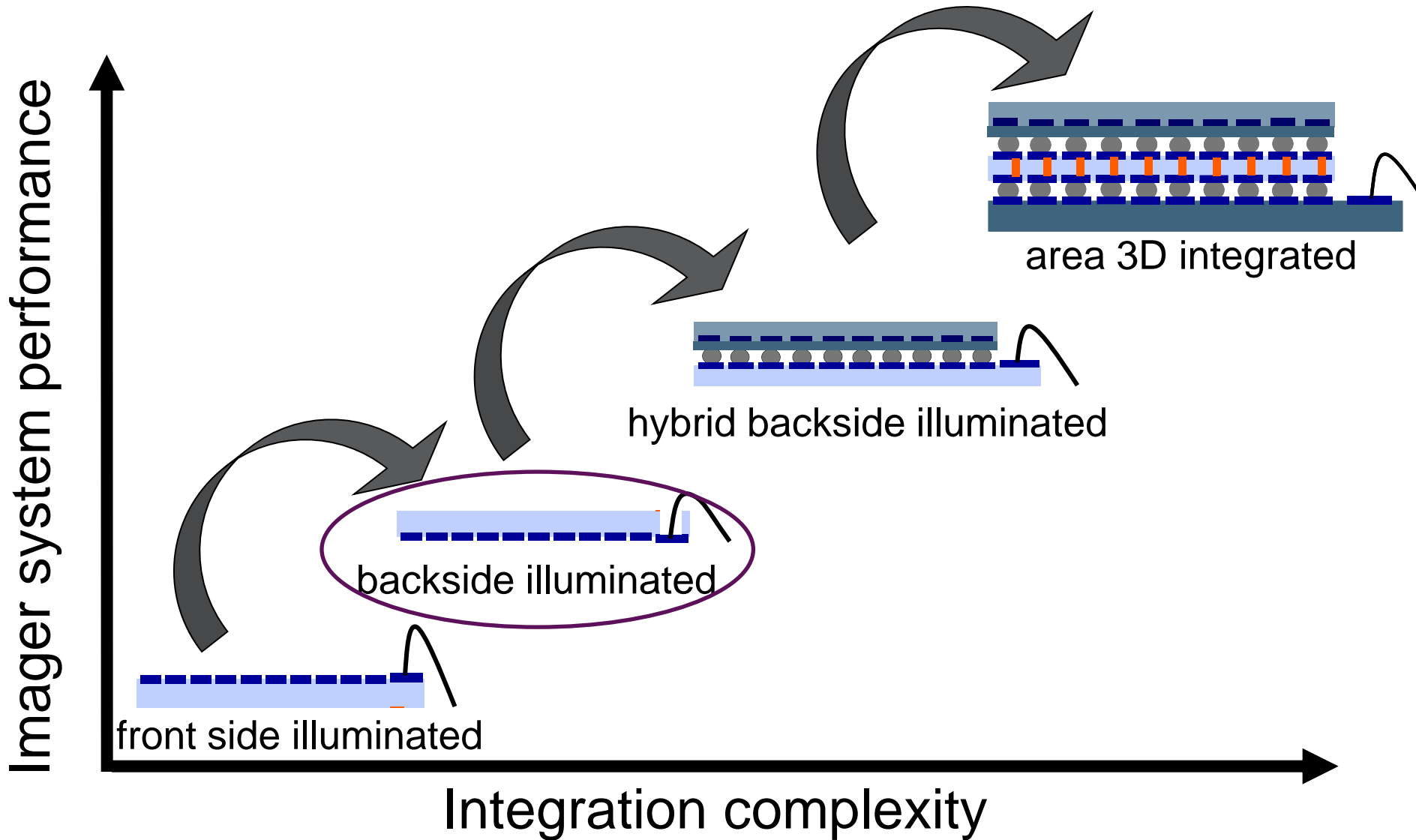
PERIPHERAL 3D INTEGRATED IMAGERS

- Advanced packaging technology at bond pad level:
 - From traditional lateral wire bonding to TSV per bond pad + bump ball bonding
 - = 3D integration at package level using Through Si Vias (TSVs)



- Advantages:
 - Smaller footprint
 - Reduced capacitance → faster/low power interconnect
 - Buttability with minimal area loss
- Applications:
 - Consumer imager packaging
 - Endoscopes
 - Large area tiled imagers with minimal dead area

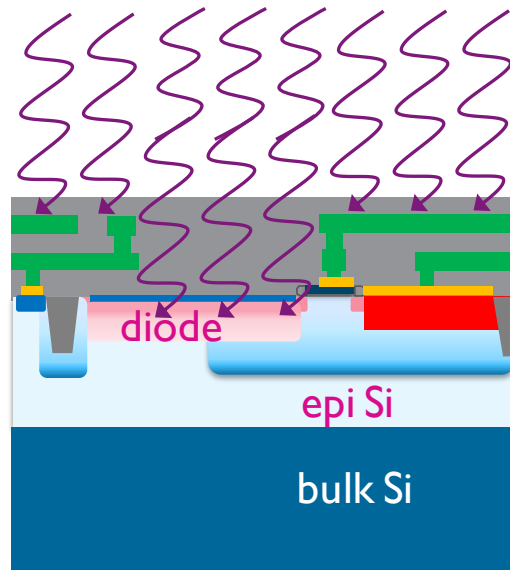
ADVANCED IMAGER INTEGRATION



BACKSIDE VS. FRONTSIDE ILLUMINATION

- **Front side illumination:**

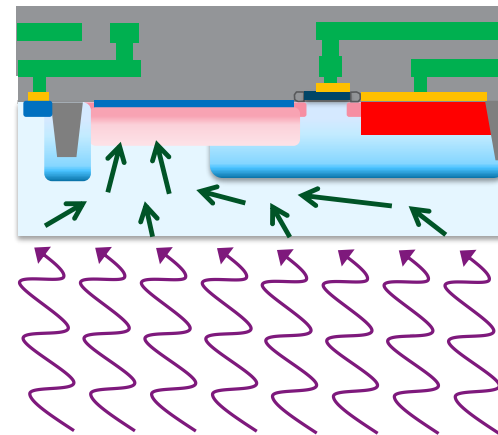
- Absorption in BEOL dielectrics



Front side illuminated

- **Backside illumination :**

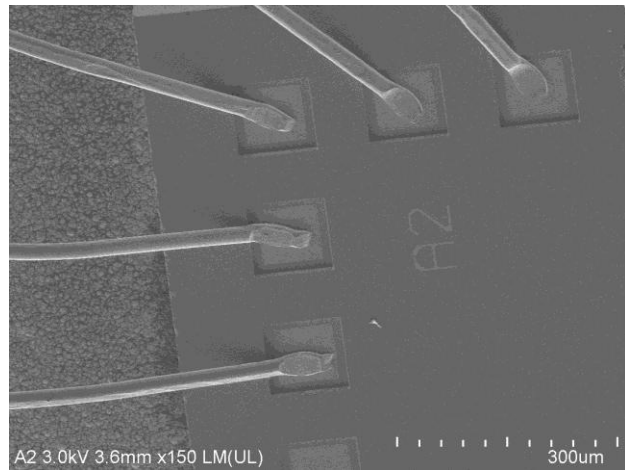
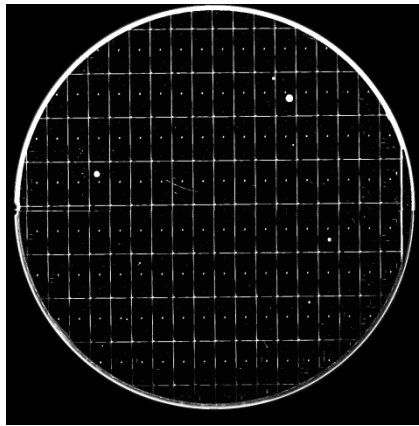
- Direct absorption in Si



Backside illuminated

- imec provides backside illuminated imager platform including **very shallow surface passivation**

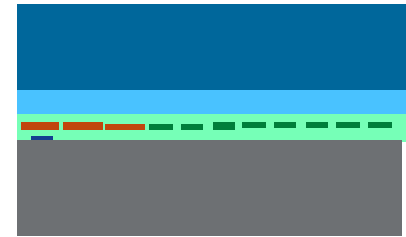
IMEC BACKSIDE ILLUMINATED IMAGER PROCESS PLATFORM



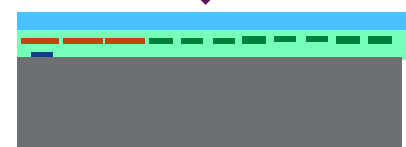
CIS CMOS



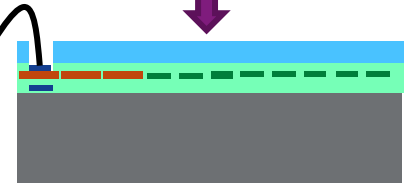
W2W Bonding



Thinning & Passivation



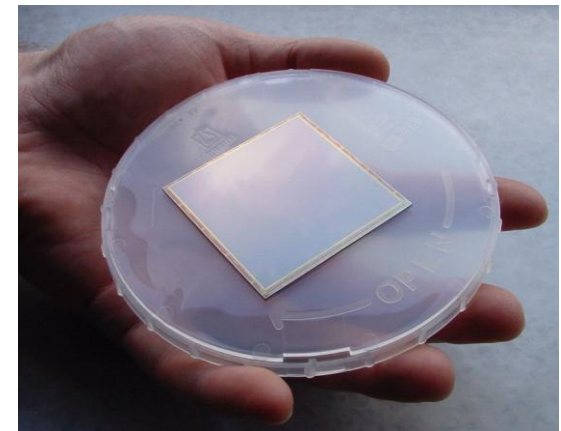
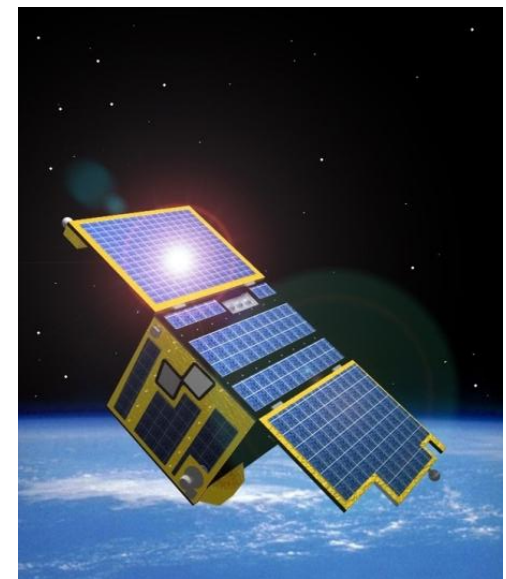
Bondpad opening



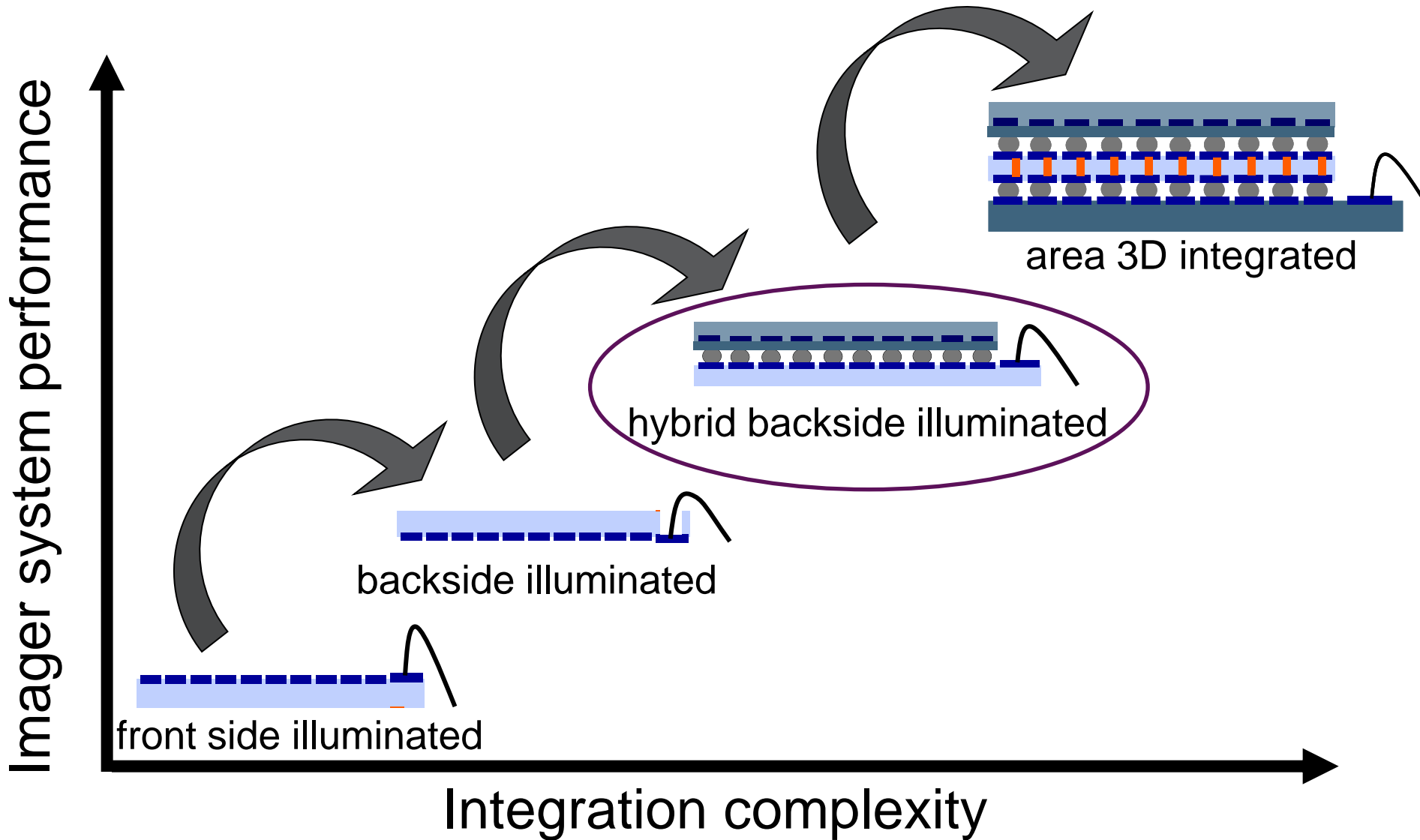
- Investments done, equipment expected ~ Q2 2013

'EUROCIS'

- European source for space imagers
- Requirements:
 - Design & process in imec 0.13 um CMOS
 - Global shutter
 - **Backside illuminated**
 - **Large area (stitched)**
 - **Radiation hard**
- Partners:



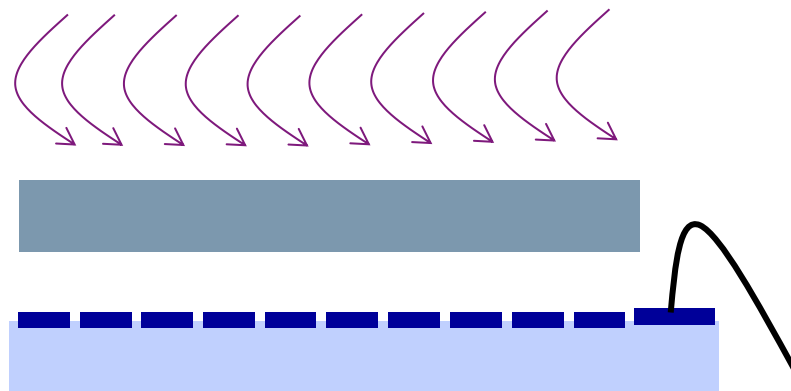
ADVANCED IMAGER INTEGRATION



HYBRID IMAGERS: APPROACH

■ 2 layers:

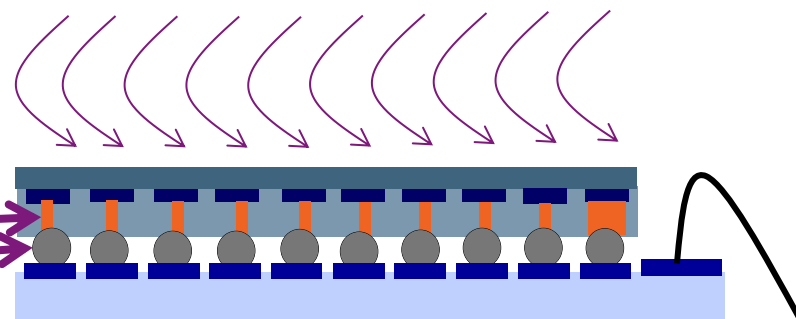
- Detection layer + optional (analog) read-out
- 2nd read-out layer



■ integration options:

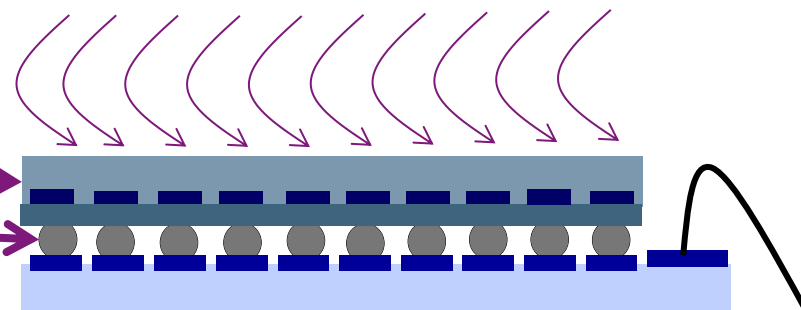
• Front side illuminated:

- through Si vias (TSVs)
- + microbumps required

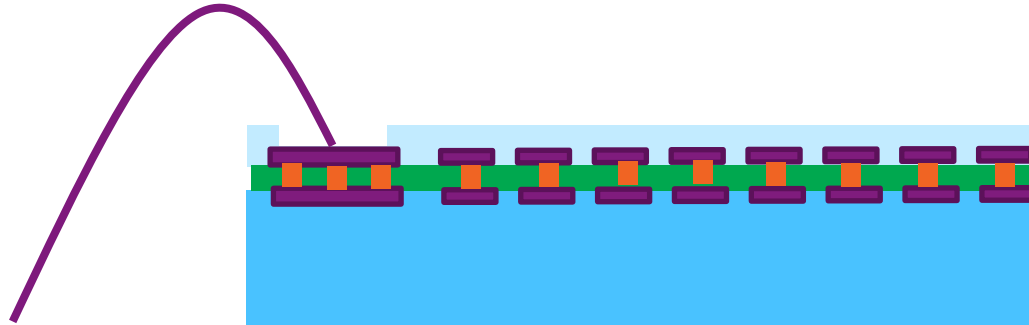


• Backside illuminated:

- Backside thinning
- + microbumps required

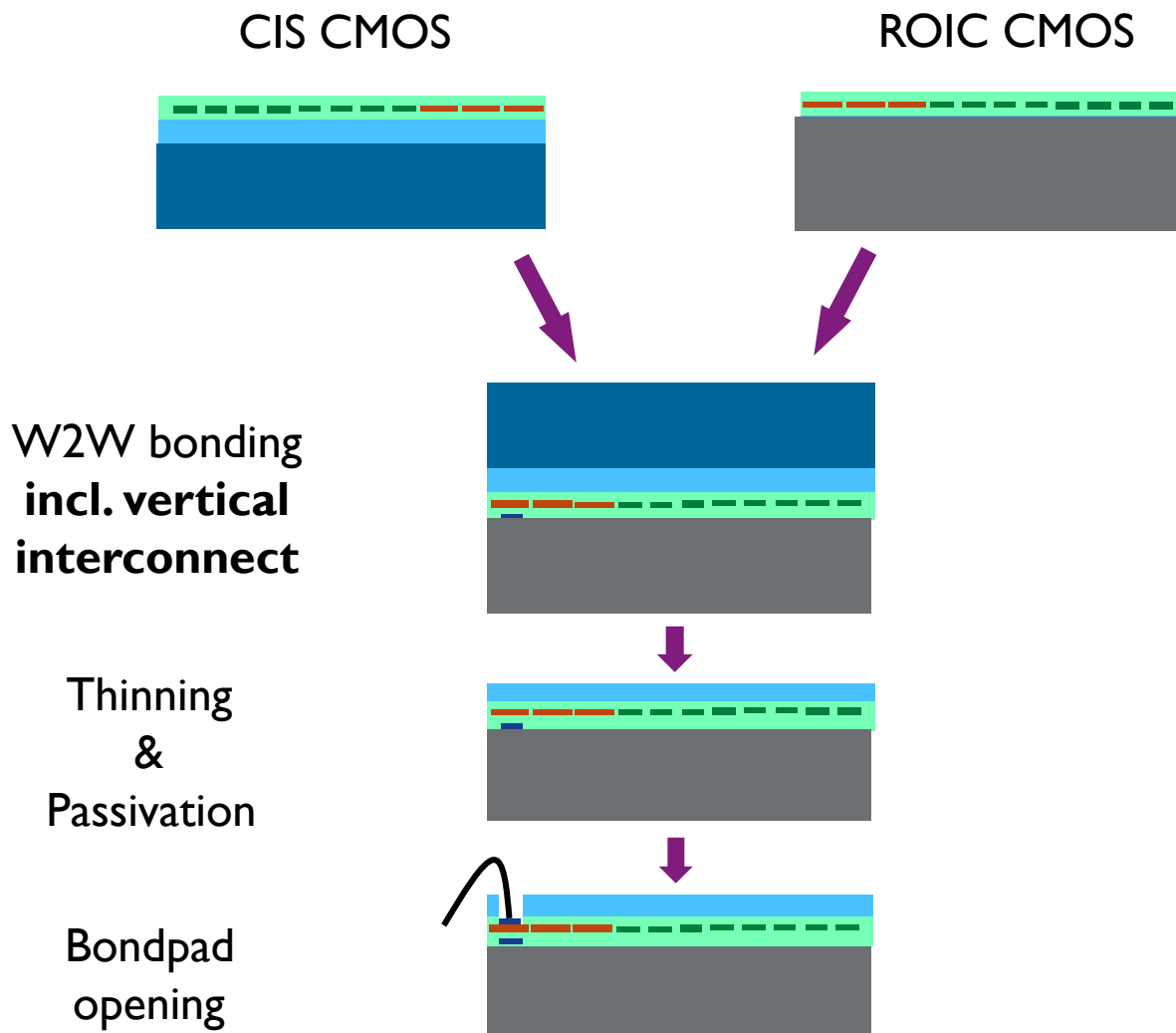


HYBRID BACKSIDE ILLUMINATED IMAGER



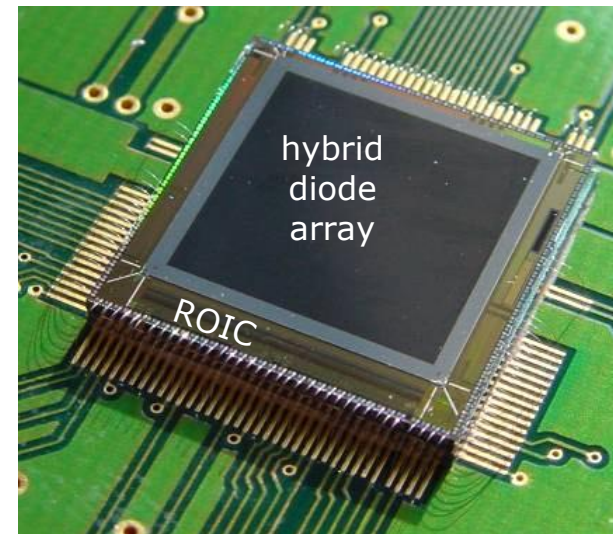
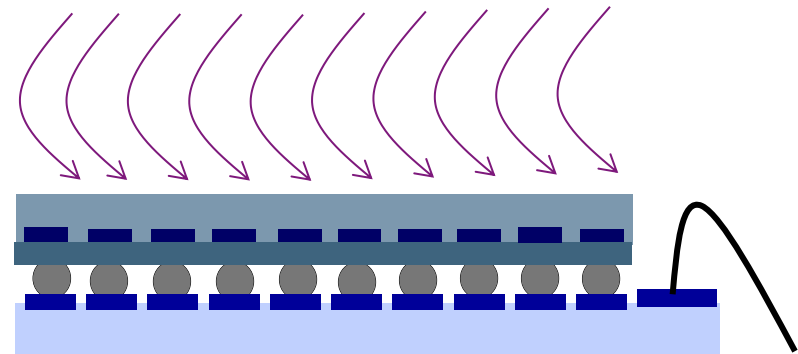
- Both top and bottom die made in imec 0.13 um CMOS:
- Wafer to wafer bonding:
 - Mechanical + electrical connection
- Backside illumination module:
 - Backside thinning + passivation
 - Bondpad opening
- Wirebond connection of bottom die using W2W electrical interconnect to top die

HYBRID BSI FLOW

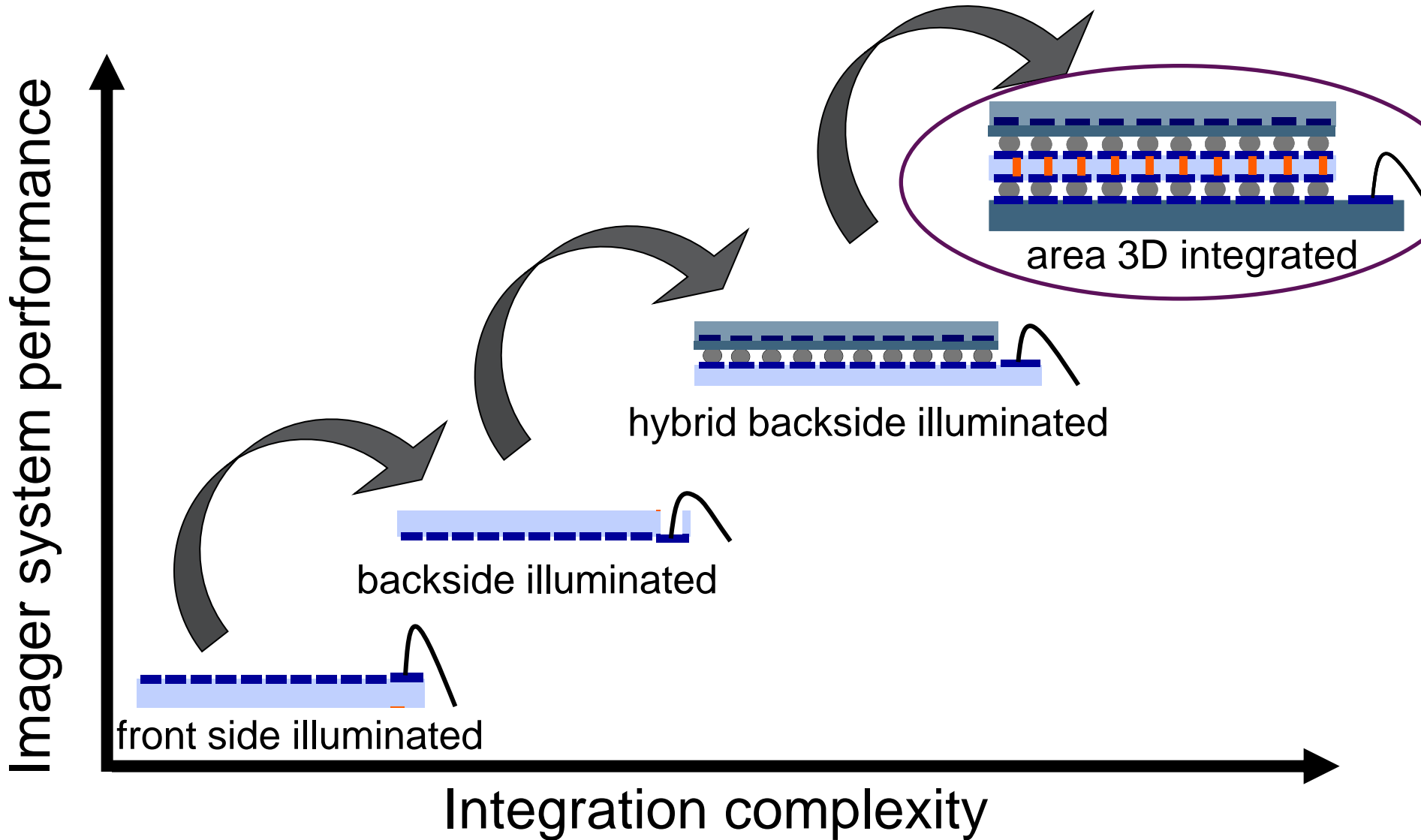


HYBRID BACKSIDE ILLUMINATED IMAGER 'HYBRID APS'

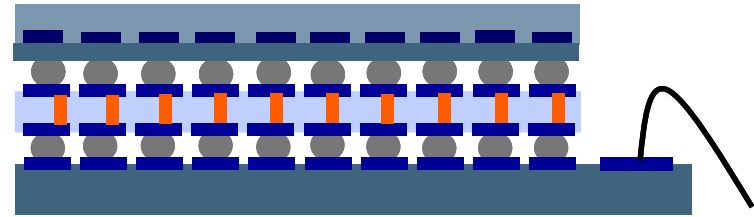
- Specifications:
 - 22.5 μm pitch
 - Stitched design: 512x512, 1024x1024
 - **QE > 80% from 400 – 850 nm**
 - Thick epi: final thickness \sim 12-35 μm
- Passive photodiode array (including trenches for X-talk reduction, graded epi) designed and fabricated @ imec
- ROIC designed by **FillFactory/Cypress**, fabricated in CMOS 0.35 μm **commercial foundry** process
- Backside thinning, backside passivation, hybridisation @ imec



ADVANCED IMAGER INTEGRATION



AREA 3D INTEGRATED IMAGERS



■ Concept:

- Stacking of multiple (>2) layers: detection layer + ROIC layers
 - Example: passive photodetector layer + analog ROIC + digital image processor
- Using high density bumping + area redistributed TSVs

■ Advantages:

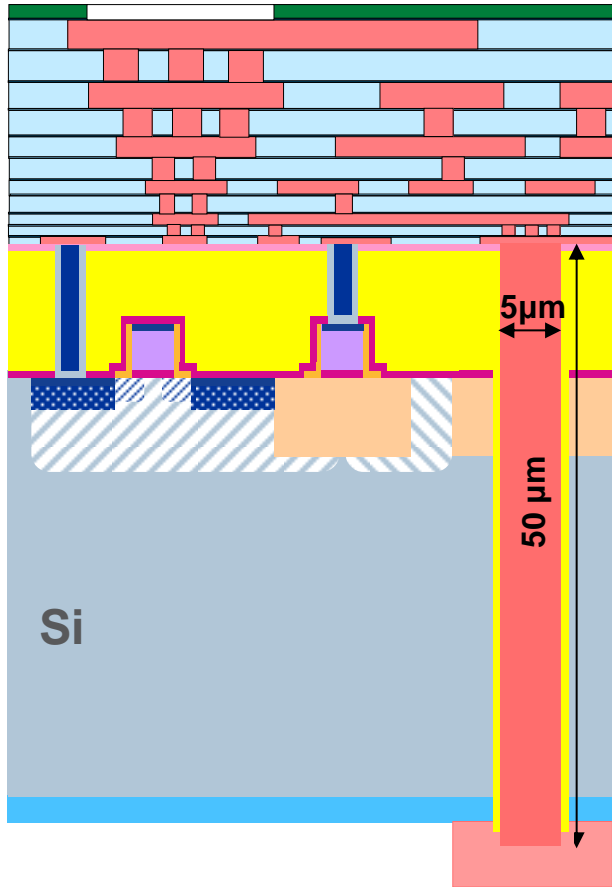
- General: optimization of (CMOS) technology for different layers
- Imager system:
 - Vertical parallel readout chain allows high speed
 - Triple (n-fold) area per pixel allows complex electronics per pixel
 - Low capacitance interconnect to digital image processor allows high speed and low power

■ Challenge: system architecture:

- Optimal split in different layers of functionality and technology

VIA MIDDLE THROUGH-SI-VIA PROCESS

"Via-middle": fabrication TSV's after FEOL device fabrication processing but before BEOL interconnect.

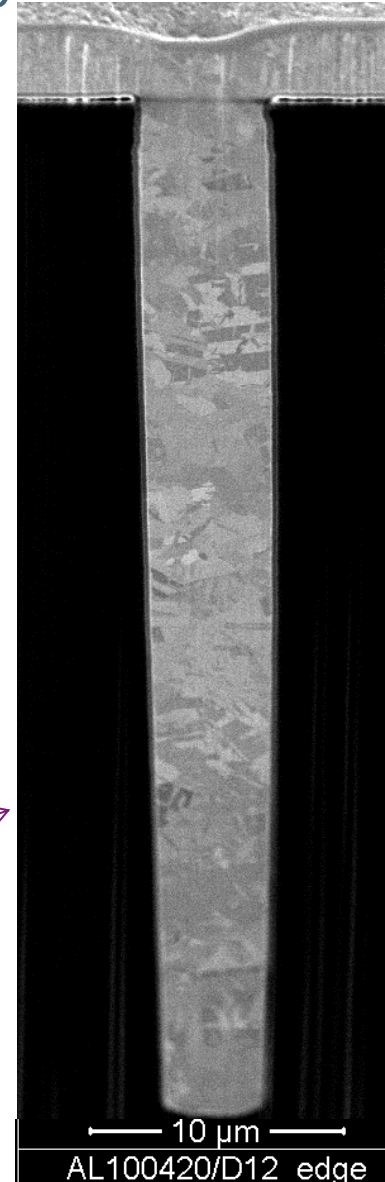


Key features :

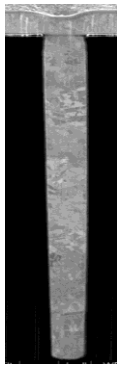
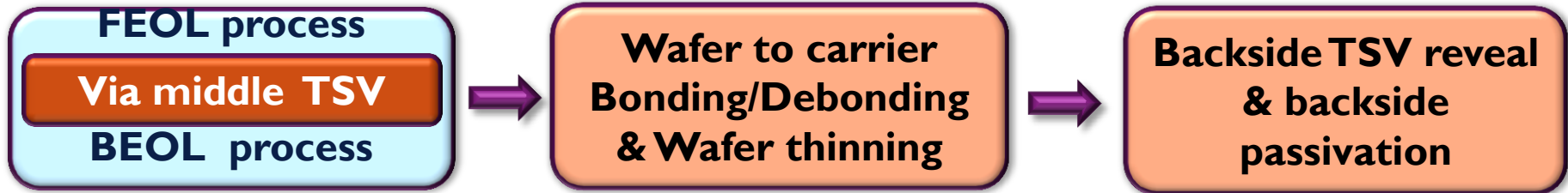
- ▶ “Cu-nail” process after FEOL, before of BEOL processing
- ▶ High aspect ratio Cu damascene technique
- ▶ Single litho-step

imec POR process:

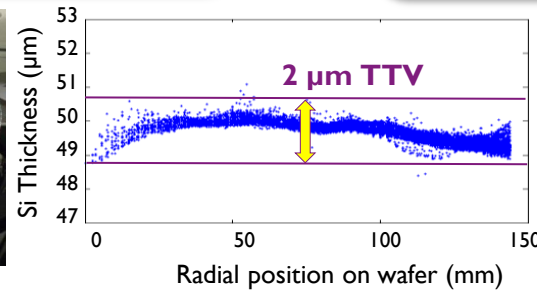
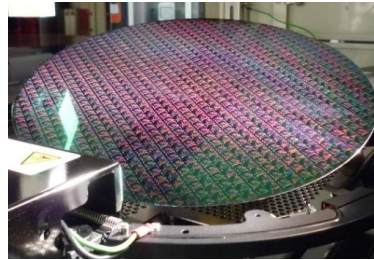
- **5 μm diameter;**
- **50 μm deep;**
- **Aspect ratio 10**



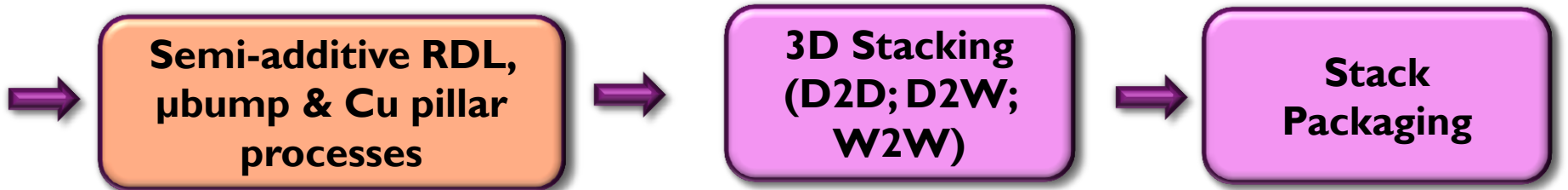
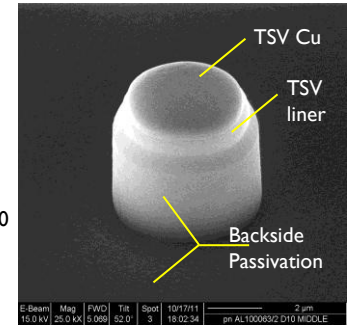
IMEC'S 3D SYSTEM INTEGRATION PROGRAM



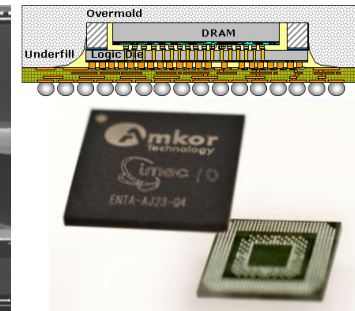
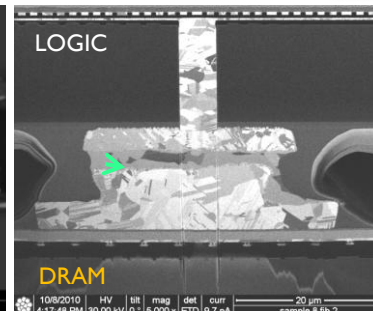
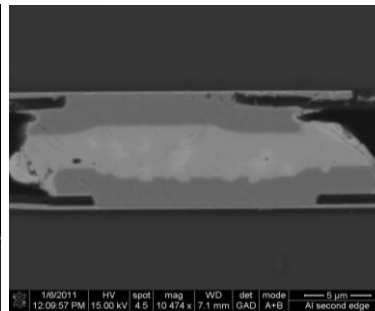
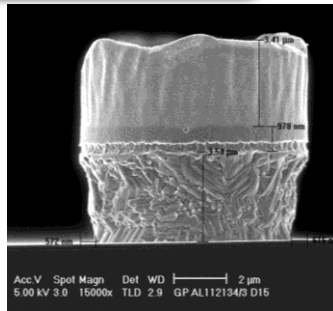
3D SIC
 ➤ POR : 5x50μm
 ➤ Scaling to 3x50μm
 2.5D Interposer:
 POR : 10x100μm



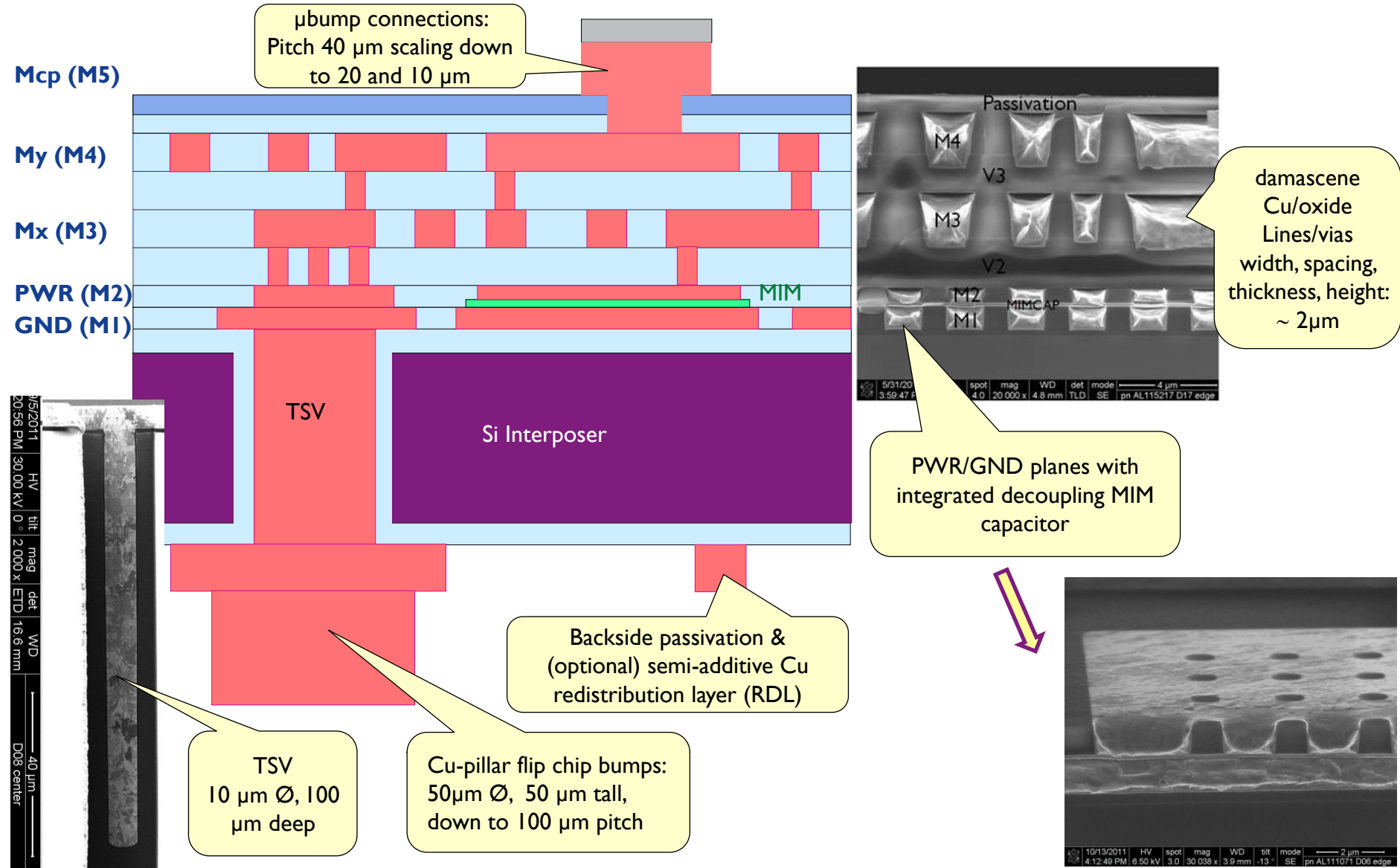
Bonding to Si-carrier ,TTV after thinning < 2μm
 Low T backside passivation (Room T debonding)



Sn-based μbumping
 ➤ Pitch: 40 ⇨ 20 ⇨ 10 μm
 ➤ Wafer-level underfill
 Cu-Cu bonding
 ➤ 10 μm Pitch
 ➤ Low Temperature
 insertion bonding

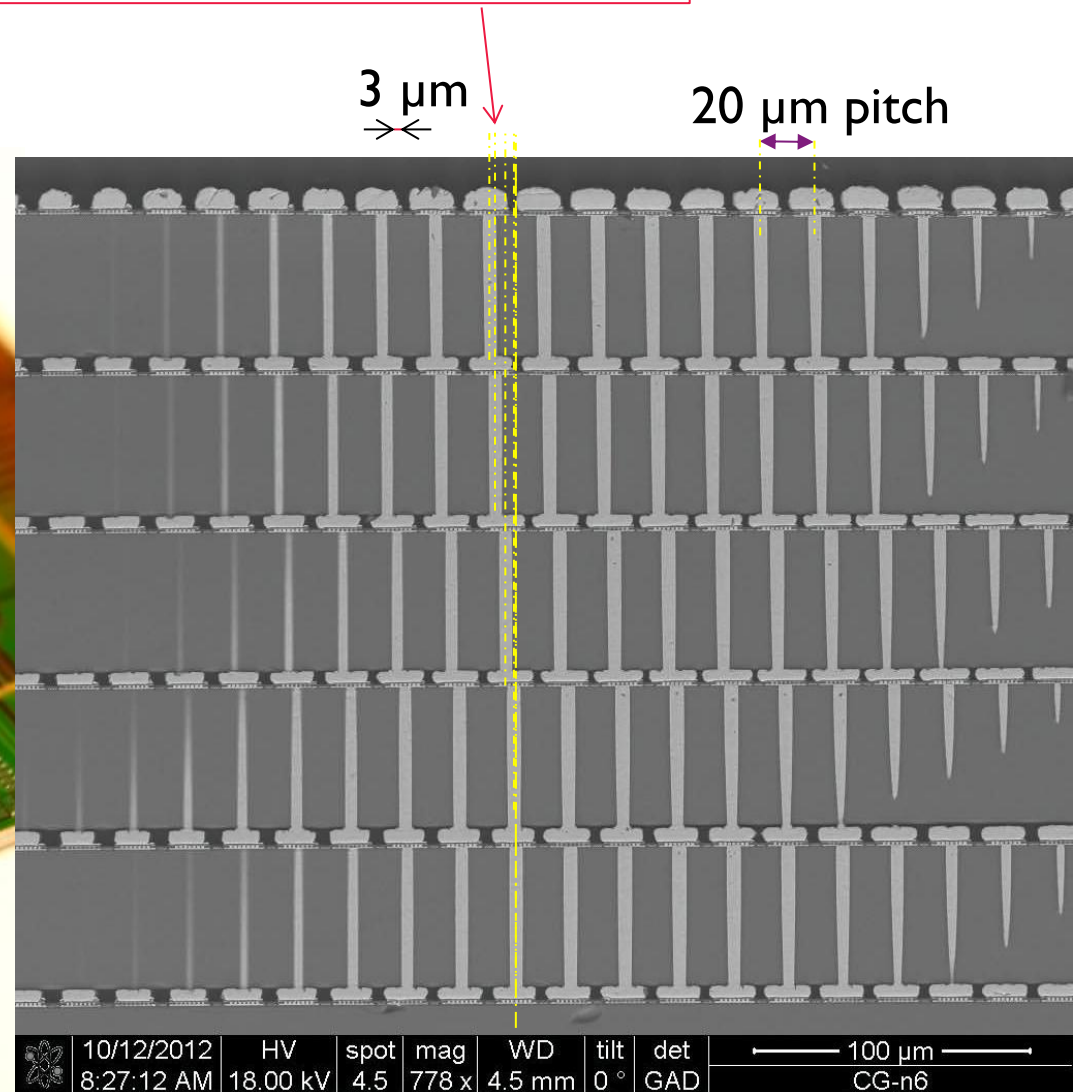
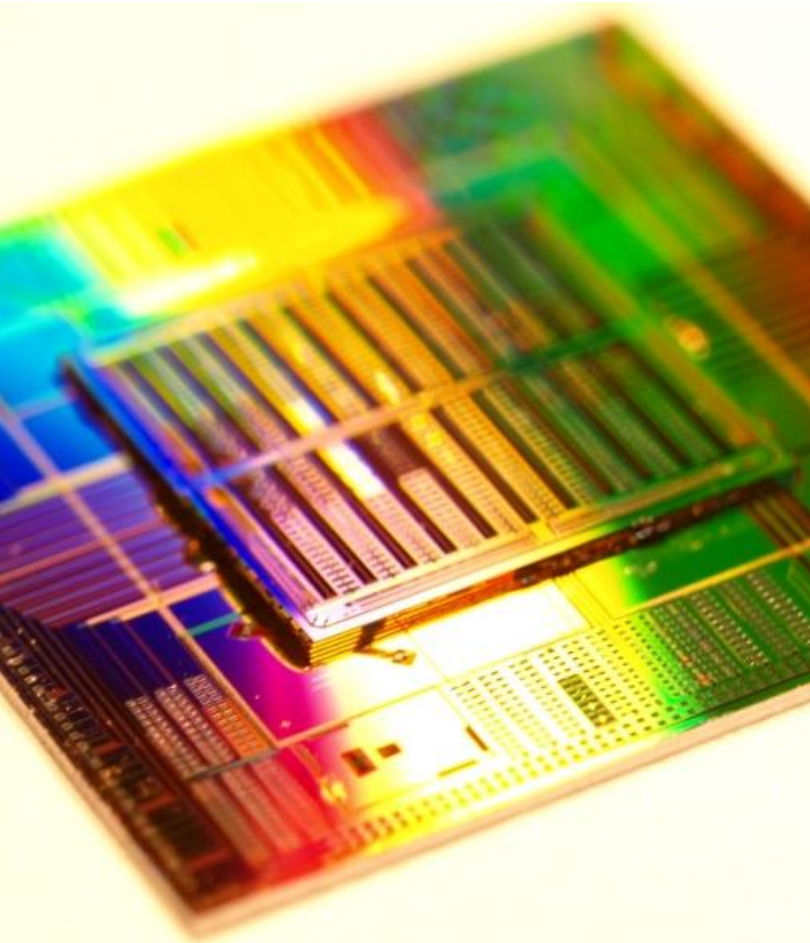


Si Interposer technology development



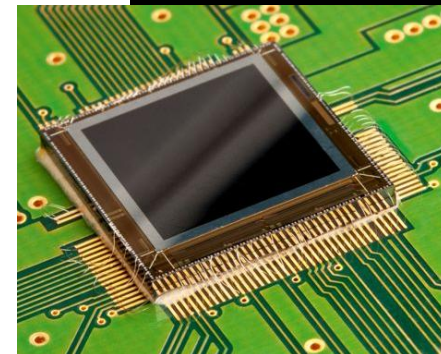
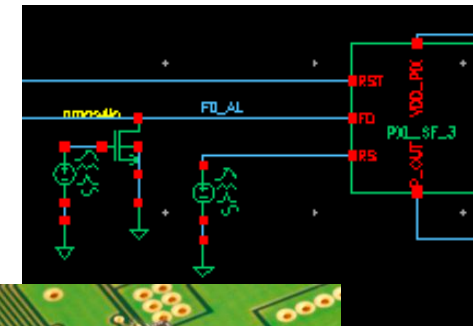
N=6 PTCO/P CU-CU DIE STACKING

Die-to-die overlay error < 3 μm



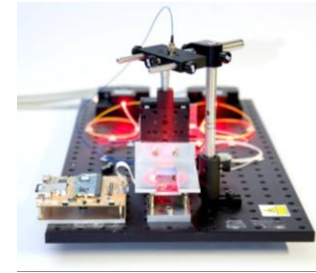
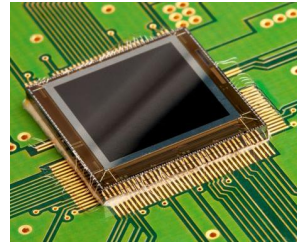
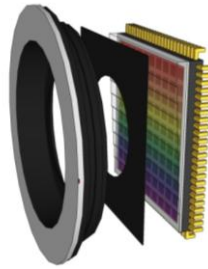
IMEC IMAGER OFFERING

- imec \neq foundry:
 - No standard technology offering
 - No MPW runs
- imec $>$ foundry:
 - imec offers customized specialty imager solutions
 - Flexible technology & design
 - Based on 0.13 μm CMOS platform
 - Imager modules: 4T pixel, BSI, eCCD, 3D ...
 - (Ultra) low volume manufacturing
- Open for collaborations:
 - Fabless design partners
 - Packaging, testing, camera partners

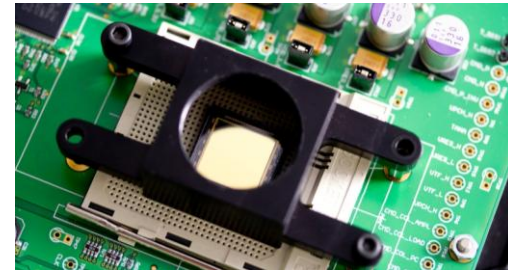
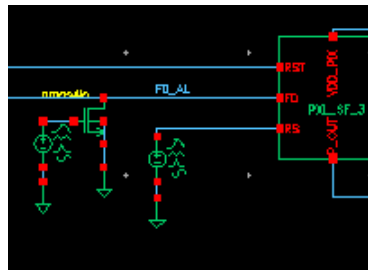


CONCLUSION: IMEC'S OFFERING

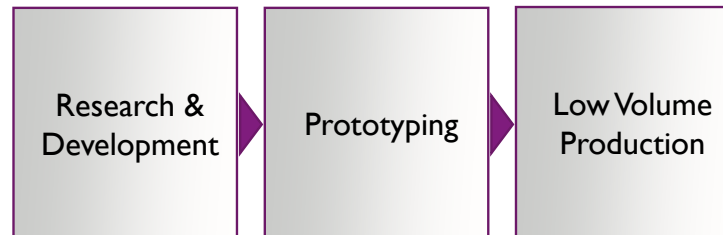
advanced vision systems solutions



innovation at technology, design and system level



from R&D to Low Volume Production



A large, abstract graphic of purple smoke or ink swirling and trailing downwards from the top left corner of the page.

**ASPIRE
INVENT
ACHIEVE**



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