CERN

Capacitively coupled active sensors in 180nm HV-CMOS technology

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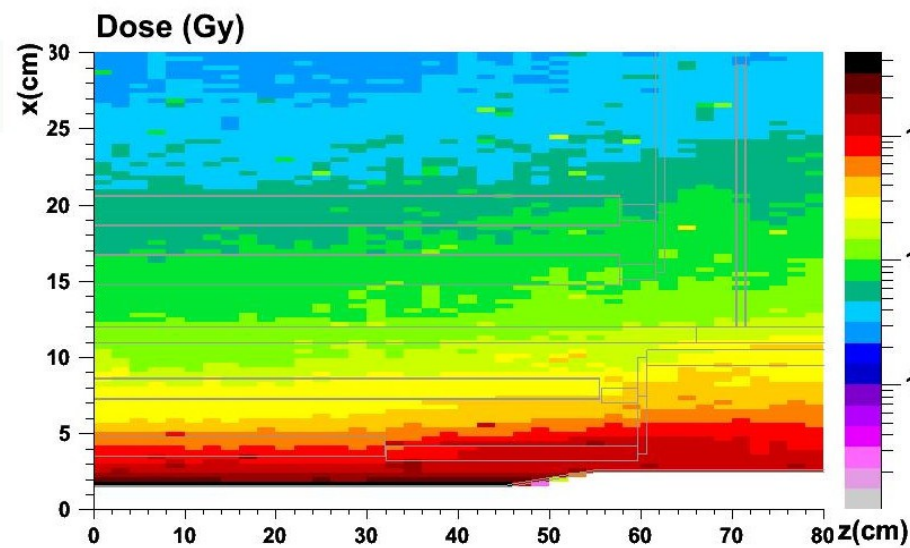
presenting also on behalf of ATLAS HV-CMOS collaborators from Berkeley, Bonn, CERN, Glasgow, Heidelberg and Marseille

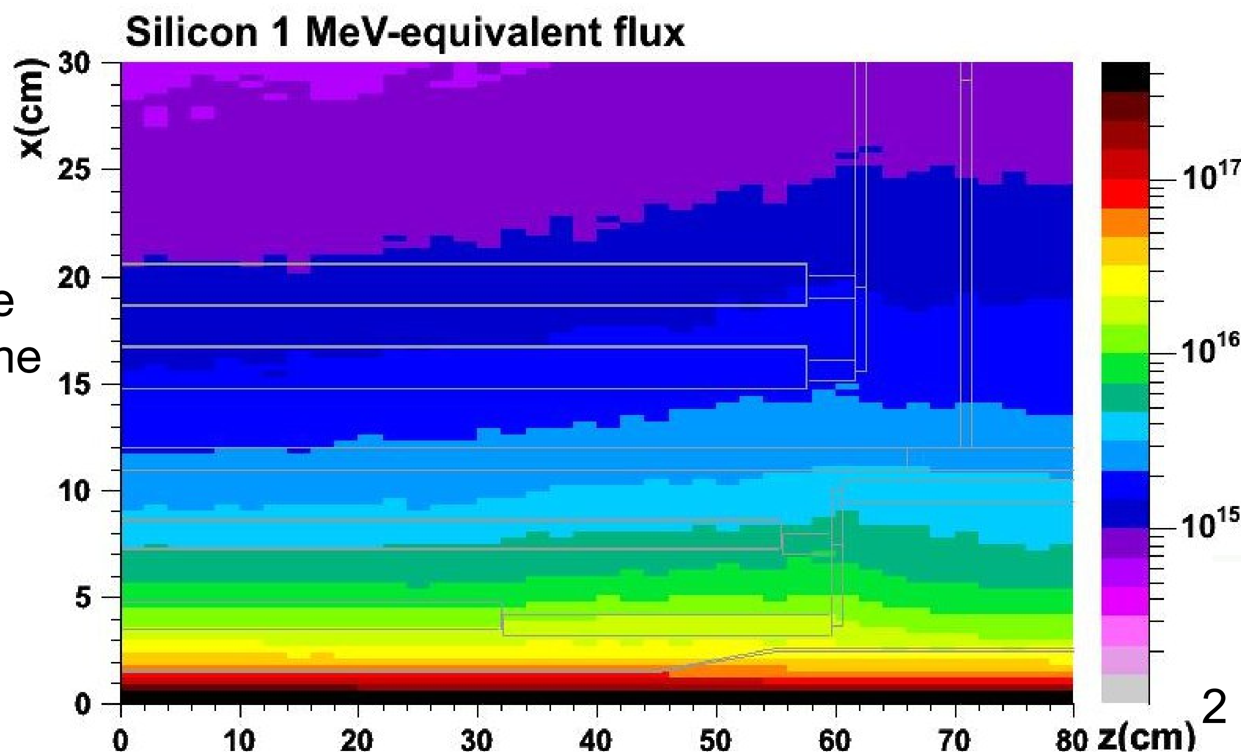
Why new sensors? Fluences at HL-LHC

- integrated luminosity: 3000 fb^{-1}
- including a safety factor of 2 to account for all uncertainties this yields for ATLAS:
  - at 5 cm radius:
    - ~$2 \cdot 10^{16}$ n_{eq} cm^{-2}
    - ~1500 MRad
  - at 25 cm radius
    - up to 10^{15} n_{eq} cm^{-2}
    - ~100 MRad
    - several m^2 of silicon

→ Current Inner Detector needs replacement

- New ID sensors need to be more rad-hard and *cheaper* at the same time (more area to cover)





Implications for Pixel Sensors

- High fluences: trapping dominant
  - reduce drift distance, increase field → reduce drift time:
    - 3D sensors
    - thin silicon
    - low depletion depth 'on purpose', e.g. low(er) resistivity silicon, dedicated annealing to increase N_{eff}
- Large areas: low cost of prime importance
  - industrialised processes
  - large wafer sizes
  - *cheap interconnection technologies*
- **Idea: explore industry standard CMOS processes as sensors**
  - commercially available by variety of foundries
    - large volumes, more than one vendor possible
  - 8” to 12” wafers
    - low cost per area: “as cheap as chips”
  - (partially too) low resistivity p-type Cz silicon
    - thin active layer
    - wafer thinning possible

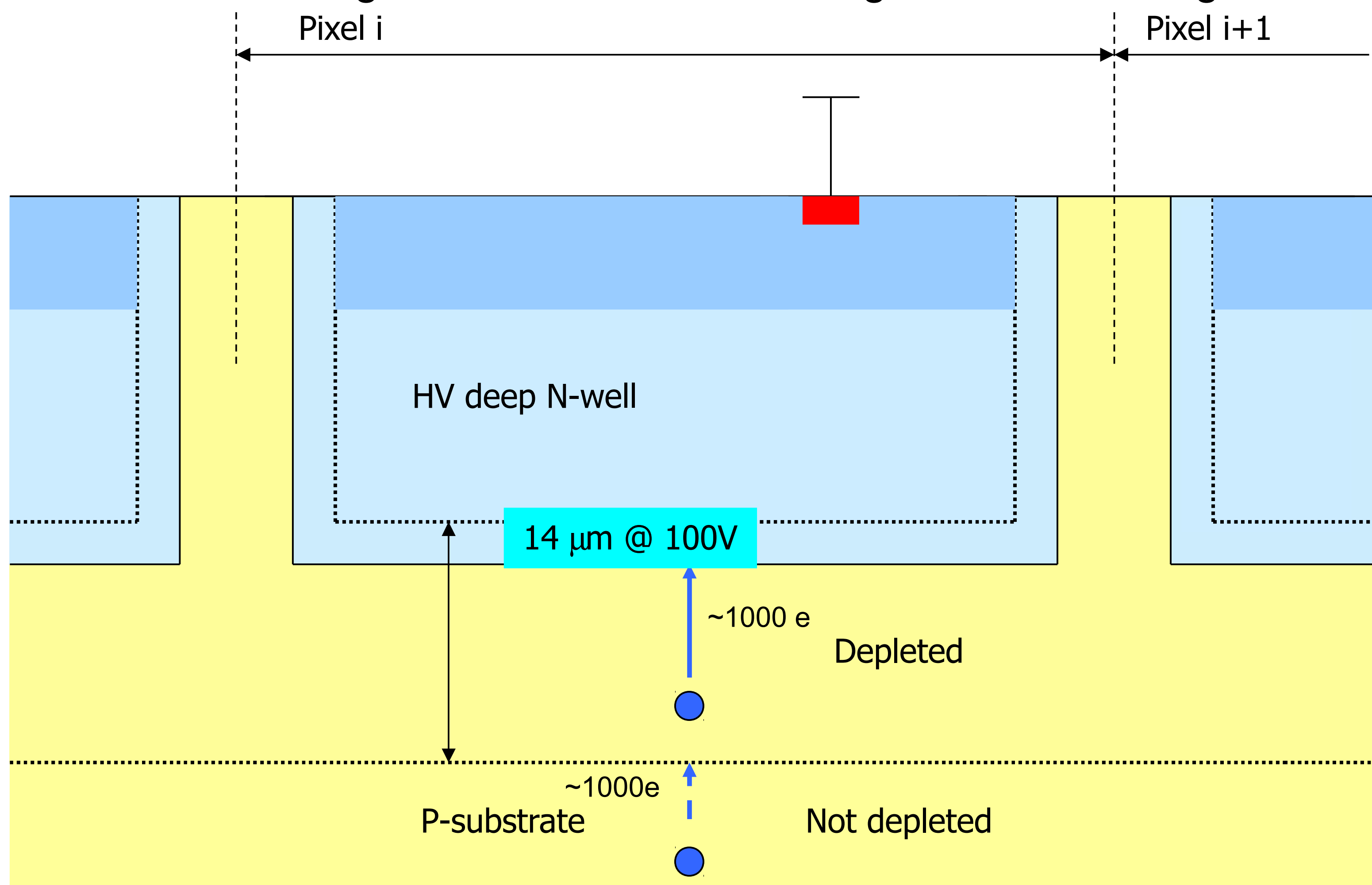
AMS H18 HV-CMOS

- Project initiated by Ivan Peric (U Heidelberg)
- Austria Micro Systems offers HV-CMOS processes with 180 nm feature size in cooperation with IBM
  - biasing of substrate to ~60(-100V) possible
  - substrate resistivity ~10 Ohm*cm → $N_{eff} > 10^{14}/cm^3$
    - radiation induced N_{eff} insignificant even for innermost layers
  - depletion depth in the order of 10-20 μm → signal ~1-2 ke^-
  - on-sensor amplification possible - and necessary for good S/N
    - key: small pixel sizes → low capacitance → low noise
  - additional circuits possible, e.g. discriminator
    - beware of 'digital' crosstalk
  - full-sized radiation hard drift-based MAPS feasible, but challenging
    - aim for 'active sensors' in conjunction with rad-hard readout electronics first

- Scope of the presentation:
  - Introduce the concept
  - Flash some results with MAPS test chips
  - Present first measurements with the active sensor prototype chip
  - Disclaimer: Too many slides, some are just for your reference...

A HV-CMOS sensor...

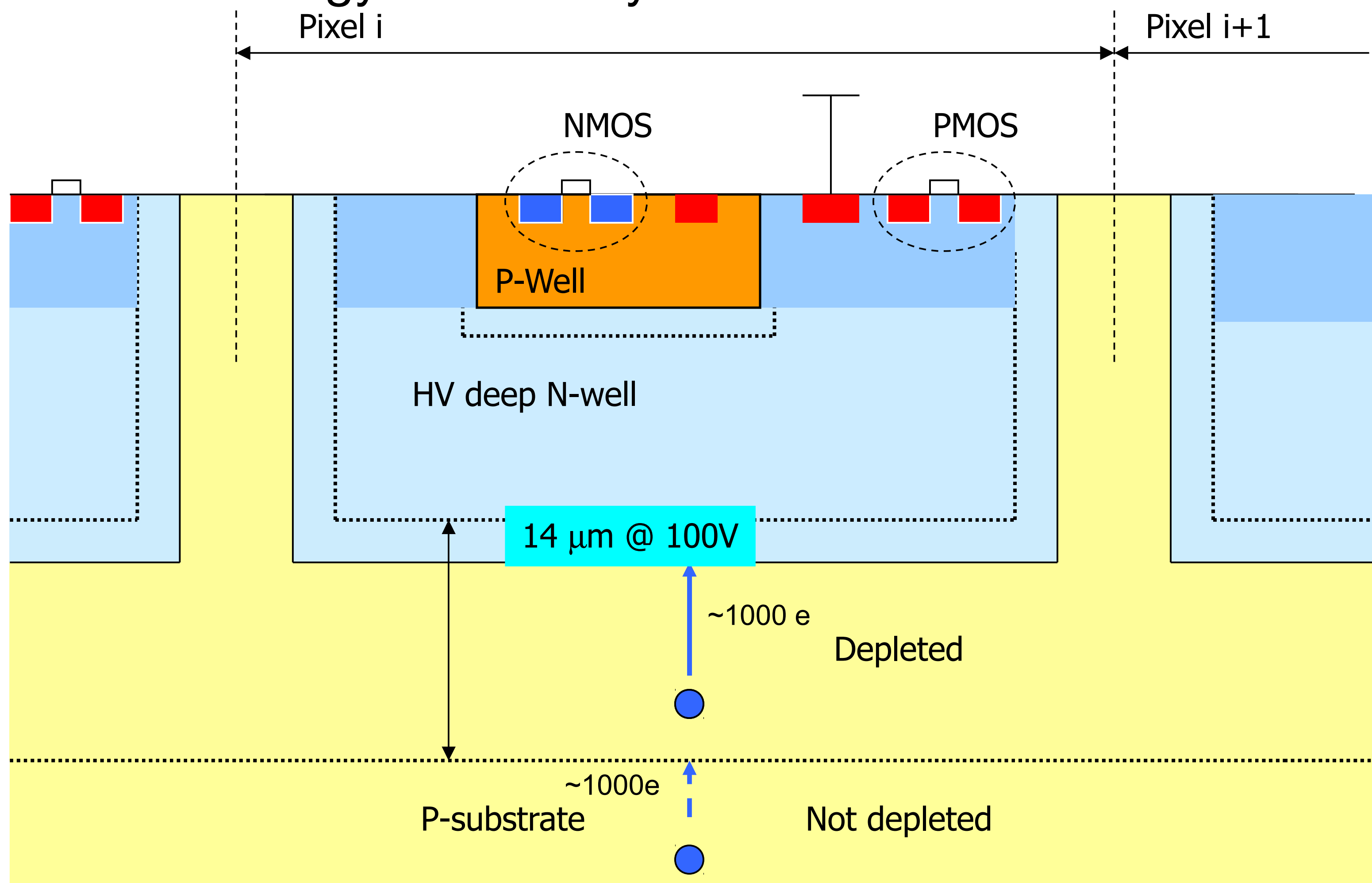
- essentially a standard n-in-p sensor
- depletion zone 10-20 µm: signal in the order of 1-2ke$^-$
  - challenging for hybrid pixel readout electronics
    - new ATLAS ROC FE-I4 might be able to reach this region – but no margin



The depleted high-voltage diode used as sensor (n-well in p-substrate diode)

...including active circuits: *smart diode array (SDA)*

- implementation of
  - first amplifier stages
  - additional cuircuits: discriminators, impedance converters, logic, …
- deep sub-micron technology intrinsically rad-hard



CMOS electronics placed inside the diode (inside the n-well)

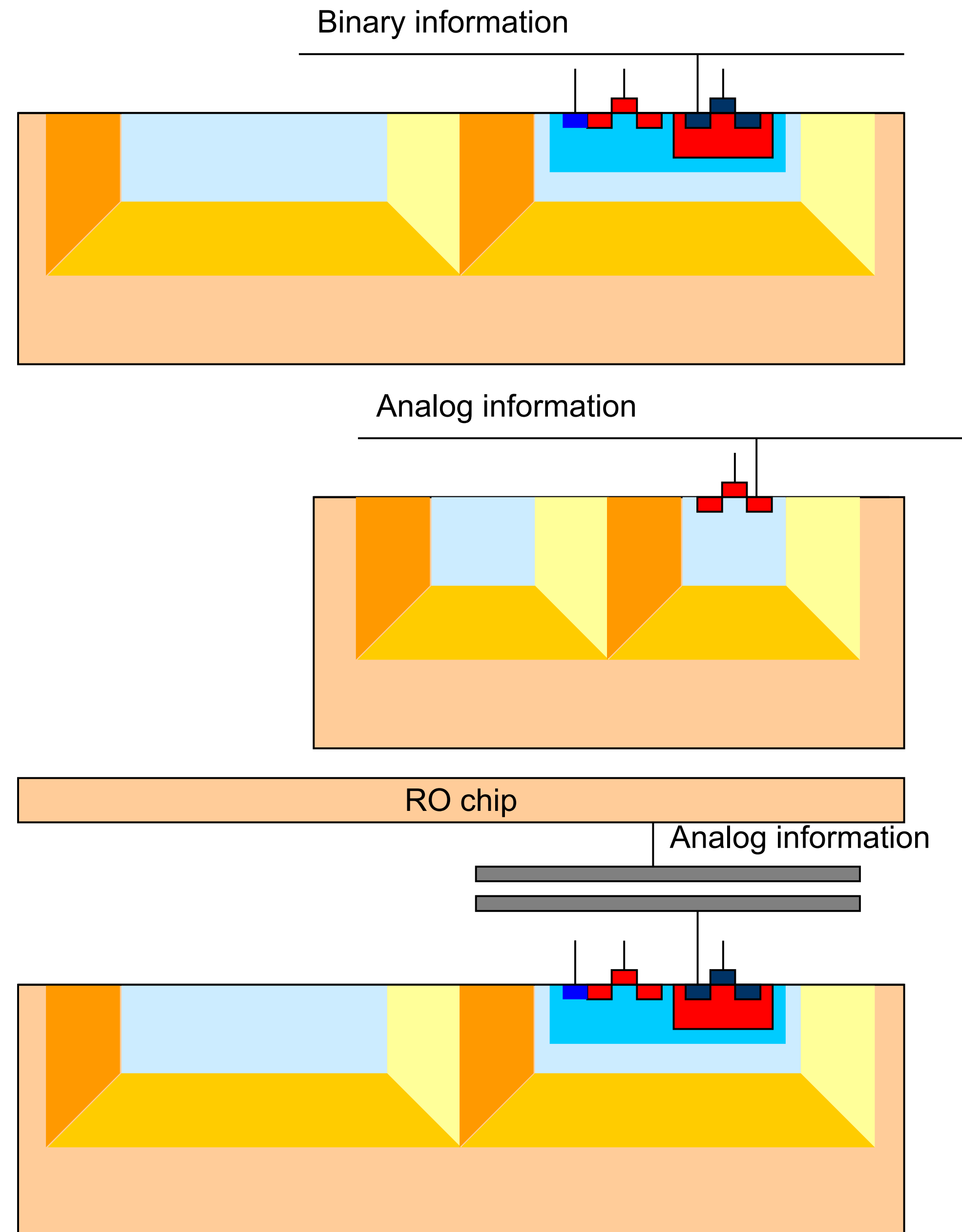
Prototypes

- Several test-chips already existing:

SDA with sparse readout
("intelligent" CMOS pixels)
HV2/MuPixel chip

SDA with frame readout
(simple PMOS pixels)
HVM chip

SDA with capacitive readout
("intelligent" pixels)
Capacitive coupled pixel detectors
CCPD1 and CCPD2 detectors



Prototype summaries

First chip – CMOS pixels
Hit detection in pixels
Binary RO
Pixel size 55x55µm
Noise: 60e
MIP seed pixel signal 1800 e
Time resolution 200ns

Bumpless hybrid detector

CCPD1 Chip
Bumpless hybrid detector
Based on capacitive chip to chip signal transfer
Pixel size 78x60µm
RO type: capacitive
Noise: 80e
MIP signal 1800e

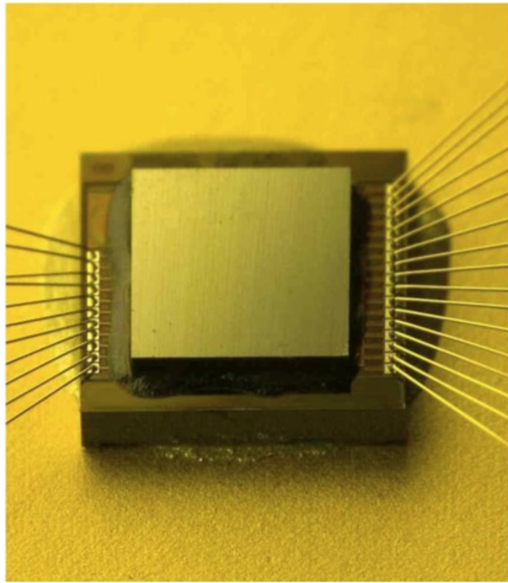
CCPD2 Chip
Edgeless CCPD
Pixel size 50x50µm
Noise: 30-40e
Time resolution 300ns
SNR 45-60

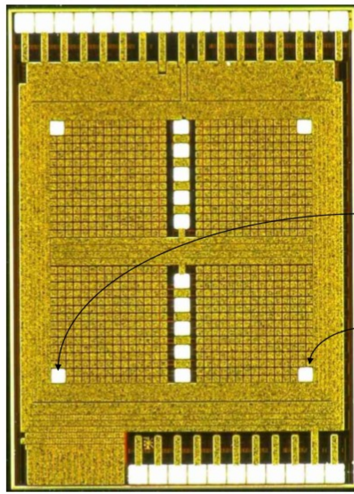
Irradiations of test pixels
60MRad – SNR 22 at 10C (CCPD1)
$10^{15}n_{eq}/cm^2$ – SNR 50 at 10C (CCPD2)

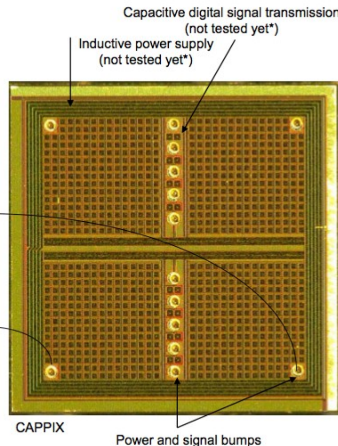
Frame readout - monolithic

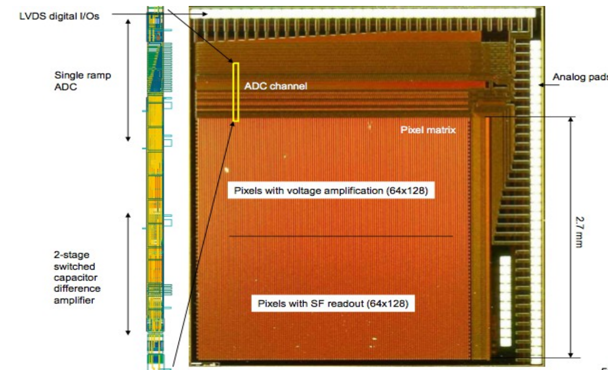
PM1 Chip
Pixel size 21x21µm
Frame mode readout
4 PMOS pixel electronics
128 on chip ADCs
Noise: 90e
Test-beam: MIP signal 2200e/1300e
Efficiency > 85% (timing problem)
Spatial resolution 7µm
Uniform detection

PM2 Chip
Noise: 21e (lab) - 44e (test beam)
Test beam: Detection efficiency 98%
Seed Pixel SNR ~ 27
Cluster Signal/Seed Pixel Noise ~ 47
Spatial resolution ~ 3.8 µm





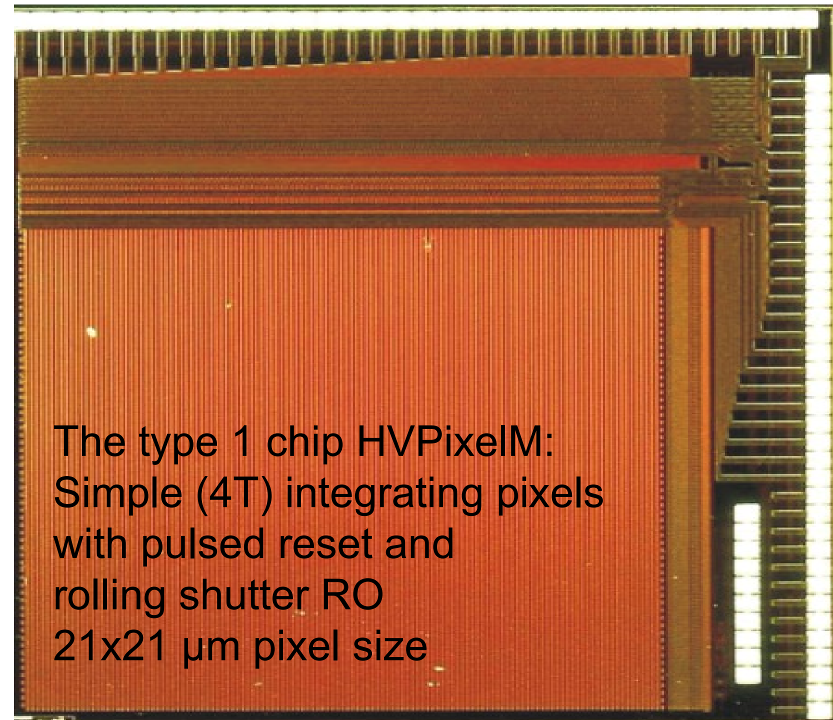


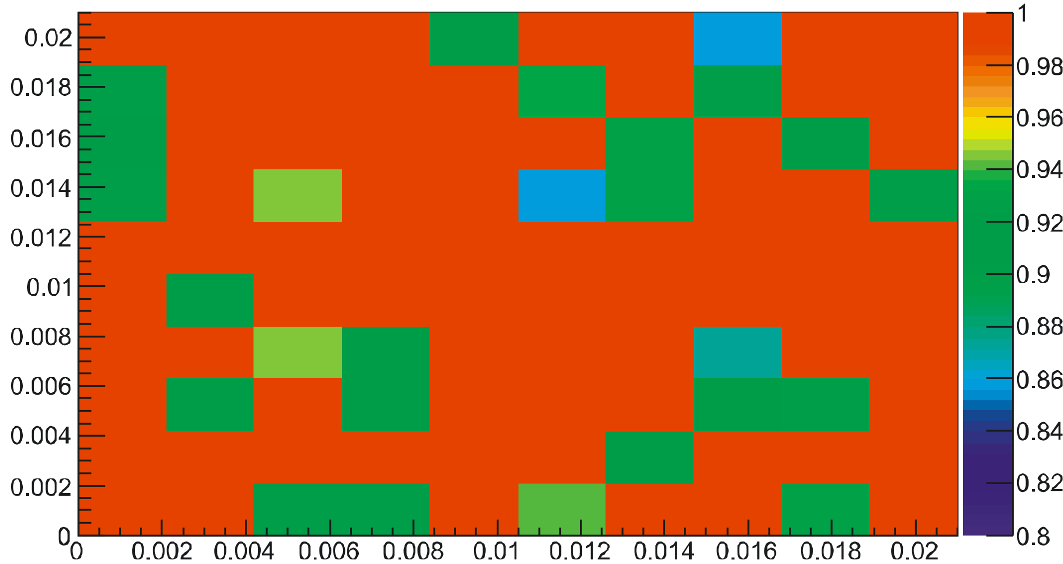


I. Peric

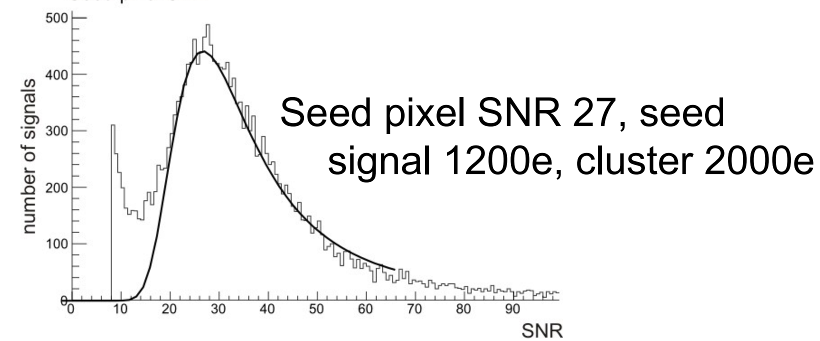
Test beam results: monolithic

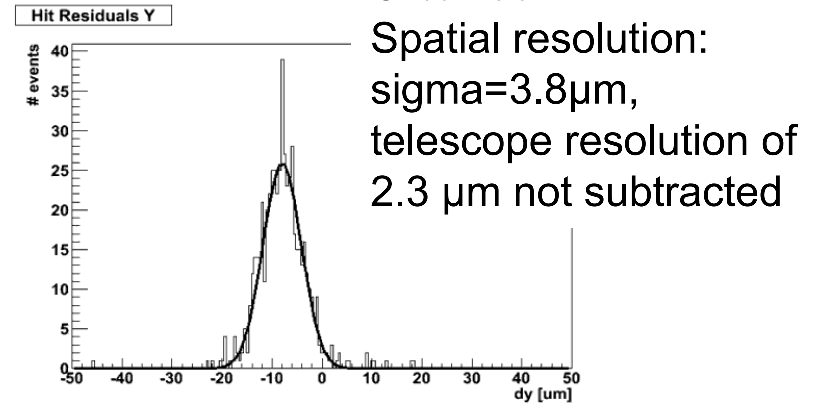
- excellent resolution
- very good S/N ratio
- efficiency limited by readout artifacts:
  - column-based readout
  - row not active during readout
  - data analysis did not correct for this
  - very small chip → low statistics





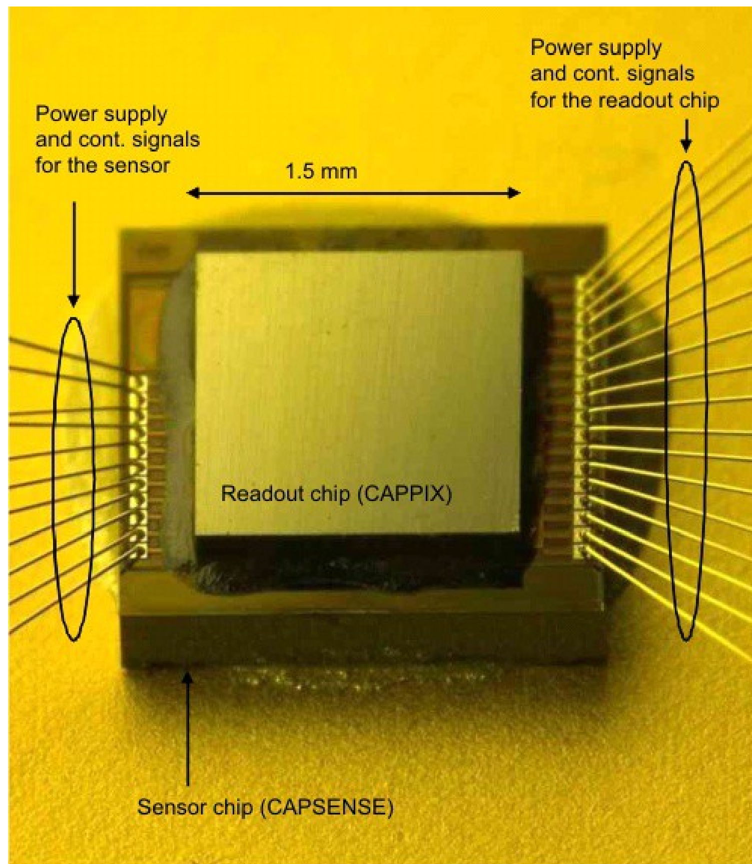
Efficiency vs. the in-pixel position of the fitted hit. Efficiency at TB: ~98% (probably due to a rolling shutter effect)



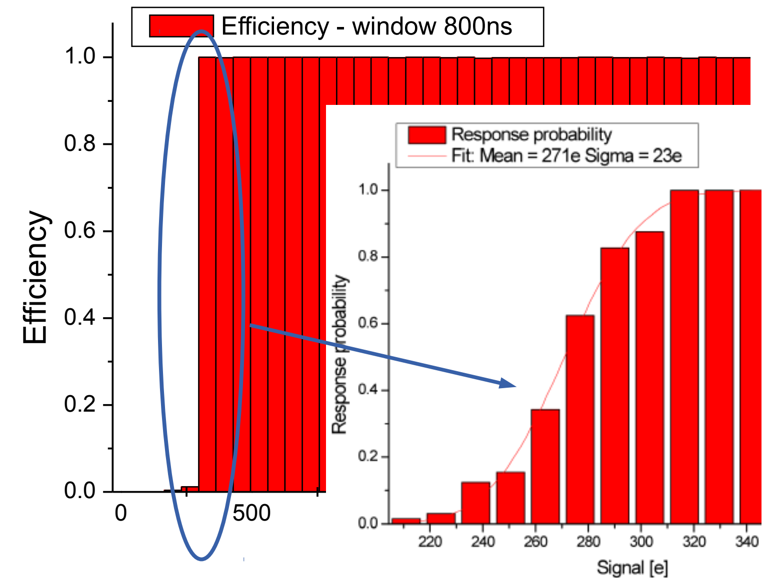


CPPD prototype results

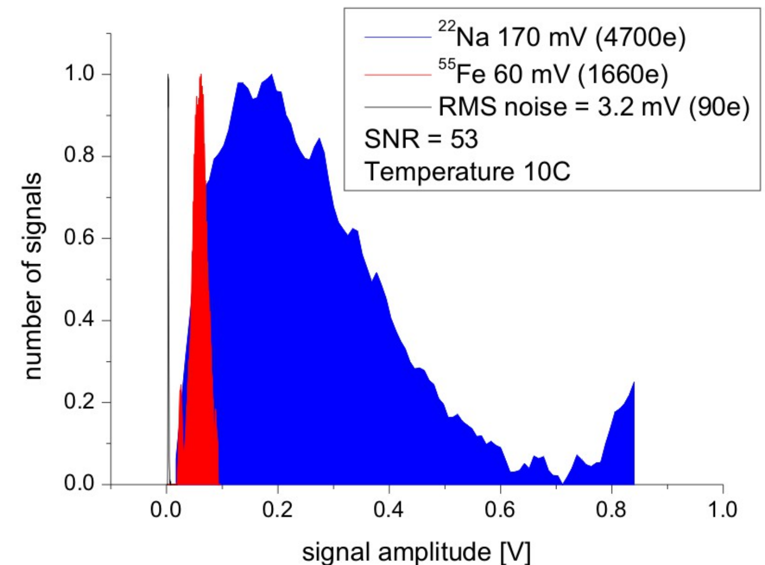
- excellent noise behaviour: stable threshold at ~330 electrons
- good performance also after irradiation



CAPPIX/CAPSENSE edgeless CCPD
50x50 μm pixel size



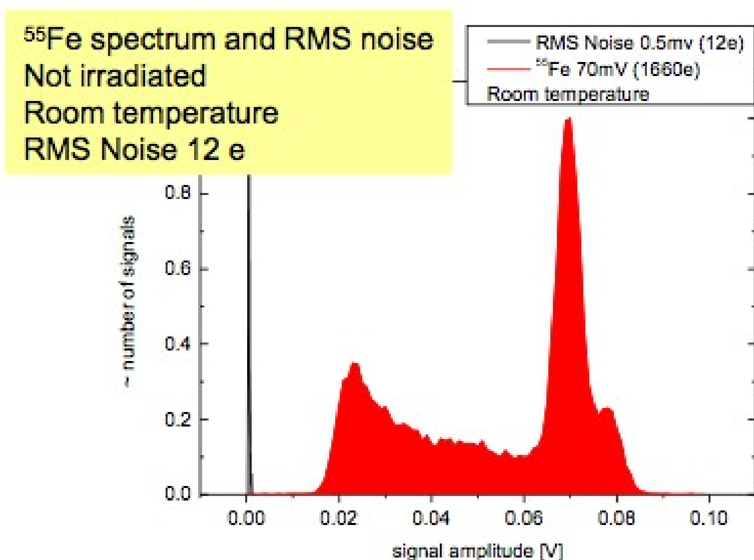
Detection efficiency vs. amplitude
Detection of signals above 330e possible with >99% efficiency.

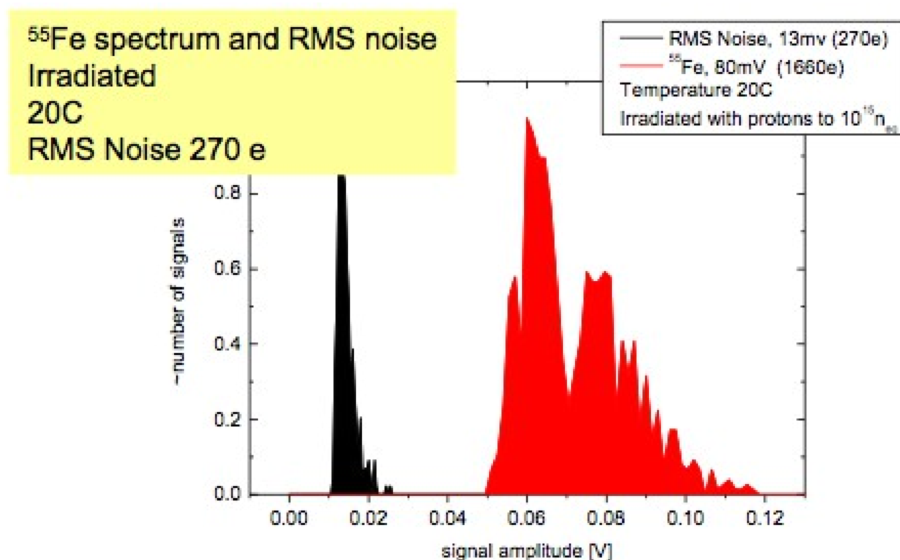


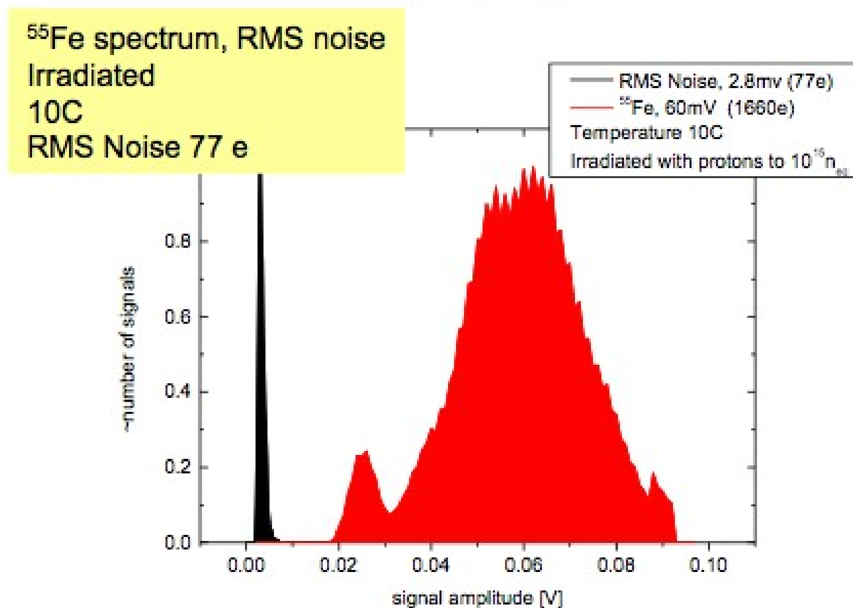
Signals and noise of a CAPSENSE pixel after $10^{15} n_{eq}/cm^2$

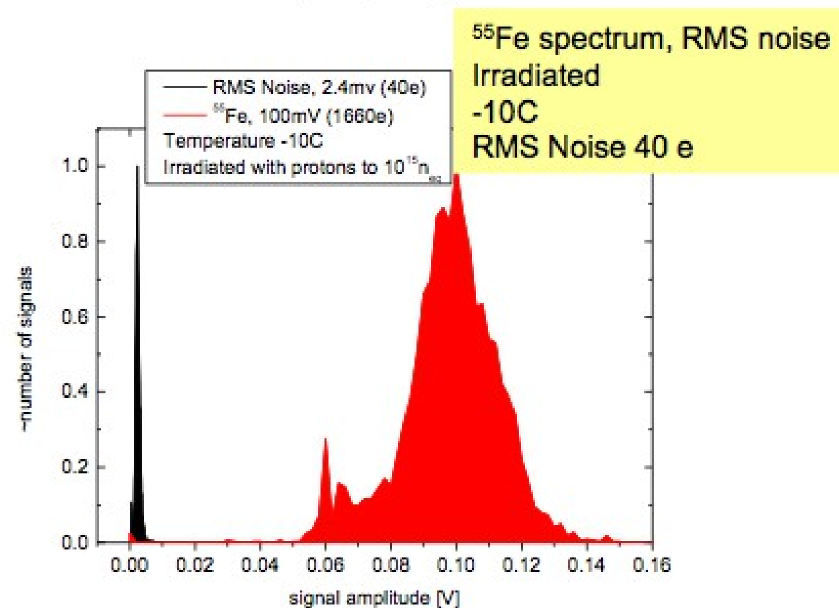
CPPD prototype results

- Irradiation with 23 MeV protons: 1e15 neq/cm2, 150MRad
- FE-55 performance recovers after slight cooling



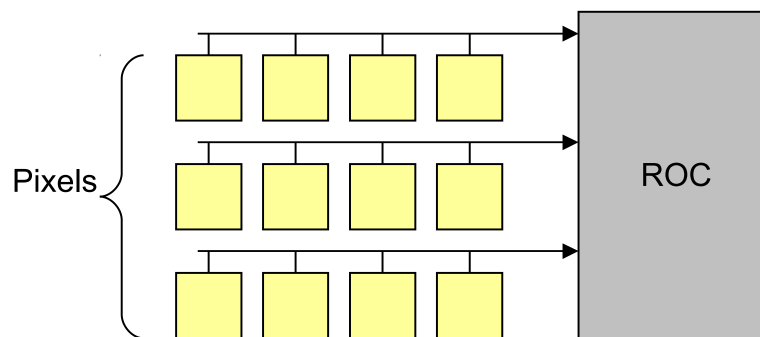






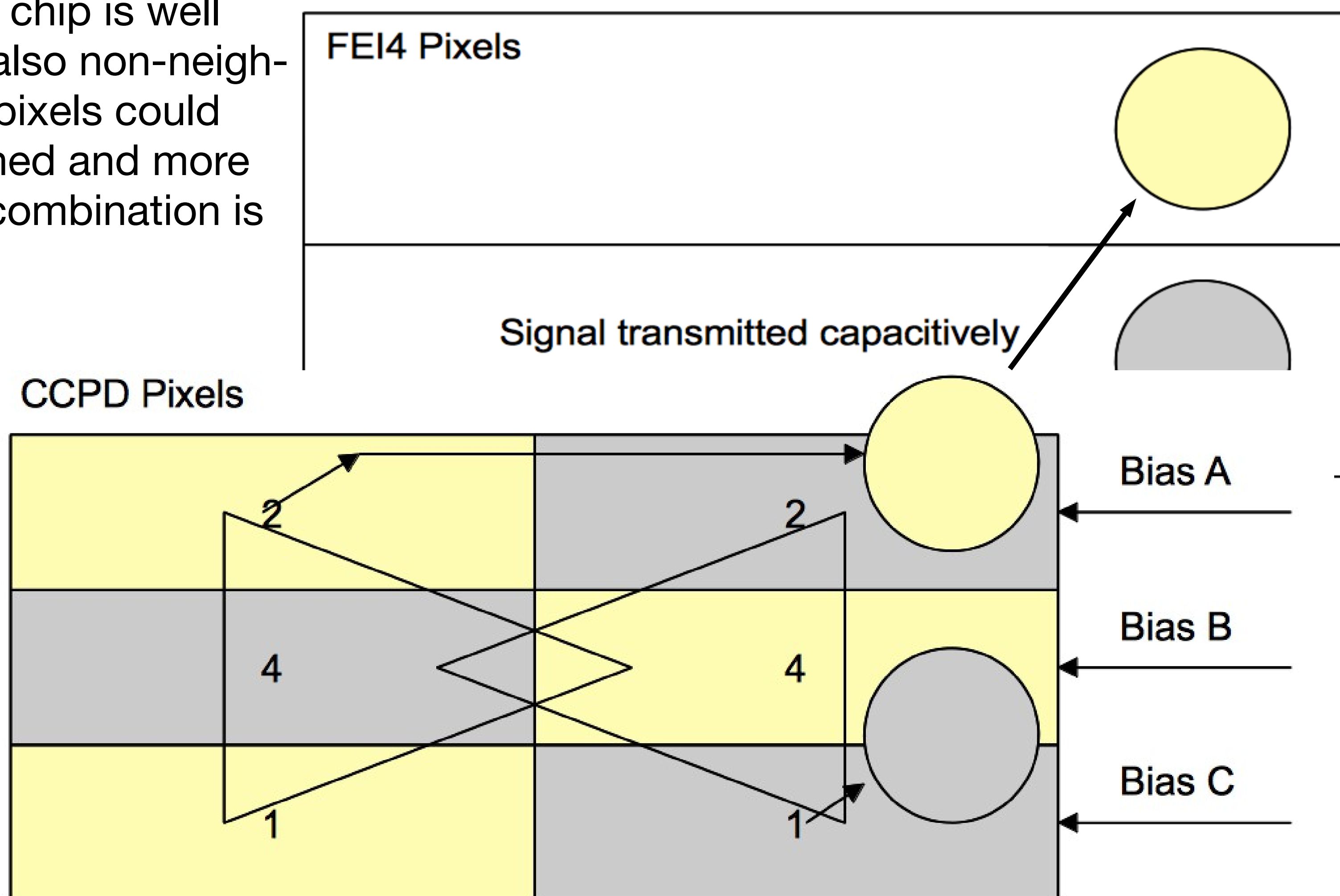
From MAPS to active sensors

- Existing prototypes would not suitable for HL-LHC, mainly because
  - readout too slow
  - time resolution not compatible with 40 MHz operation
  - high-speed digital circuits might affect noise performance
- Idea: use HV-CMOS as sensor in combination with existing readout technology
  - fully transparent, can be easily compared to other sensors
  - can be combined with several readout chips
  - makes use of highly optimised readout circuits
  - can be seen as first step towards a sensor being integrated into a 3D-stacked readout chip (not only analogue circuits but also charge collection)
- Basic building blocks: *small* pixels (low capacitance, low noise)
  - can be connected in any conceivable way to match existing readout granularity, e.g.
    - (larger) pixels
    - strips



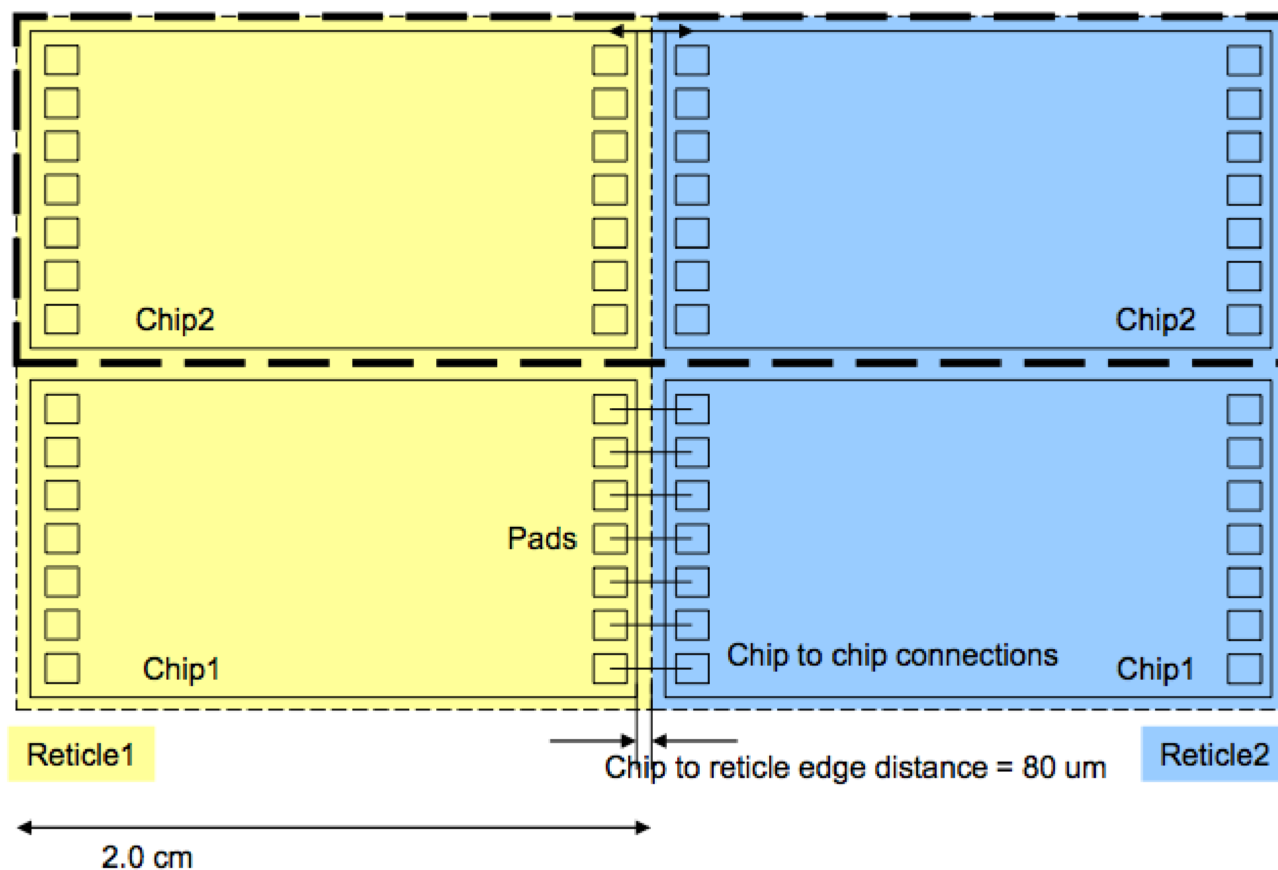
Pixels: sizes and combinations

- Possible/sensible pixel sizes: 20x20 to 50x125 µm
  - 50x250 µm (current ATLAS FE-I4 chip) too large
  - combine several sensor “sub-pixels” to one ROC-pixel
    - sub-Pixels encode their address/position into the signal as pulse-height-information instead of signal proportional to collected charge
    - routing on chip is well possible, also non-neighbour sub-pixels could be combined and more than one combination is possible



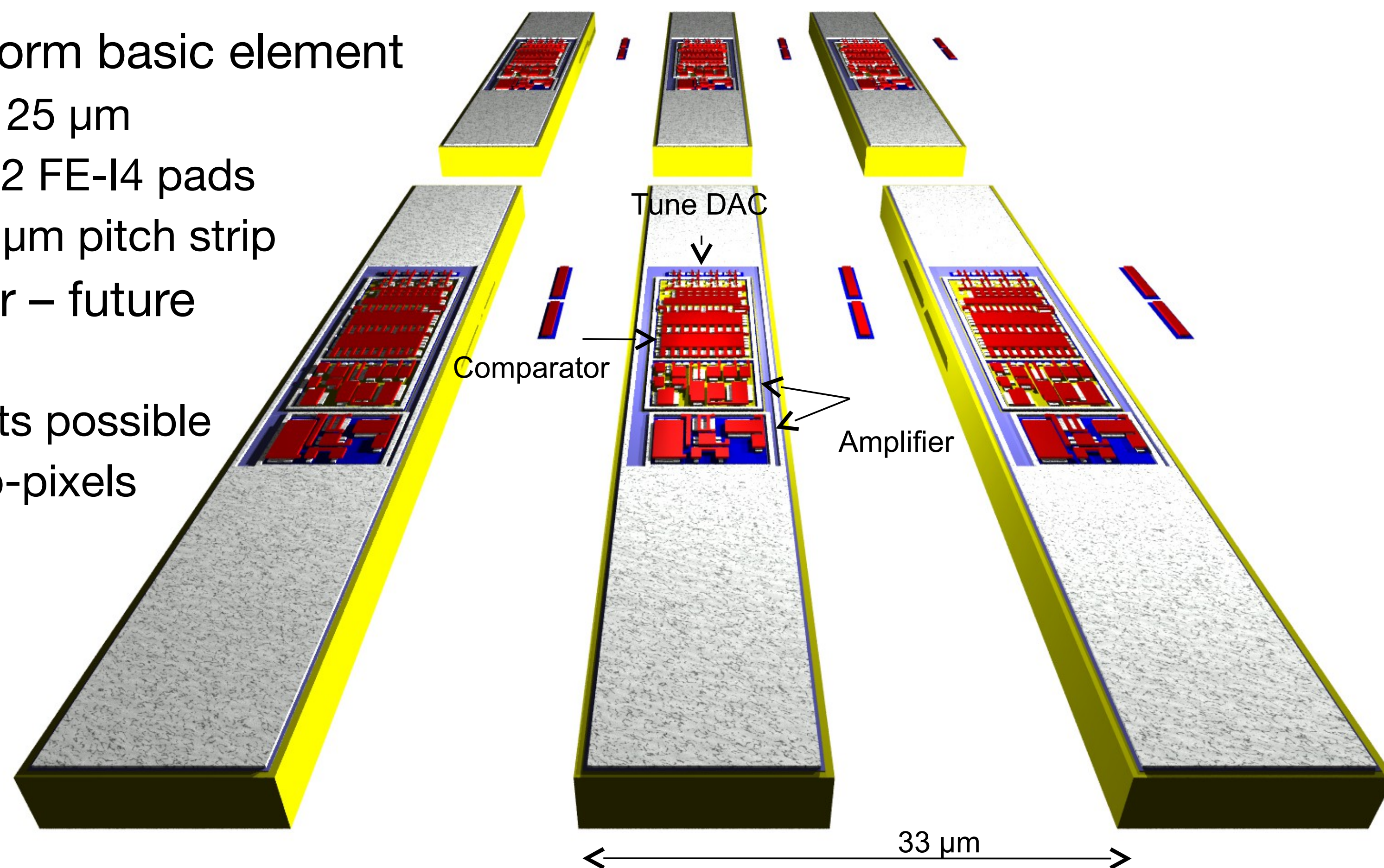
Reticule size/stitching

- Sensor size is currently limited by reticule size of ~2x2 cm
  - however, the yield should be excellent (very simple circuit, essentially no “central” parts) so it might be interesting to cut large arrays of sensors from a wafer and connect individual reticules by
    - wire-bonding
    - post-processing (one metal layer, large feature size)
- There are HV-CMOS processes/foundries which allow for stitching
- Very slim dicing streets
  - Gaps between 1-chip modules could be rather narrow



HV2FEI4

- A combined active strip/pixel sensor was designed and produced
  - strips compatible with ATLAS ABCN and LHCb/Alibava Beetle
  - pixels match new ATLAS FE-I4 readout chip
    - capacitive coupling
    - bump-bonding possible
- Structure
  - 6 sub-pixels form basic element
    - each 33 x 125 µm
    - connect to 2 FE-I4 pads
    - form a 100 µm pitch strip
  - small fill factor – future options:
    - more circuits possible
    - smaller sub-pixels

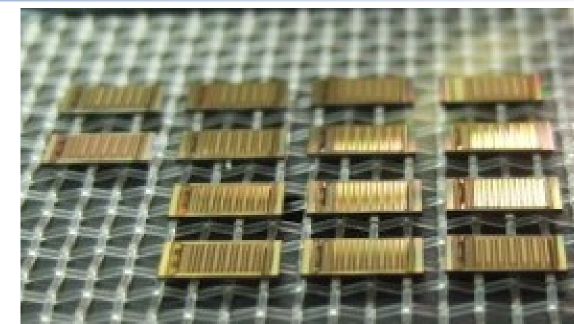


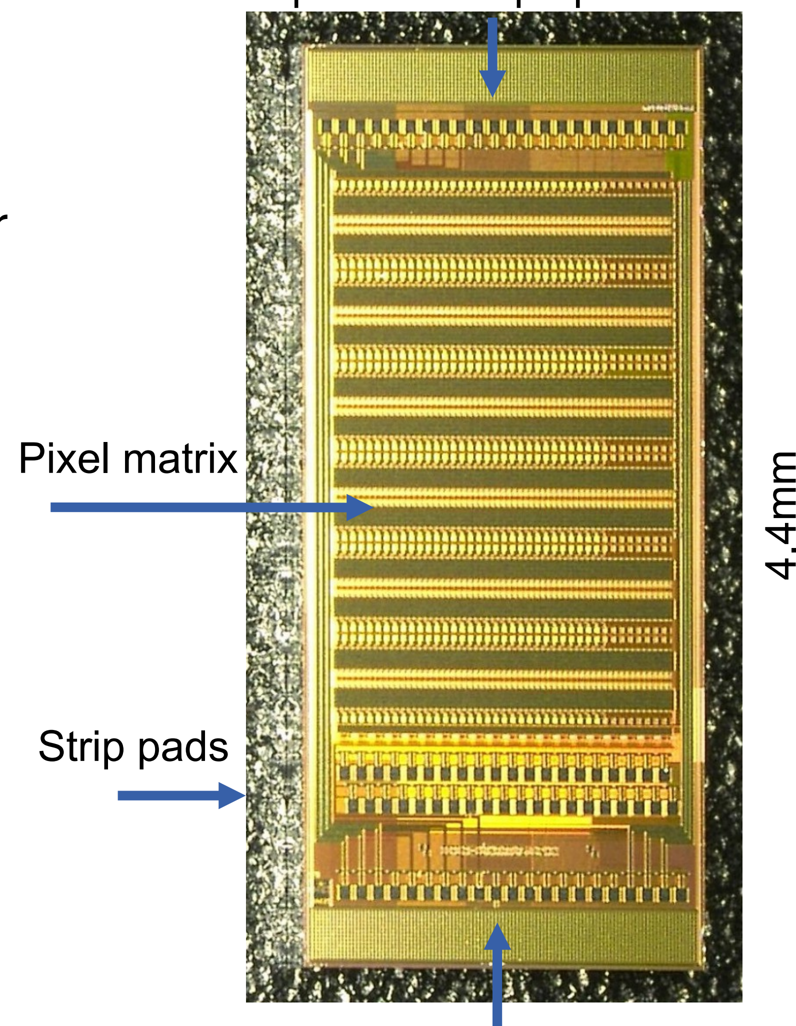
HV2FEI4

- Chip size: 2.2mm x 4.4mm
- Pixel matrix: 60x24 (sub-)pixels of 33 μm x 125 μm
- 21 IO pads at the lower side for CCPD operation
- 40 strip-readout pads (100 μm pitch) at the lower side and 22 IO pads at the upper side for (virtual) strip operation
- On chip bias DACs
- Pixels contain charge sensitive amplifier, comparator and tune DAC
- Configuration via FPGA or μC: 4 CMOS lines (1.8V)

3 possible operation modes

- standalone on test PCB
- strip-like operation
- pixel (FE-I4) readout





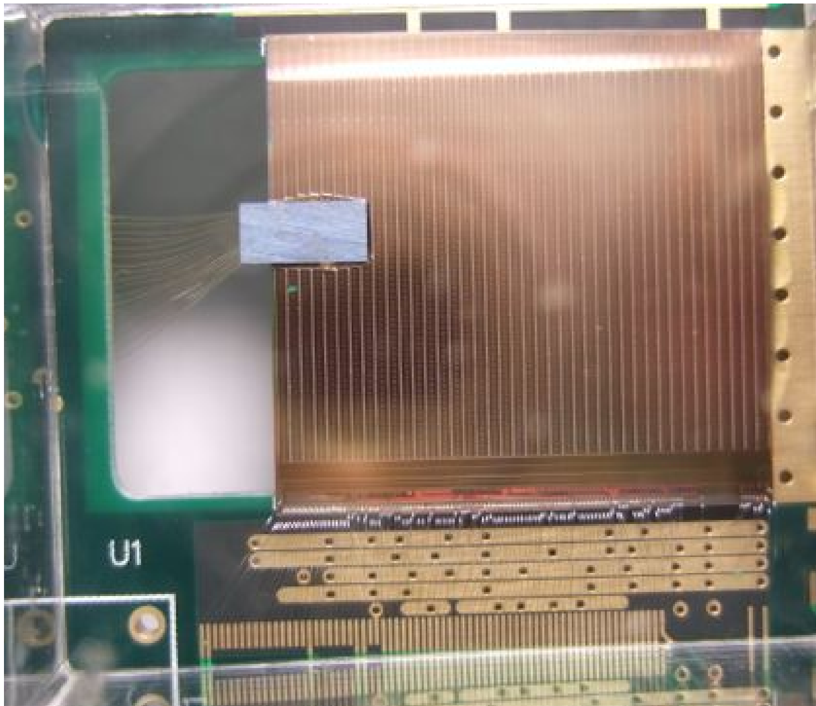
HV2FEI4: characterisation

Standalone tests

- first measurements at Heidelberg/Mannheim
- behaviour as expected
- monitor output showing physics (radioactive source events)

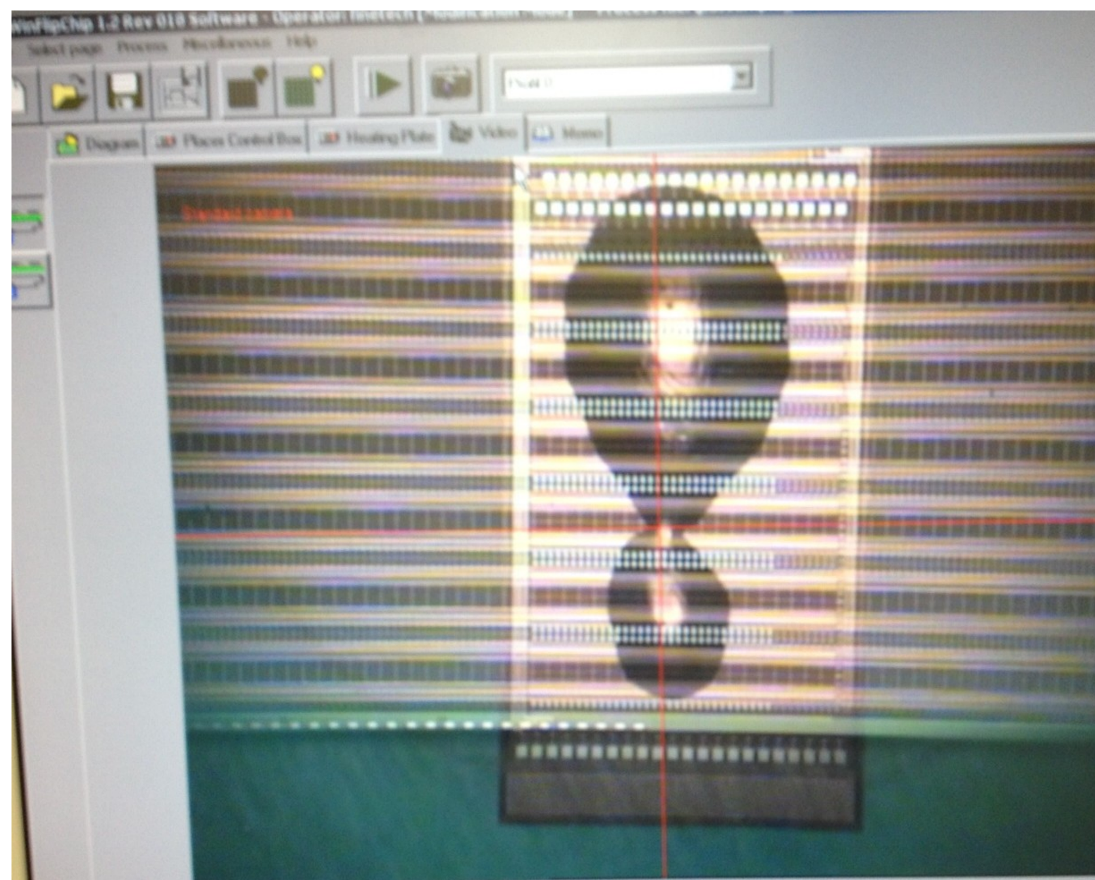
HV2FEI4: Pixel readout

- First HV2FEI4s glued (!) to FE-I4A and FE-I4B
- HV2FEI4 wirebonds done through hole in PCB
  - could be bumps, anisotropic glue or TSVs later



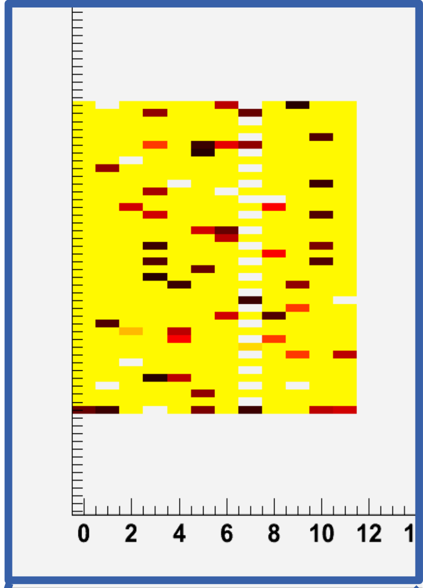
HV2FEI4: Gluing

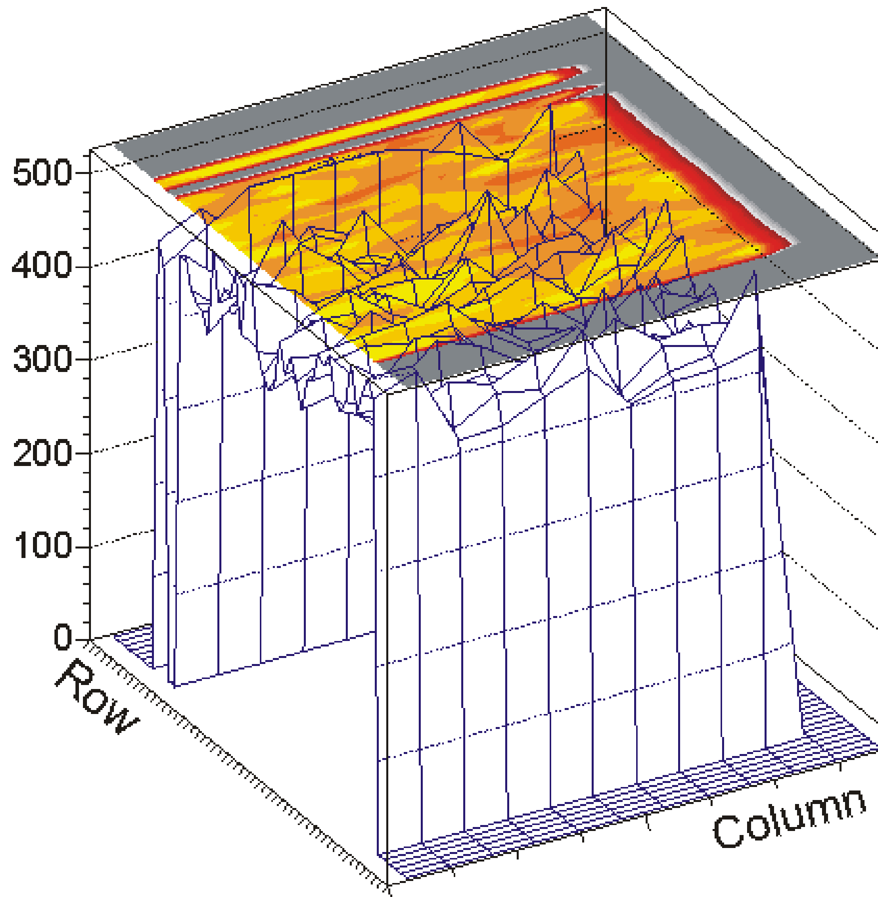
- Required alignment precision estimated to better than 10µm
  - bump pads on FE-I4 in this order of magnitude
  - easy to reach with bump-bonding machines (best quote <1µm precision)
- Up to now gluing trials done with
  - epoxy-based 12.5 µm thick lamination glue sheet
    - tricky handling, fairly thick
  - liquid 2-component epoxy glue
    - very small amounts of glue necessary, how to apply in a reproducible way?
    - distribution by pressure, what pattern to choose for larger areas?
      - first measurements indicate a glue thickness of <3µm (!)
    - issues from air bubbles and/or inhomogenious glue thickness?

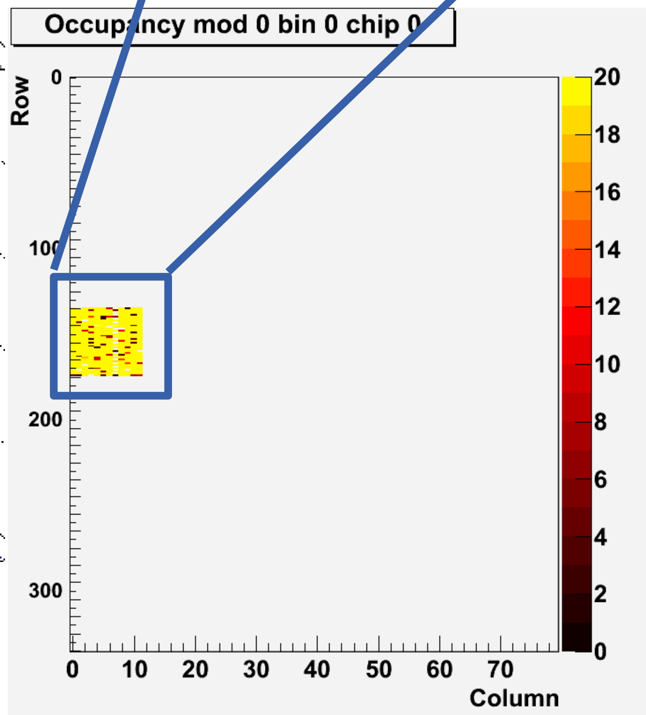


HV2FEI4: Pixel readout

- First measurement:
  - FE-I4A (w/ bumps) sees HV2FEI4 being glued to it
  - Physics (^{22}Na source) is seen by FE-I4B (w/o bumps)
  - Homogeneity to be checked
    - few pixels with less entries
    - looks like many with more entries
      - cross-talk?

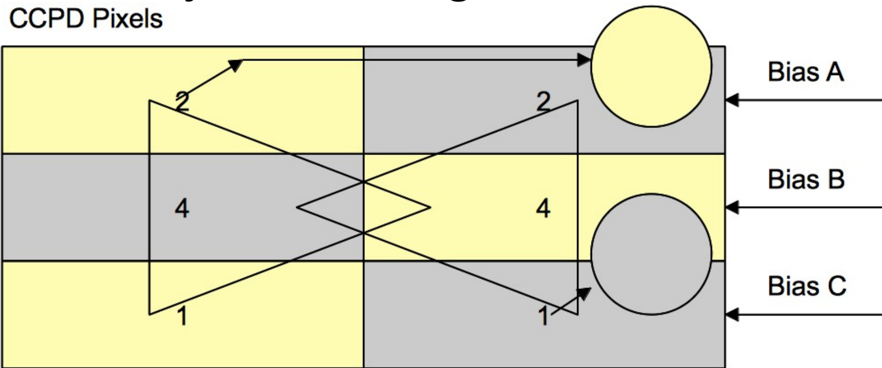


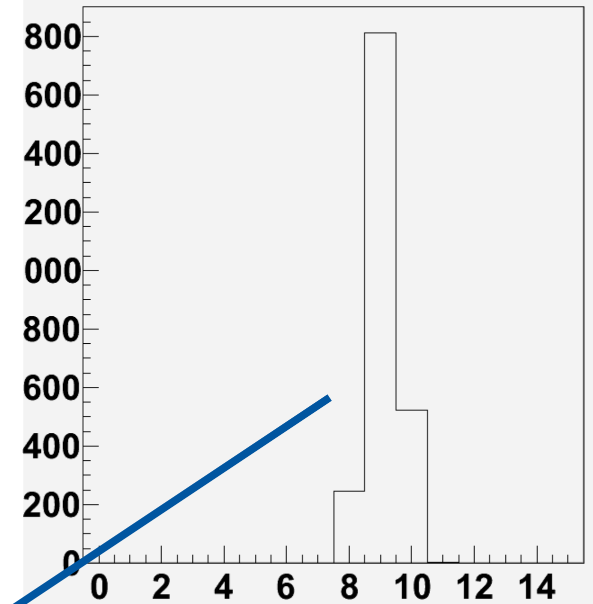




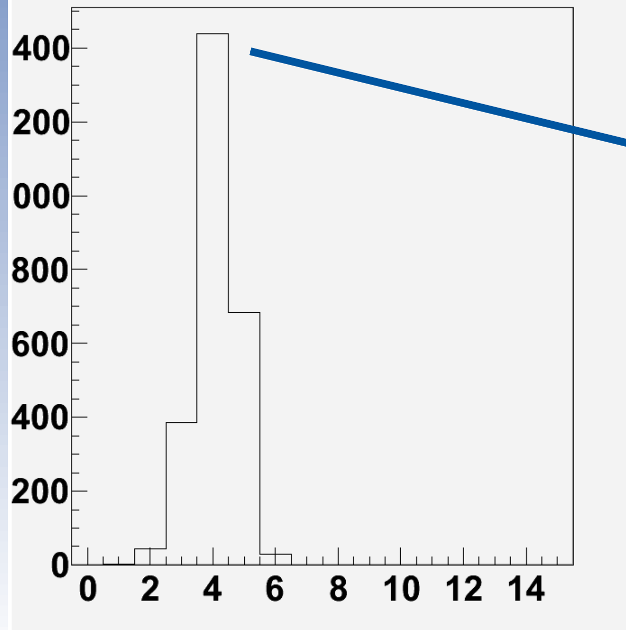
HV2FEI4: Pixel readout

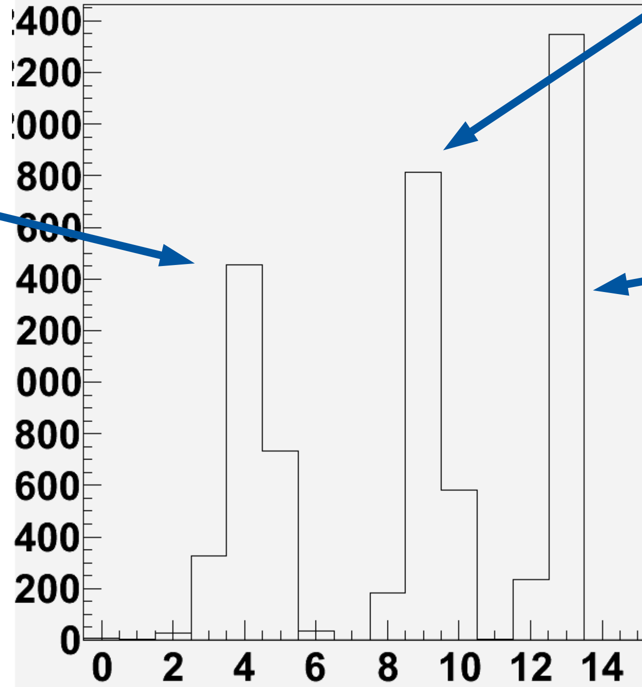
- ToT encoding:
  - 3 sub-pixels clearly distinguishable
    → sub-pixel encoding works!
  - dynamic ranges to be better matched

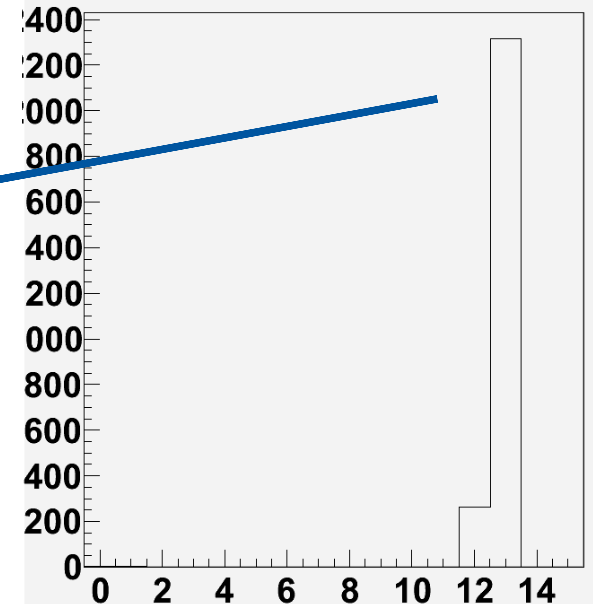




All on



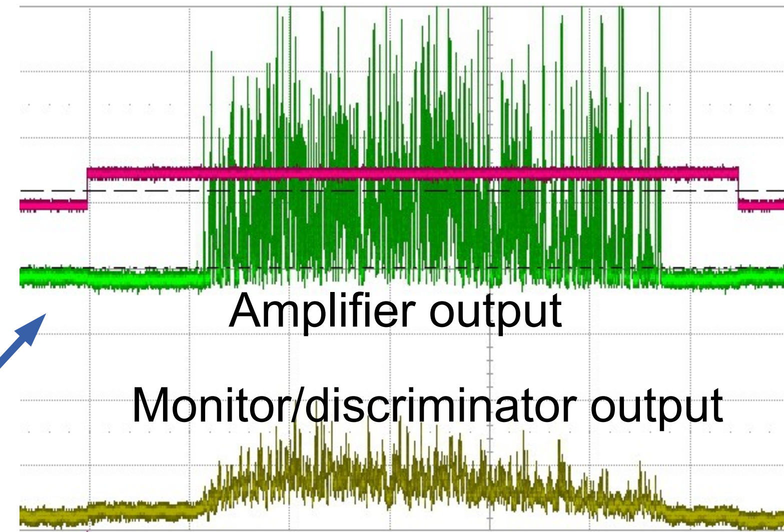




HV2FEI4: irradiation

Standalone tests: irradiation

- at CERN/PS on special PCB allowing for remote operation
- HV2FEI4 powered and read-out during irradiation
  - low-intensity beam, before irradiation



RS232

DE2 board

LVDS 20m long cable

4 signals

5V max

3,3V

io

Lvds

5m

4 signals

Monitor signal 20m long cable

Monitor signal

0,4V max

HV2FEI4

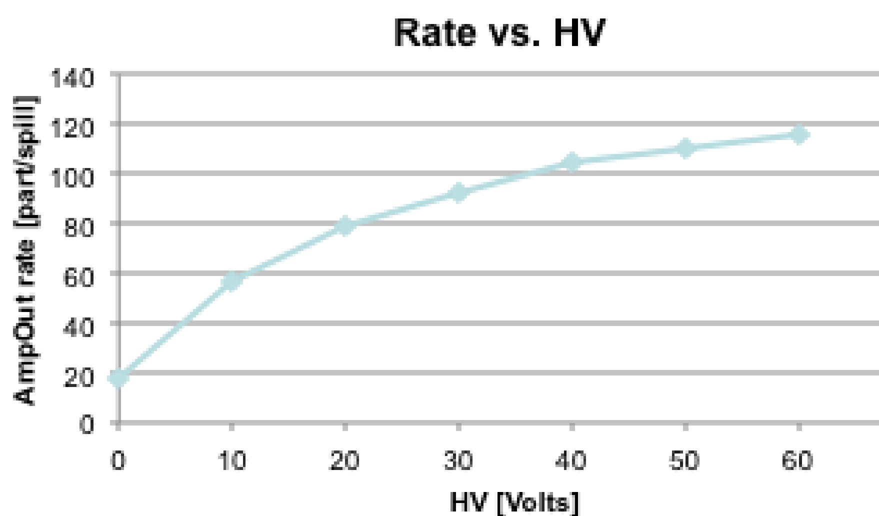
Board n°2

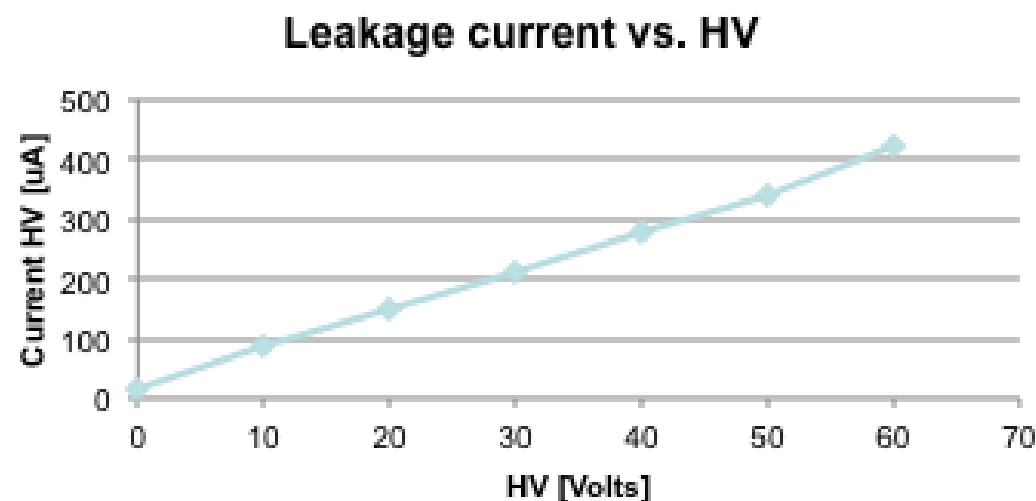
VDDA – VSSA – Threshold – Gate – HV

A. Rozanov

Results after 144 MRad

- The rate of detected particles depends on the high voltage bias, superposition of two effects:
  - Positive effect: The increase of HV bias leads to an increase of the depleted region depth => better detection efficiency.
  - Negative effect: The increase of the leakage current leads to a signal loss.
- Measured leakage current dependence on the high voltage bias
  - Leakage current depends on the volume of the depleted region





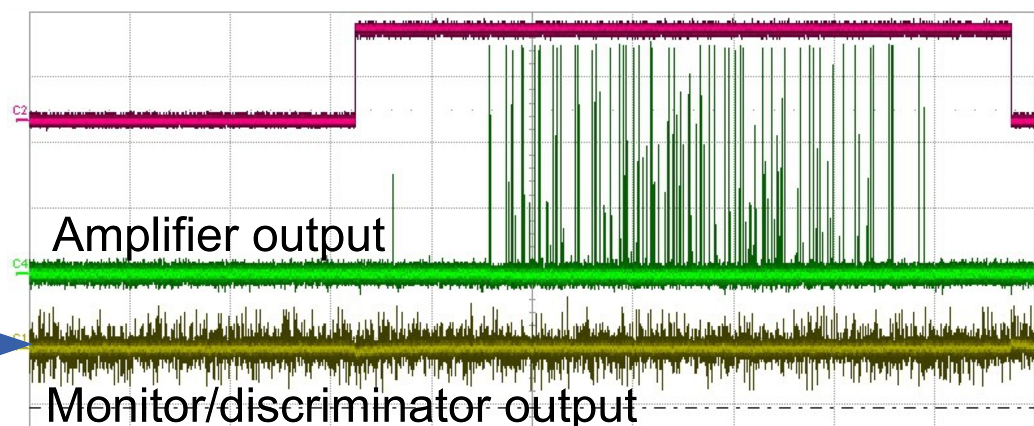
A. Rozanov

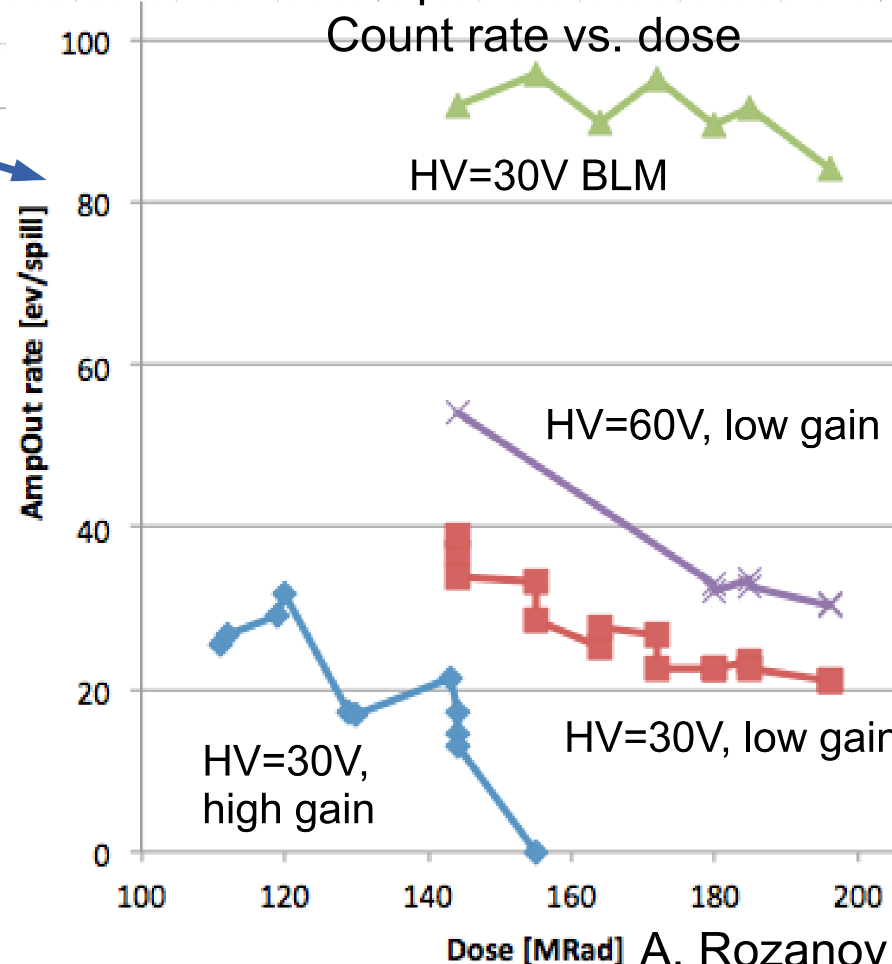
Results after 200 MRad

Preliminary irradiation results after ~200 Mrad (about IBL fluence!)

- significant radiation effects seen
  - discriminator output decreases with current settings after ~110 MRad
  - "lower" count rate, but physics still seen
    - high gain settings failing
    - low gain still works
  - strong leakage current increase (as expected): nA → ~mA
- full characterisation difficult:
  - limited access
  - radiation vs. temperature effects

Amplifier and monitor output after 195 MRad



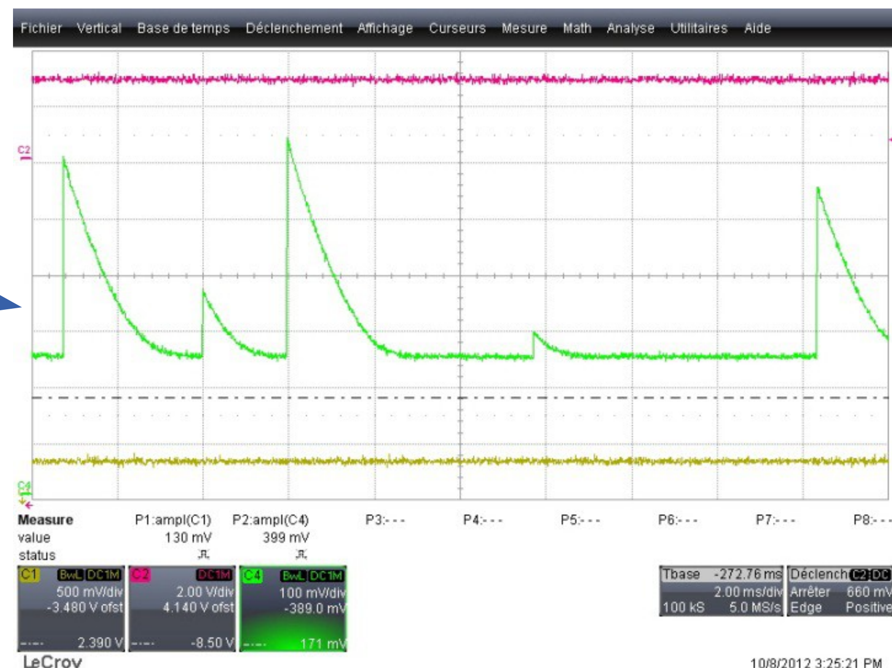


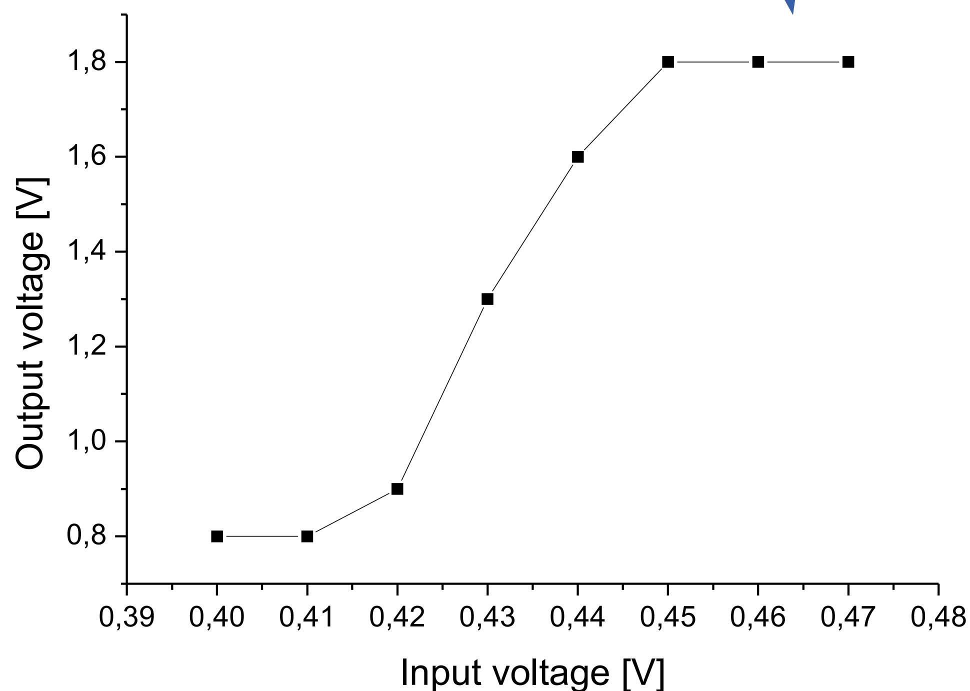
A. Rozanov

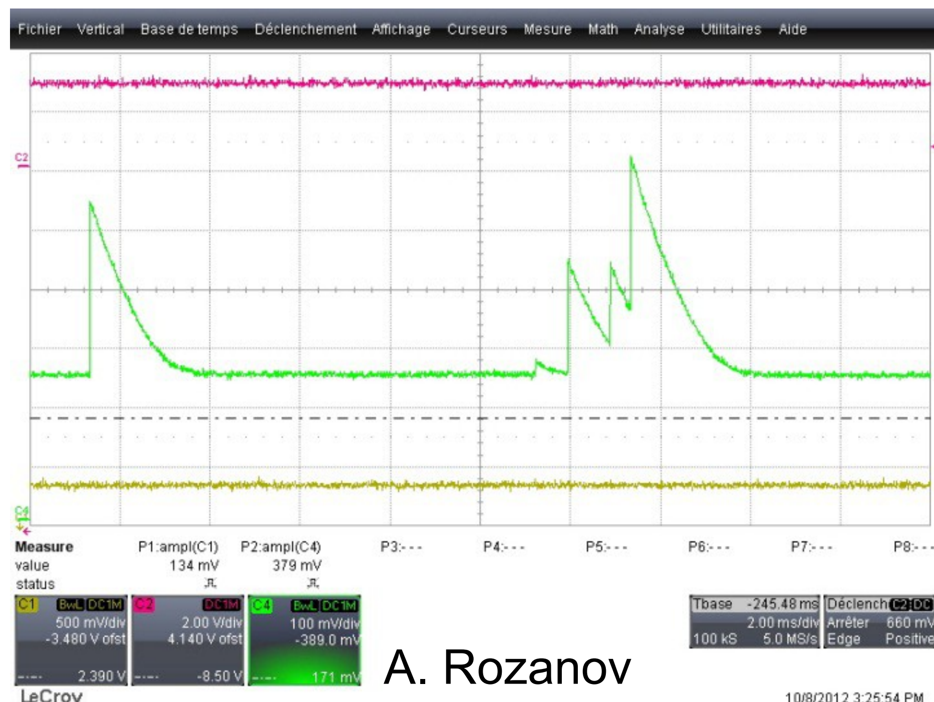
Results after 380 MRad and ~ 8 x 10^{15} n_{eq}/cm^2

Preliminary irradiation results:

- Output of the amplifier: the chip still works, particles are measured when the chip is in the beam
- Comparator characteristics
- many open questions, need better understanding







A. Rozanov

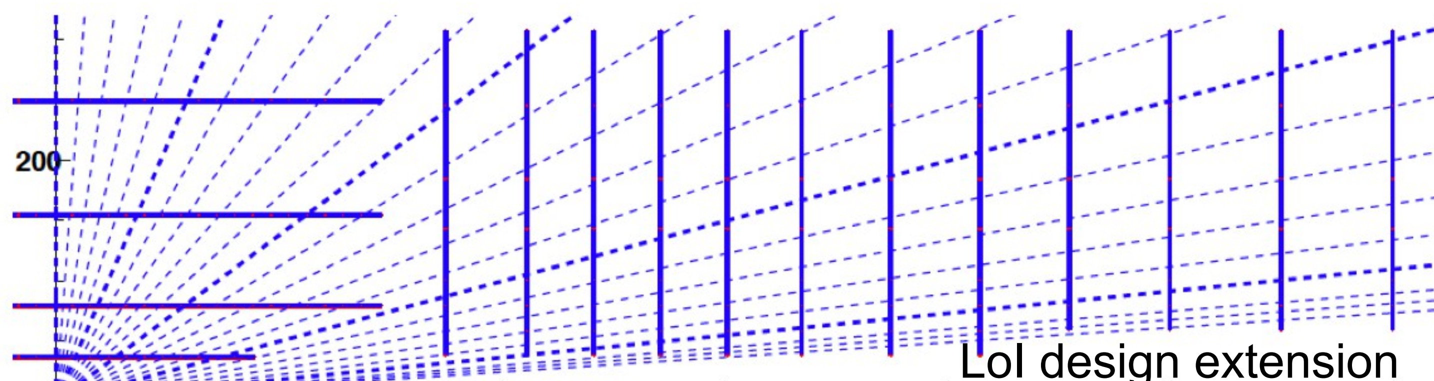
Future plans

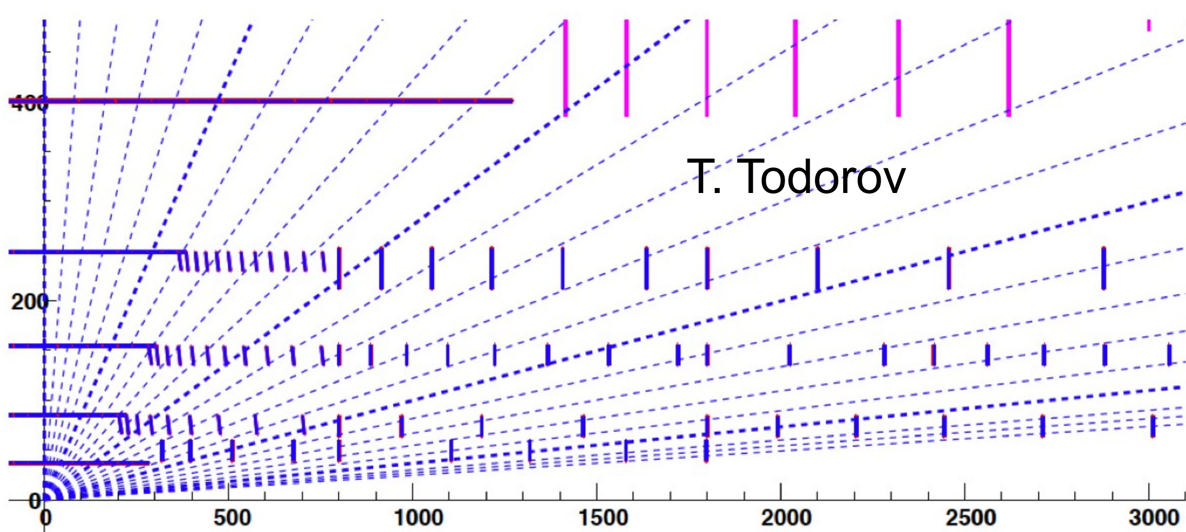
- More pixel assemblies being put together
  - several unirradiated
  - a bump-bonded one in preparation at Glasgow for comparison
  - 4 neutron-irradiated (1e15 and 1e16 neq/cm2)
- current HV2FEI4: standard design blocks on purpose (see how far we can get with standards), obviously radiation effects seen
  - experience with FE chips: 180nm technology can be rad-hard
- a modified HV2FEI4 chip was submitted in November
  - added guard rings for all NMOST
  - circular transistors at important positions
  - many other improvements
- further submissions are being discussed
  - dedicated to strip readout
    - optimised sub-strip pitch (40 μm? 20 μm?) in combination with z-resolution
  - dedicated to disks
    - square pixels preferred
    - 50x50 μm should be achievable with FE-I4
    - sensor candidate for “standard disks” and for very forward tracking

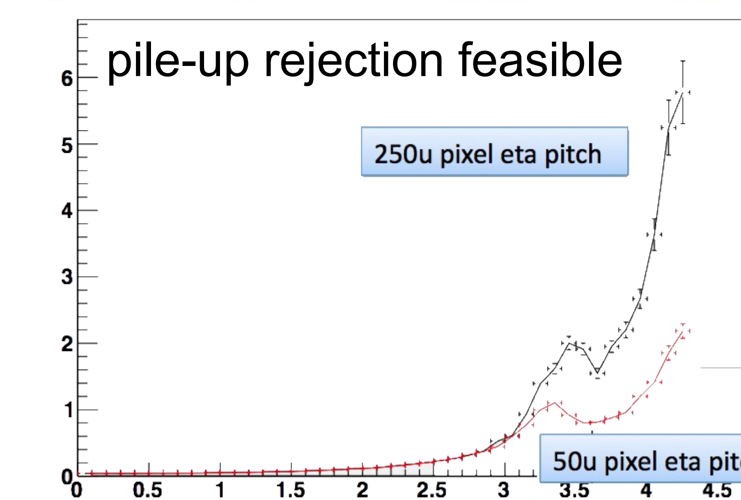
Case study: Very forward tracking

- Limitation to pseudorapidity of eta = 2.5 inappropriate wrt VBF/VBS
- Design studies ongoing for an extension to eta~4 (phase 2 upgrade)
  - physics: Higgs self-coupling, vector boson scattering
  - layout: acceptable area increase
  - sensor challenges: mass production, rad-hardness at small radii, square pixels/small eta pitch preferred → HV-CMOS?

Alpine stave design extension







Conclusions

- HV-CMOS processes might yield radiation-hard, low-cost, improved-resolution, low-bias-voltage, low-mass sensors
- First test chips indicate rad-hardness up to at least 1e15 n_{eq}/cm^2
  - general principles suggest rad-hardness up to full HL-LHC fluence
- Process can be used for
  - 'active' n-in-p sensors with capacitive coupling
  - drift-based MAPS chips (baseline for μ3e-Experiment)
- First active sensor prototypes being explored within ATLAS
  - capacitively coupled pixel sensors – first results look promising
  - “virtual” strip sensors – z-position encoding working