# Performance of capacitively coupled active pixel sensors in 180 nm HV CMOS technology irradiated to HL-LHC fluences

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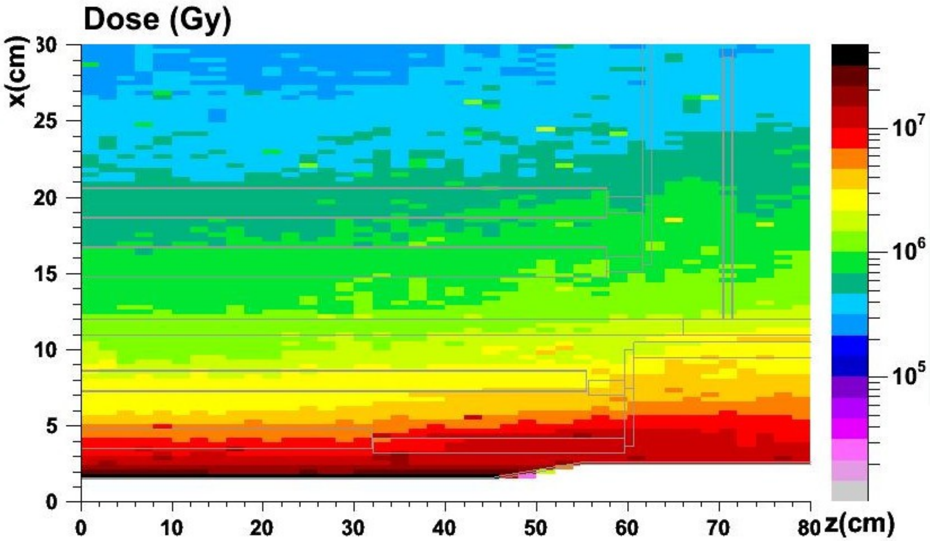
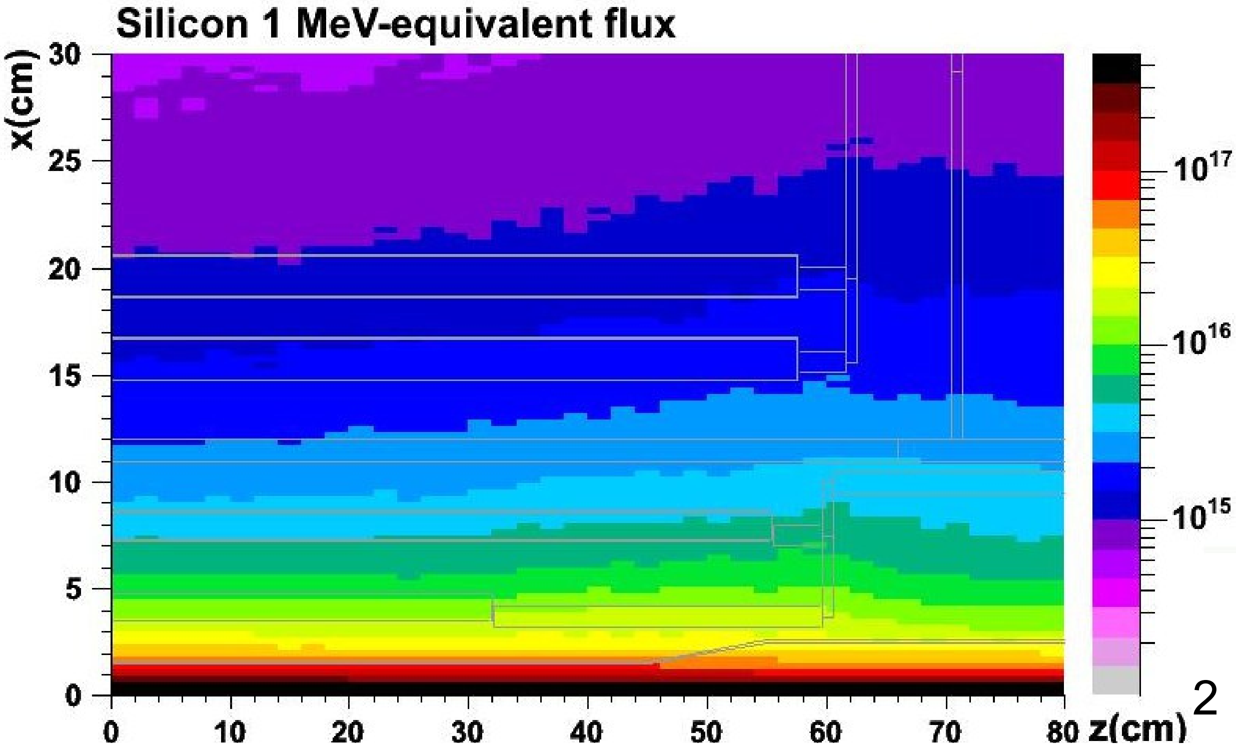
*on behalf of the participating institutes:*

*U Bonn, CERN, CPPM Marseille, U Geneva,*
*U Glasgow, U Heidelberg, LBNL*

# Reminder: fluences at HL-LHC

- integrated luminosity: 3000 $fb^{-1}$
- including a safety factor of 2 to account for all uncertainties this yields for ATLAS:
  - at 5 cm radius:
    - ~$2 \cdot 10^{16}$ $n_{eq}$ $cm^{-2}$
    - ~1500 MRad
  - at 25 cm radius
    - up to $10^{15}$ $n_{eq}$ $cm^{-2}$
    - ~100 MRad
    - several $m^2$ of silicon
  - strip region
    - some $10^{14}$ $n_{eq}$ $cm^{-2}$
    - up to ~100 $m^2$ of silicon

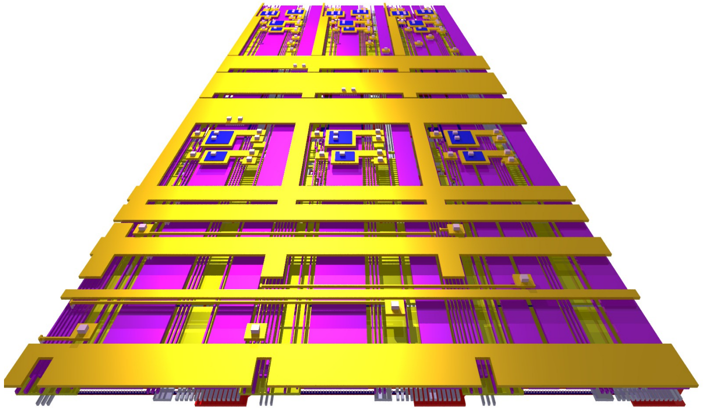

Dose (Gy)


Silicon 1 MeV-equivalent flux

# Implications

- High fluences: trapping dominant
  - reduce drift distance, increase field → reduce drift time:
    - 3D sensors
    - thin silicon
    - low depletion depth 'on purpose' to increase field:
      - low(er) resistivity silicon
      - dedicated annealing to increase $N_{eff}$
- Large areas: low cost of prime importance
  - industrialised processes
  - large wafer sizes
  - cheap interconnection technologies
- **Idea: explore industry standard CMOS processes as sensors**
  - commercially available by variety of foundries
    - large volumes, more than one vendor possible
  - 8” to 12” wafers
    - low cost per area: “as cheap as chips”
  - (partially too) low resistivity p-type Cz silicon
    - thin active layer
    - wafer thinning possible

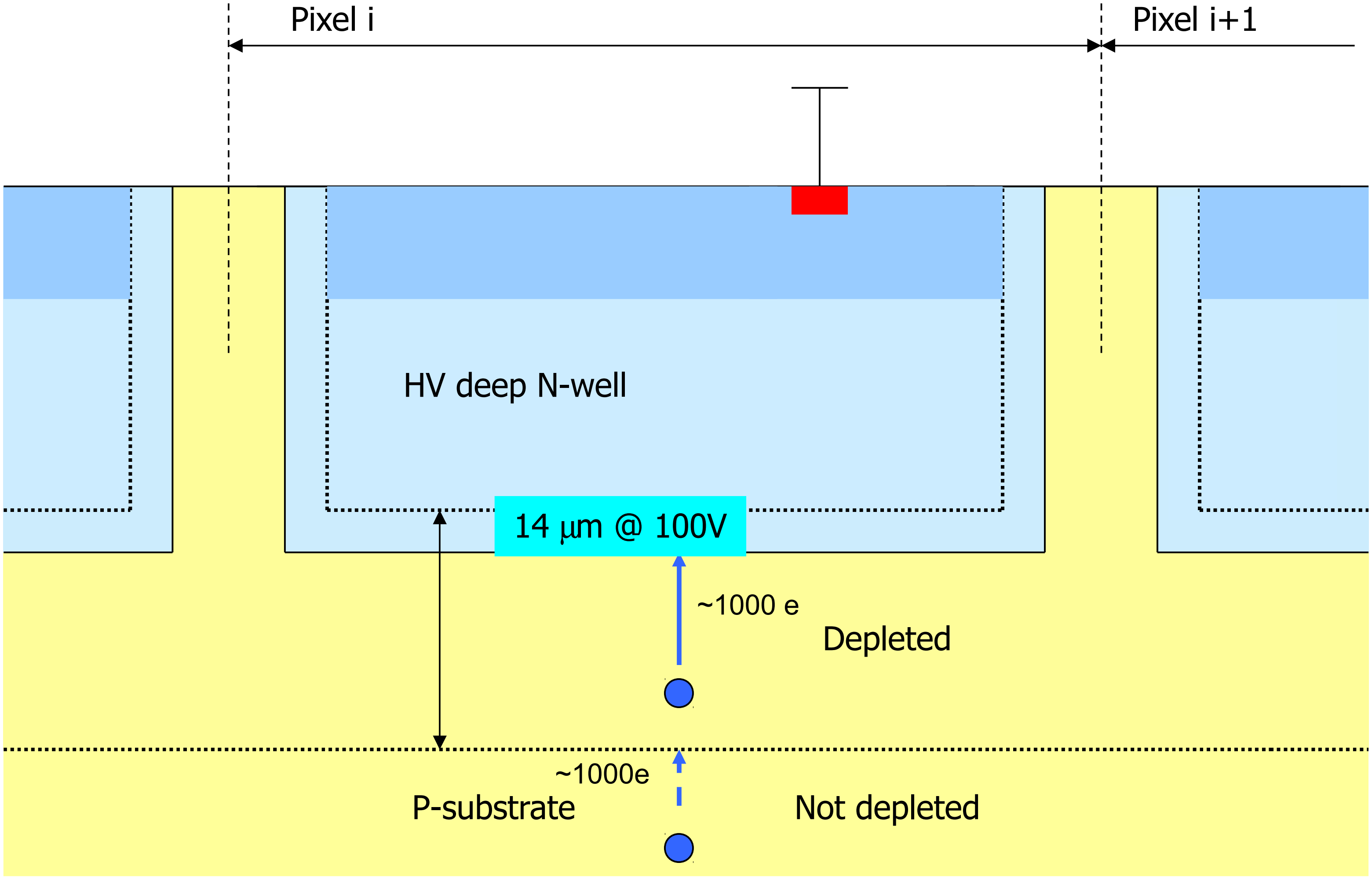
# AMS H18 HV-CMOS



- Project initiated by Ivan Peric (U Heidelberg)
- Austria Micro Systems offers HV-CMOS processes with 180 nm feature size in cooperation with IBM
  - biasing of substrate to ~60-100V possible
  - substrate resistivity ~20 Ohm*cm → $N_{eff} > 10^{14}/cm^3$
    - radiation induced $N_{eff}$ insignificant even for innermost layers
  - depletion depth in the order of 10-20 µm → signal ~1-2 $ke^-$
  - on-sensor amplification possible - and necessary for good S/N
    - key: small pixel sizes → low capacitance → low noise
  - additional circuits possible, e.g. discriminator
    - beware of 'digital' crosstalk
  - full-sized radiation hard drift-based MAPS feasible, but challenging
    - aim for 'active sensors' in conjunction with rad-hard readout electronics first

# A HV-CMOS sensor...

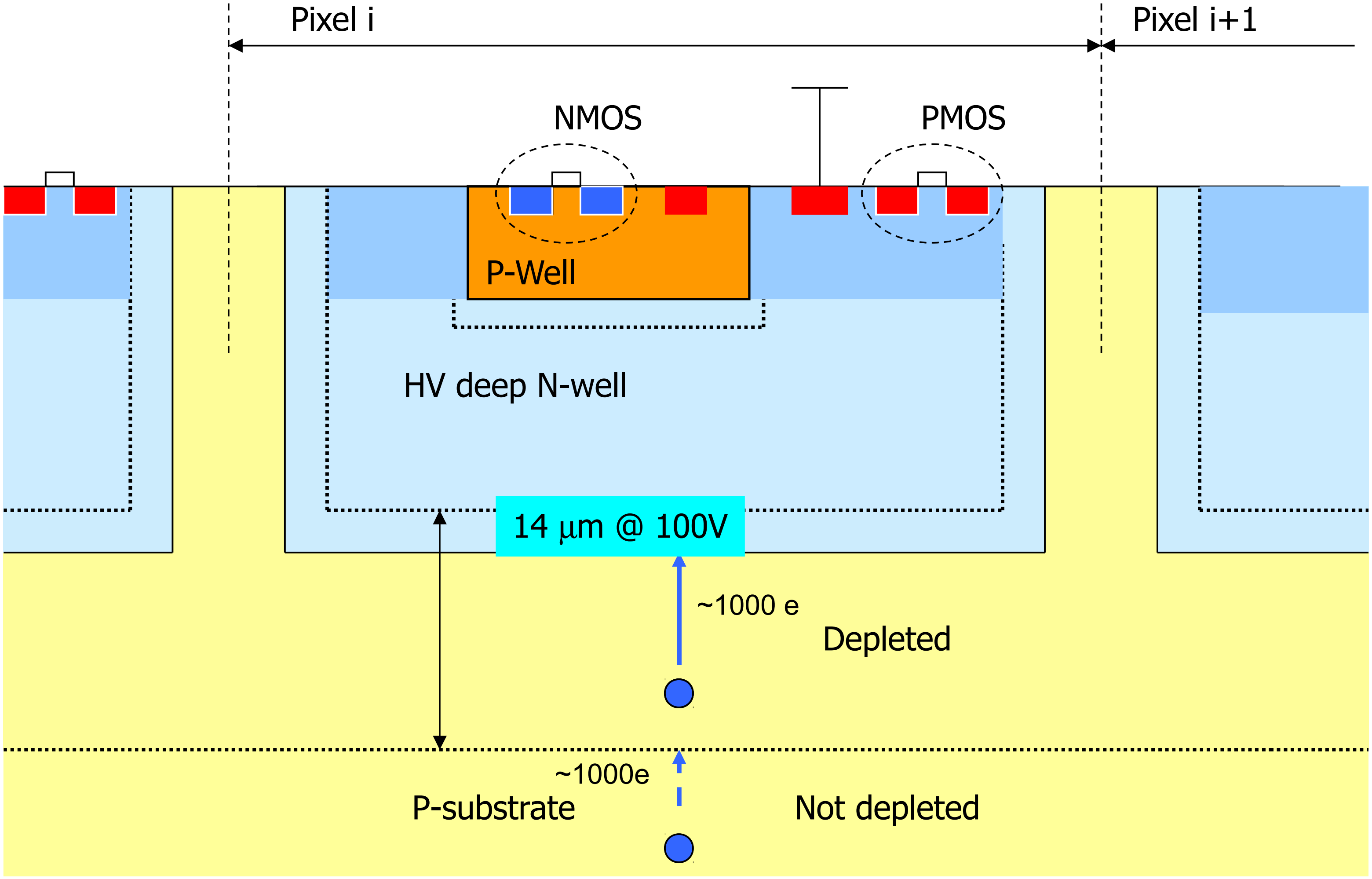
- essentially a standard n-in-p sensor
- depletion zone 10-20 µm: signal in the order of 1-2ke$^-$
  - challenging for hybrid pixel readout electronics
    - new ATLAS ROC FE-I4 might be able to reach this region – but no margin



The depleted high-voltage diode used as sensor (n-well in p-substrate diode)

# ...including active circuits: *smart diode array (SDA)*

- implementation of
  - first amplifier stages
  - additional cuircuits: discriminators, impedance converters, logic, …
- deep sub-micron technology intrinsically rad-hard

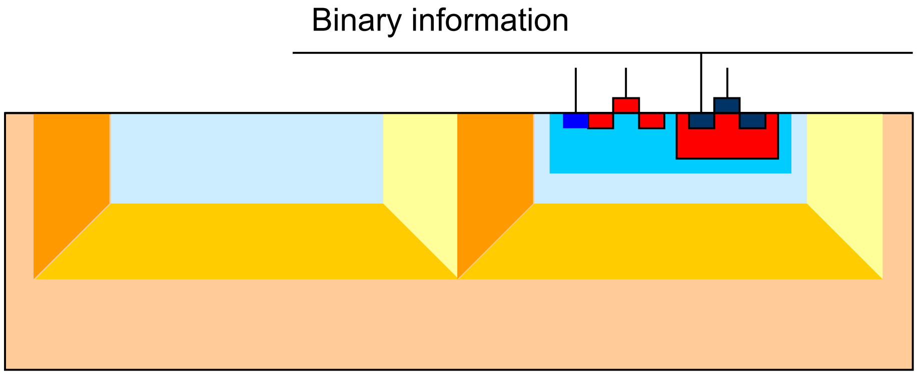


CMOS electronics placed inside the diode (inside the n-well)

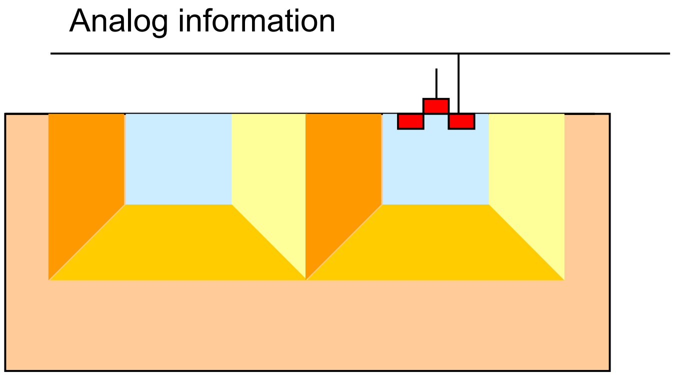
# Prototypes

- Several test-chips already existing, see backup slides for more detailed results

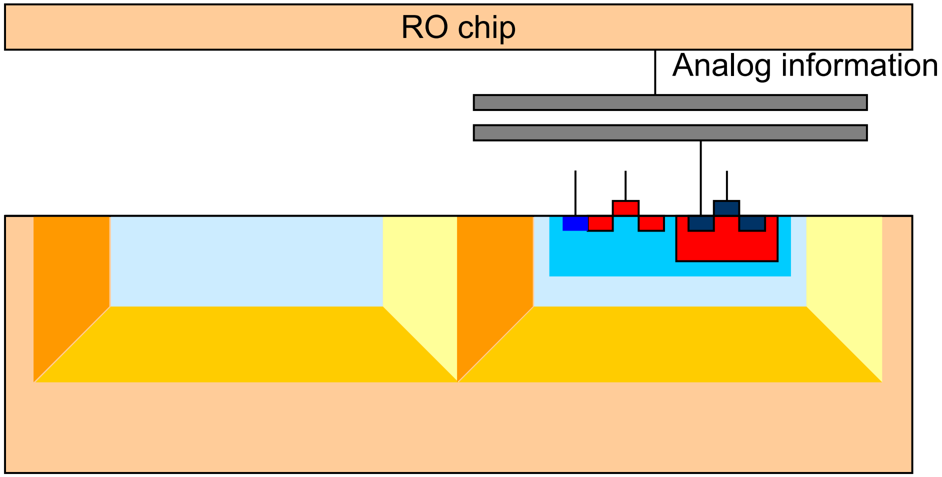
SDA with sparse readout
(“intelligent” CMOS pixels)
HV2/MuPixel chip



SDA with frame readout
(simple PMOS pixels)
HVM chip



SDA with capacitive readout
(“intelligent” pixels)
Capacitive coupled pixel detectors
CCPD1 and CCPD2 detectors

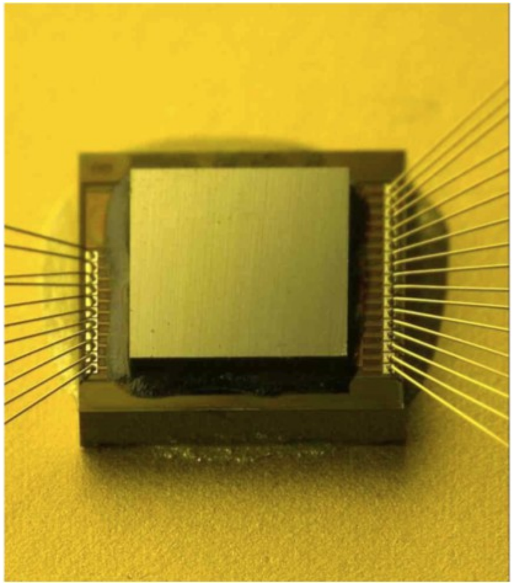


# Prototype summaries

First chip – CMOS pixels
Hit detection in pixels
Binary RO
Pixel size 55x55µm
Noise: 60e
MIP seed pixel signal 1800 e
Time resolution 200ns

Bumpless hybrid detecto

CCPD1 Chip
Bumpless hybrid detector
Based on capacitive chip to chip signal transfer
Pixel size 78x60µm
RO type: capacitive
Noise: 80e
MIP signal 1800e



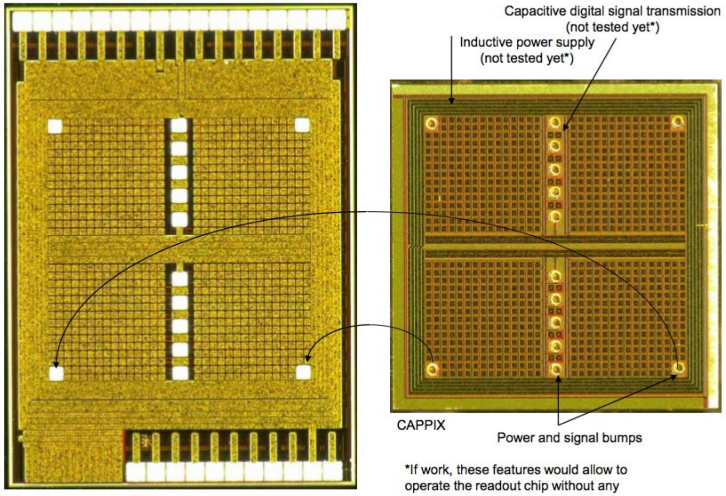
**CCPD2 Chip**
Edgeless CCPD
Pixel size 50x50µm
Noise: 30-40e
Time resolution 300ns
**SNR 45-60**

Irradiations of test pixels
**60MRad – SNR 22 at 10C (CCPD1)**
**$10^{15} n_{eq}/cm^2$ – SNR 50 at 10C (CCPD2)**

Frame readout - monolithic

PM1 Chip
Pixel size 21x21µm
Frame mode readout
4 PMOS pixel electronics
128 on chip ADCs
Noise: 90e
Test-beam: MIP signal 2200e/1300e
Efficiency > 85% (timing problem)
Spatial resolution 7µm
Uniform detection

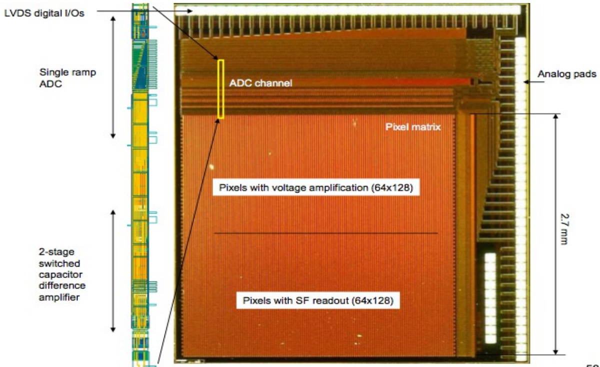
PM2 Chip
Noise: 21e (lab) - 44e (test beam)
**Test beam: Detection efficiency 98%**
**Seed Pixel SNR ~ 27**
**Cluster Signal/Seed Pixel Noise ~ 47**
**Spatial resolution ~ 3.8 µm**



*If work, these features would allow to operate the readout chip without any mechanical contact

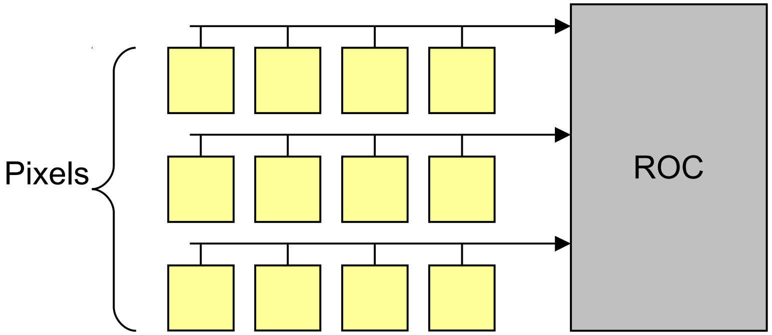
Peric, ATLAS Upgrade Week, November 2011, CAPSENSE

I. Peric



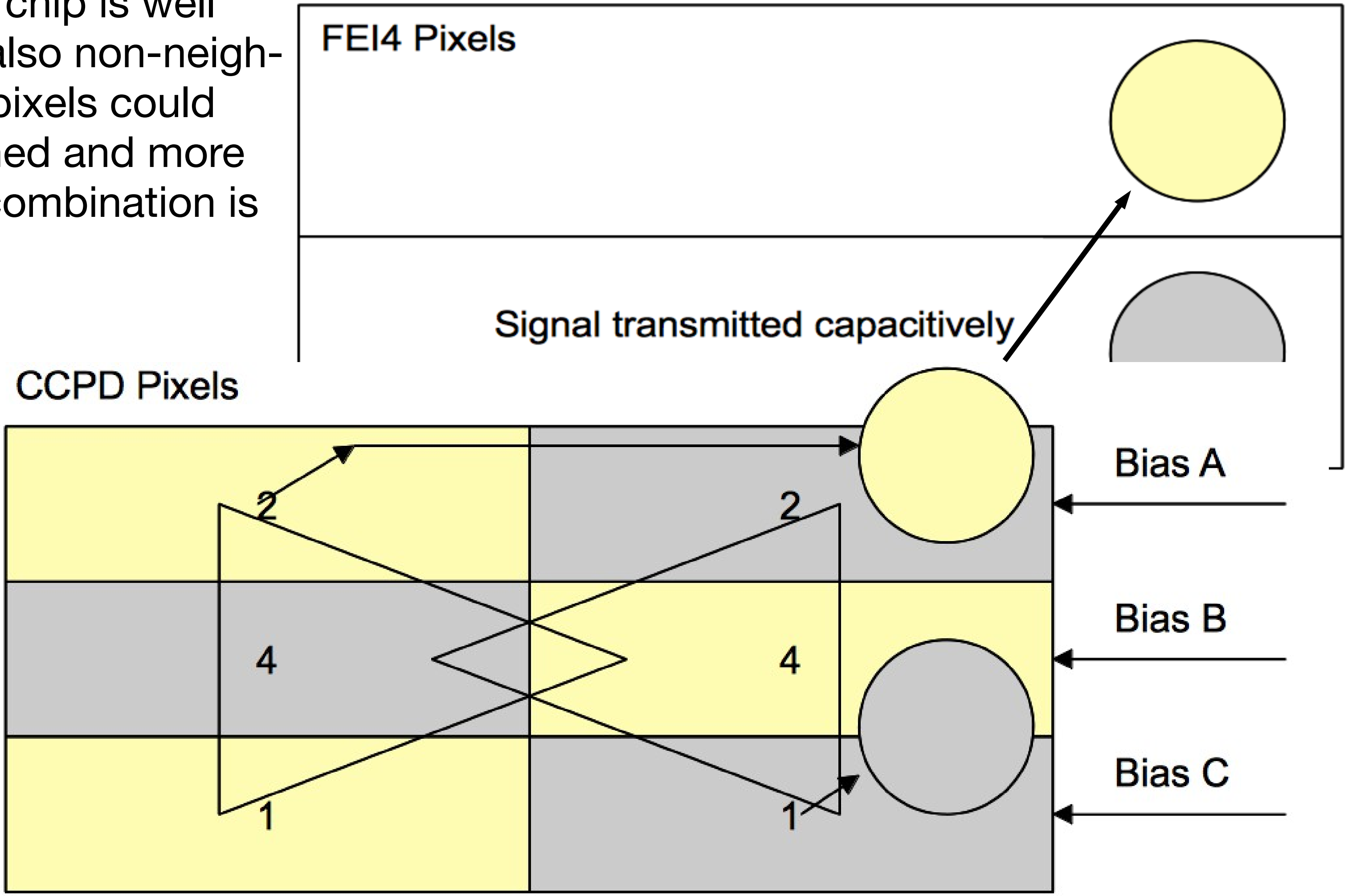
# From MAPS to active sensors

- Existing prototypes would not suitable for HL-LHC, mainly because
  - readout too slow
  - time resolution not compatible with 40 MHz operation
  - high-speed digital circuits might affect noise performance
- Idea: use HV-CMOS as sensor in combination with existing readout technology
  - fully transparent, can be easily compared to other sensors
  - can be combined with several readout chips
  - makes use of highly optimised readout circuits
  - can be seen as first step towards a sensor being integrated into a 3D-stacked readout chip (not only analogue circuits but also charge collection)
- Basic building blocks: *small* pixels (low capacitance, low noise)
  - can be connected in any conceivable way to match existing readout granularity, e.g.
    - (larger) pixels
    - strips



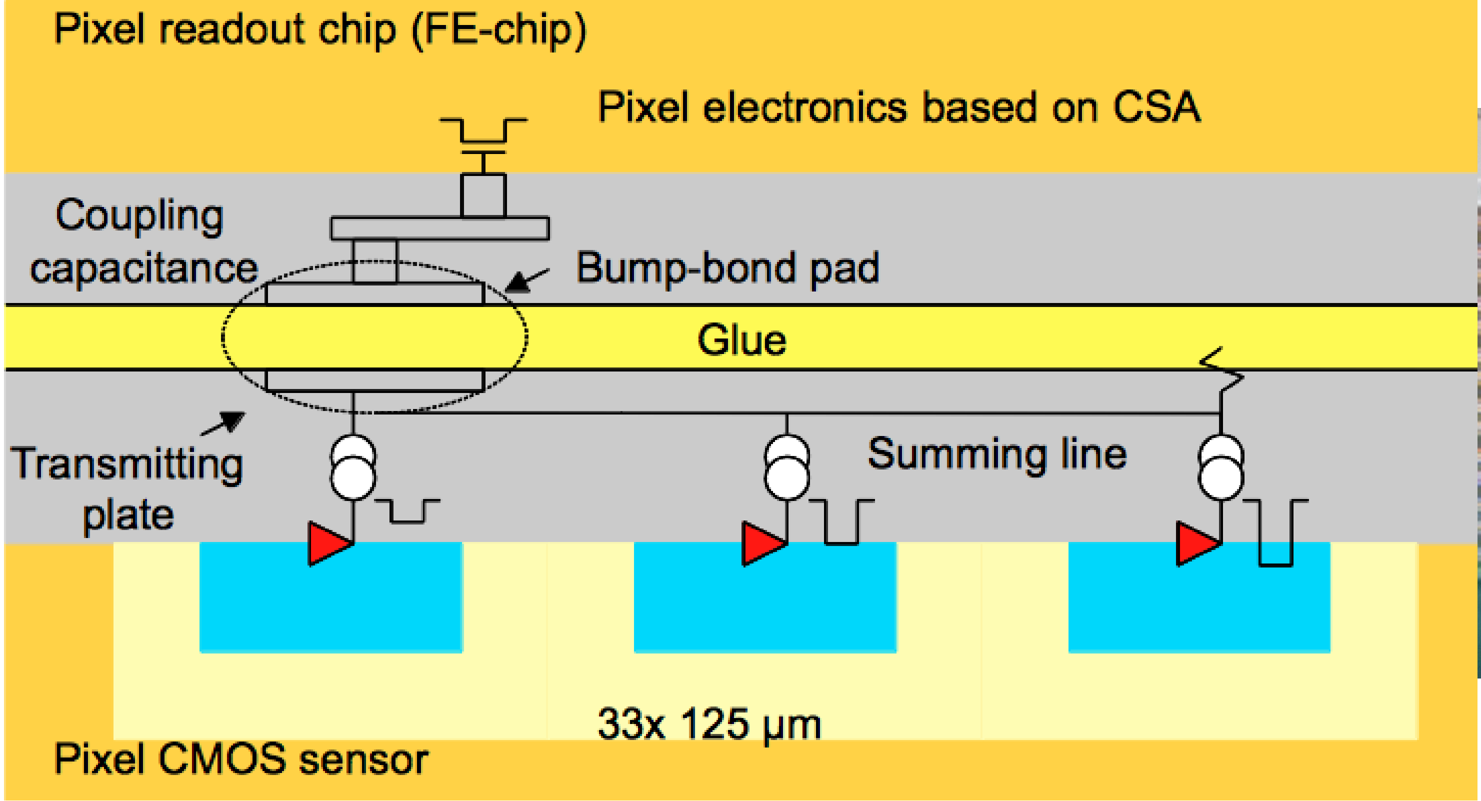
# Pixels: sizes and combinations

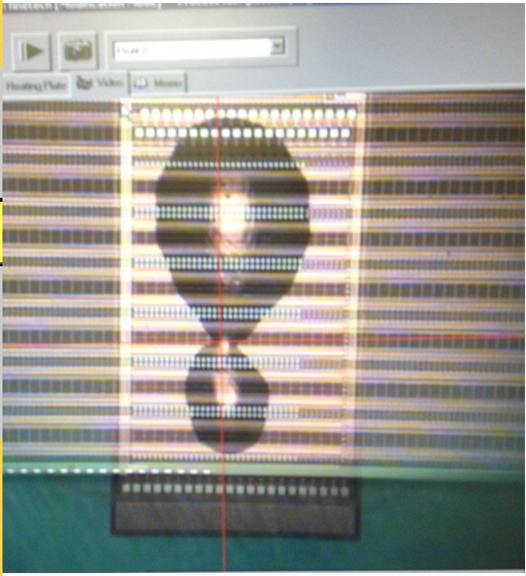
- Possible/sensible pixel sizes: 20x20 to 50x125 µm
    - 50x250 µm (current ATLAS FE-I4 chip) too large
    - combine several sensor “sub-pixels” to one ROC-pixel
        - sub-Pixels encode their address/position into the signal as pulse-height-information instead of signal proportional to collected charge
        - routing on chip is well possible, also non-neighbour sub-pixels could be combined and more than one combination is possible



# Pixels: bonding?

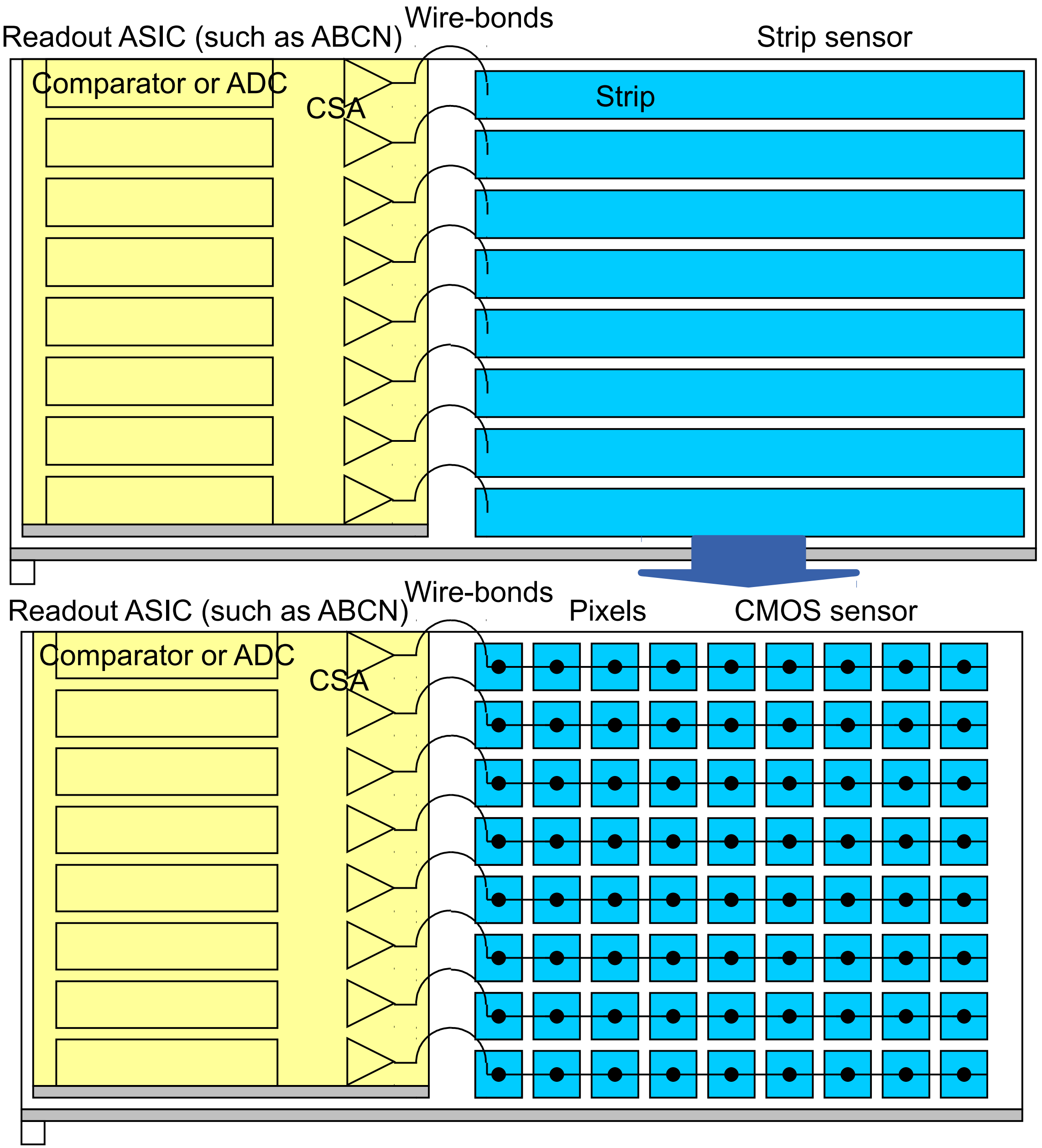
- Only reason not to use AC coupling with pixel sensors up to now was small coupling capacitance in association with low signal
  - amplification possible, hence AC transmission not a problem at all
  - allows to get rid of costly bump-bonding
  - layer thicknesses below 5 µm have been reached with industry standard flip-chipping machines and rad-hard liquid epoxy glues
  - variations in glue thickness are handled by tuning procedures and offline corrections if necessary

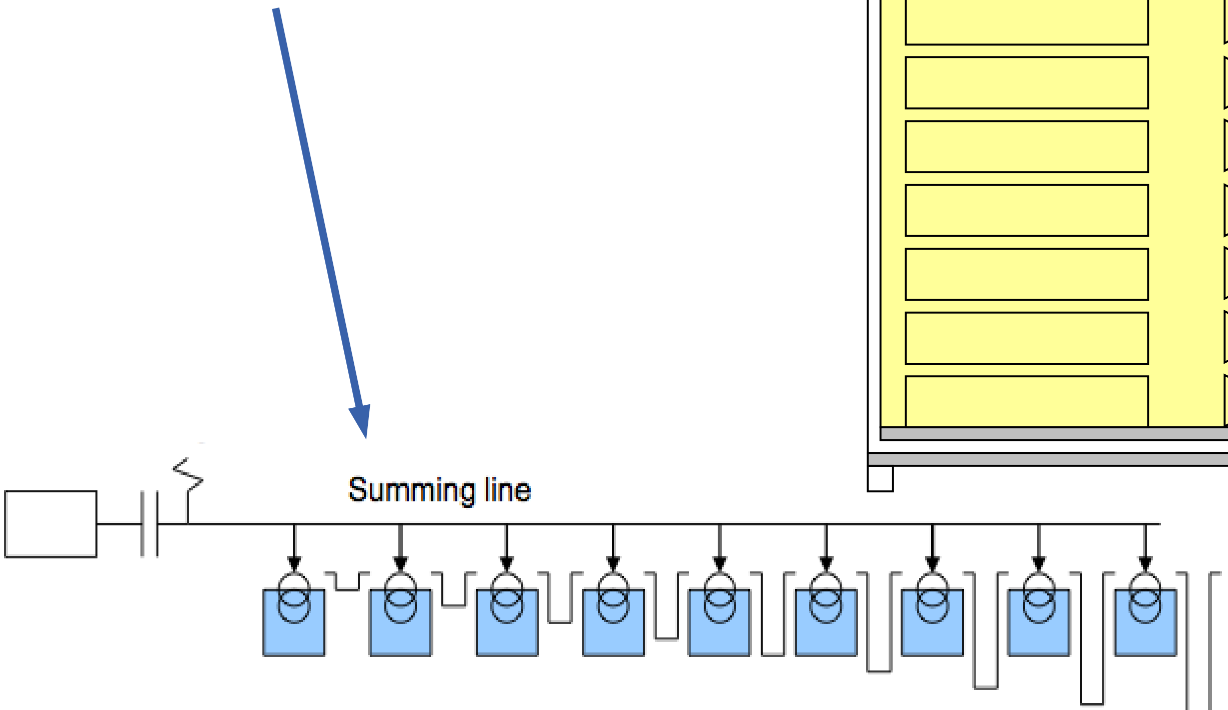




# Strips

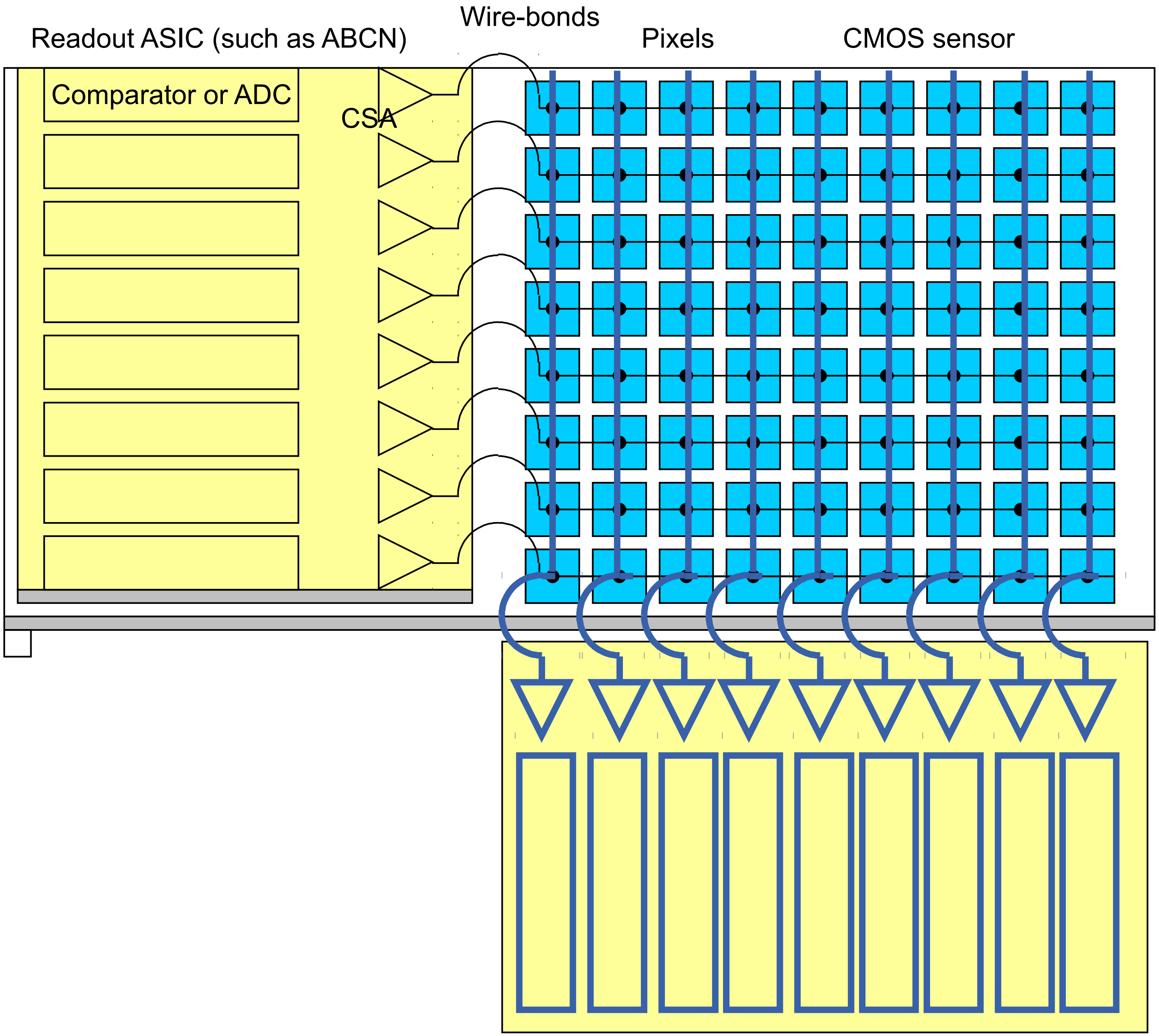
- Easiest idea would be to simply sum all pixels within a virtual strip
- Hit position along the strip can be again encoded by pulse height for analogue readout chips (e.g. Beetle)





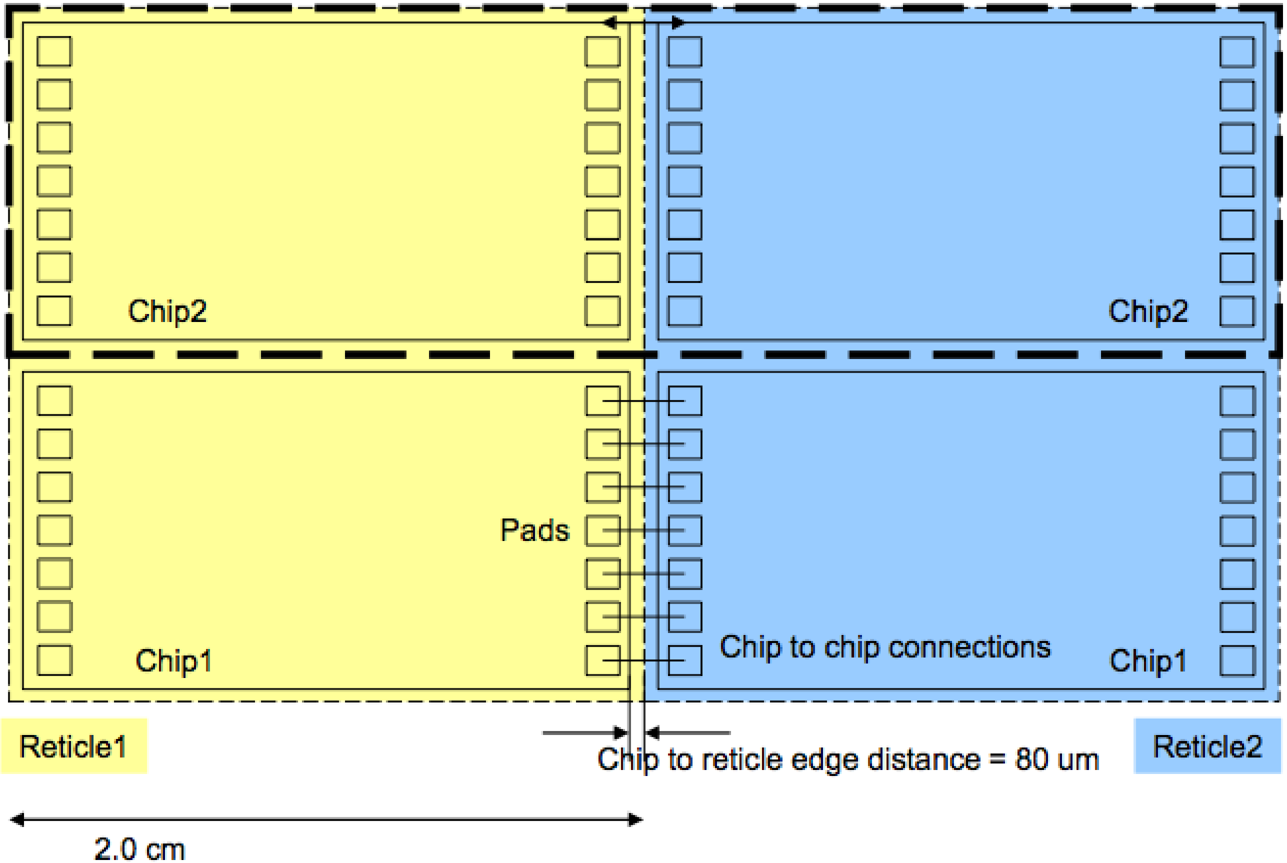
# Strips

- Signals are digital so multiple connections are possible, e.g.
  - “crossed strips”
  - strips with double length but only half the pitch in r-phi



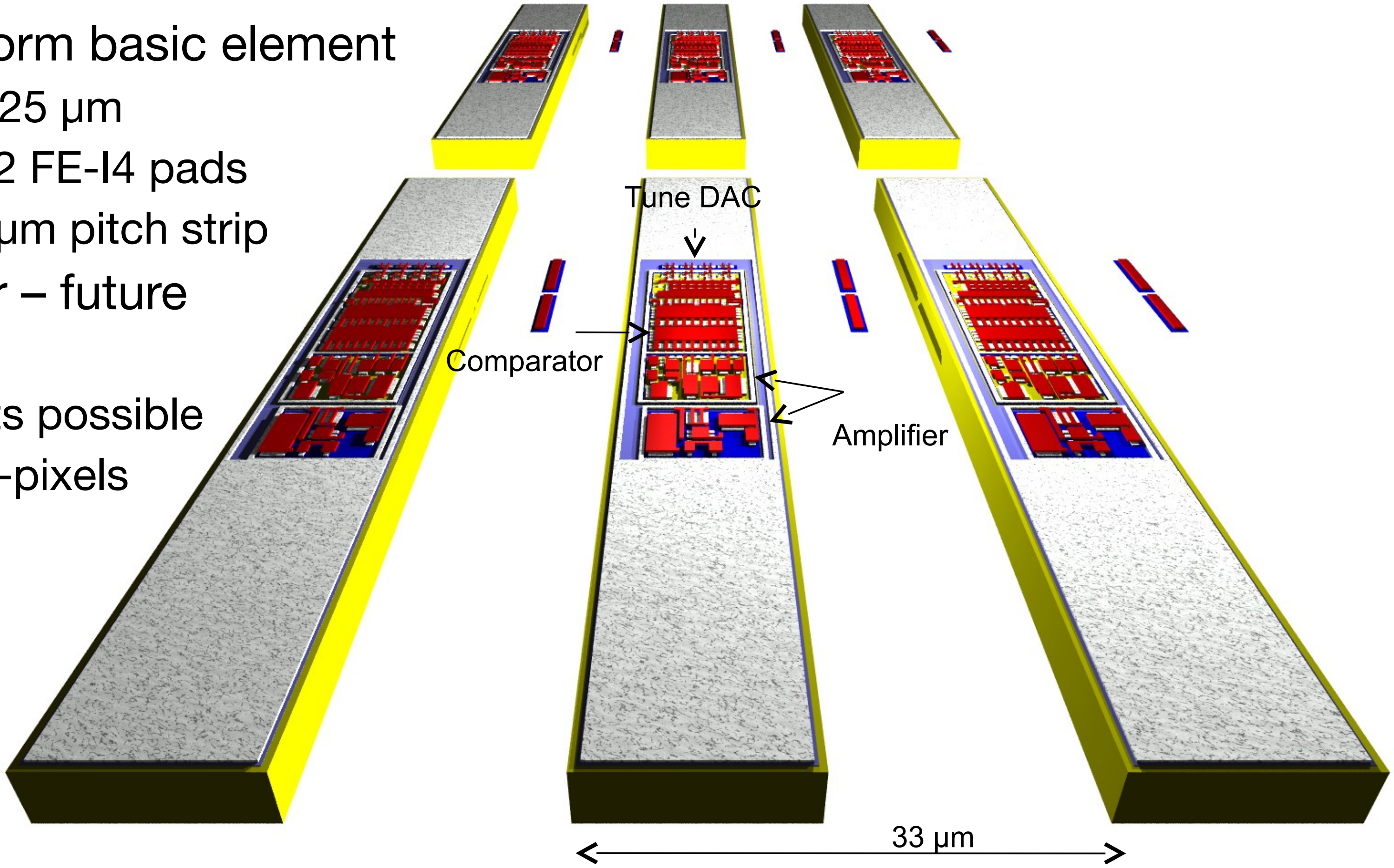
# Reticule size/stitching

- Sensor size is currently limited by reticule size of ~2x2 cm
  - however, the yield should be excellent (very simple circuit, essentially no "central" parts) so it might be interesting to cut large arrays of sensors from a wafer and connect individual reticules by
    - wire-bonding
    - post-processing (one metal layer, large feature size)
- There are HV-CMOS processes/foundries which allow for stitching
- Very slim dicing streets
  - Gaps between 1-chip modules could be rather narrow



# HV2FEI4

- A combined active strip/pixel sensor was designed and produced
  - strips compatible with ATLAS ABCN and LHCb/Alibava Beetle
  - pixels match new ATLAS FE-I4 readout chip
    - capacitive coupling
    - bump-bonding possible
- Structure
  - 6 sub-pixels form basic element
    - each 33 x 125 μm
    - connect to 2 FE-I4 pads
    - form a 100 μm pitch strip
  - small fill factor – future options:
    - more circuits possible
    - smaller sub-pixels

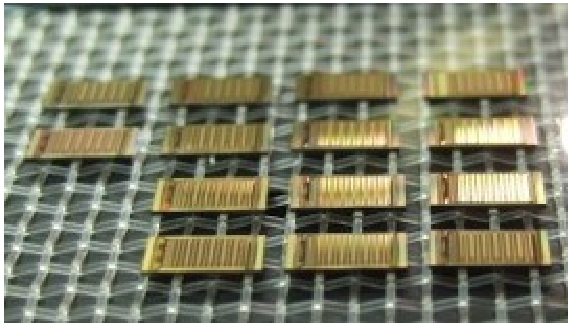


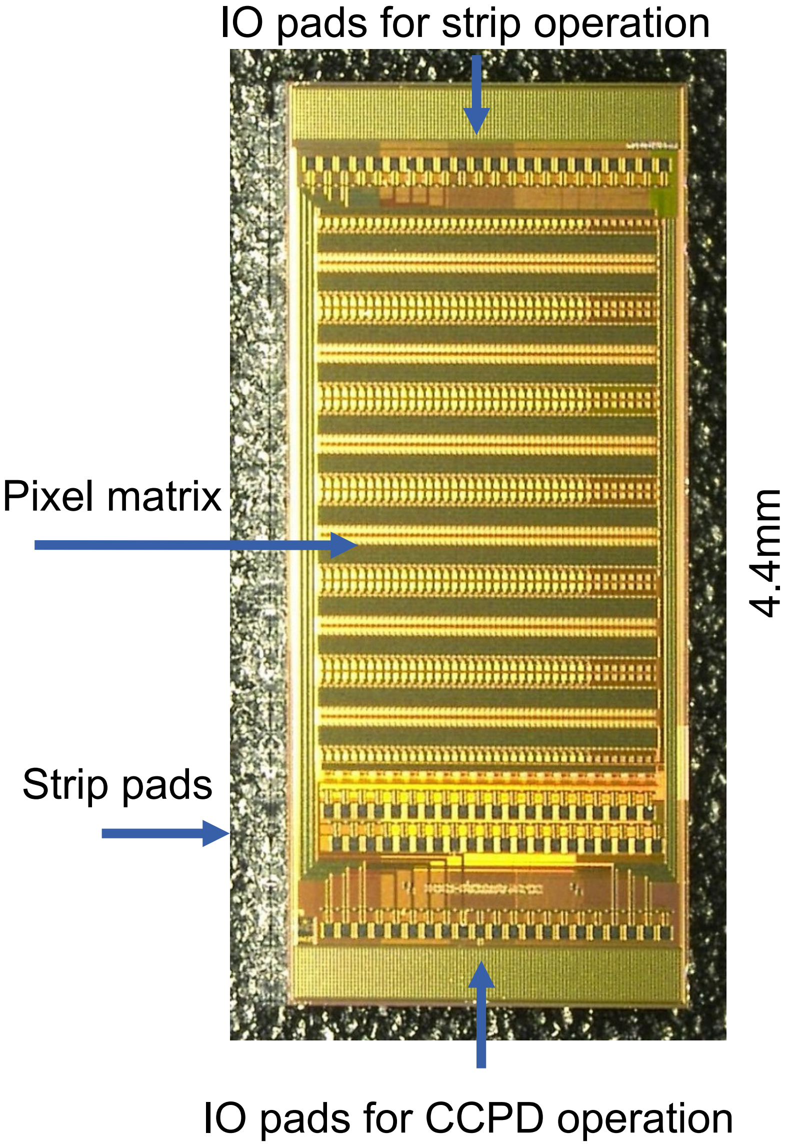
# HV2FEI4

- Chip size: 2.2mm x 4.4mm
- Pixel matrix: 60x24 (sub-)pixels of 33 μm x 125 μm
- 21 IO pads at the lower side for CCPD operation
- 40 strip-readout pads (100 μm pitch) at the lower side and 22 IO pads at the upper side for (virtual) strip operation
- On chip bias DACs
- Pixels contain charge sensitive amplifier, comparator and tune DAC
- Configuration via FPGA or μC: 4 CMOS lines (1.8V)

3 possible operation modes

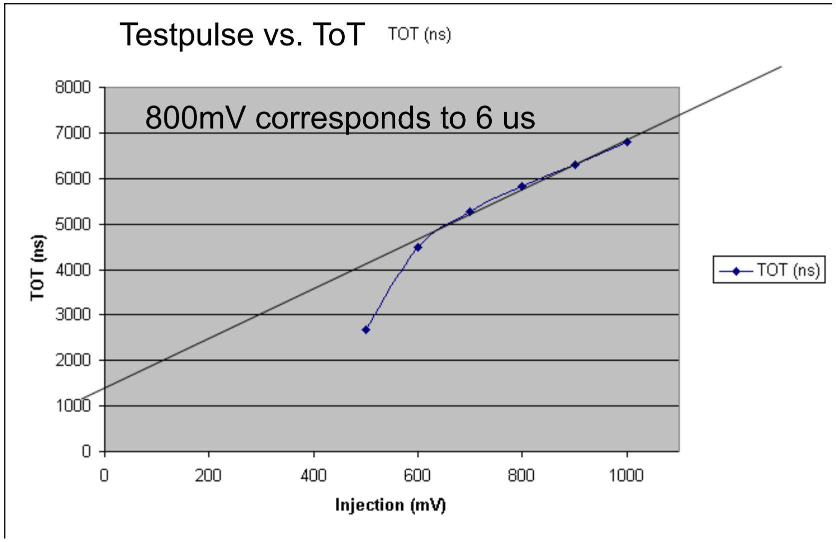
- standalone on test PCB
- strip-like operation
- pixel (FE-I4) readout



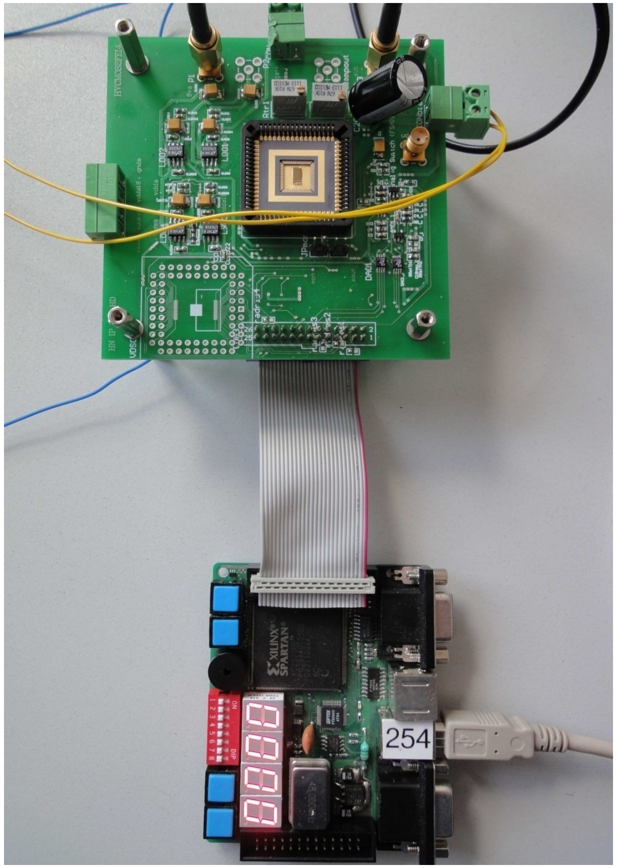


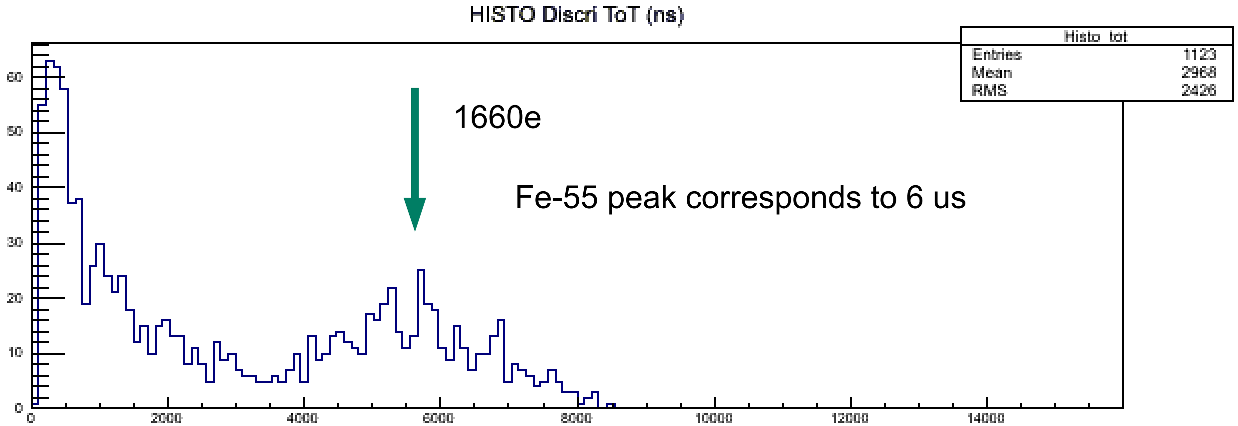
# HV2FEI4: characterisation

- standalone, by I. Peric (Mannheim)
- MPW for $^{90}$Sr at ~1900 $e^-$
    - would mean more than 20µm active depth?
    - corresponds to 900mV injection



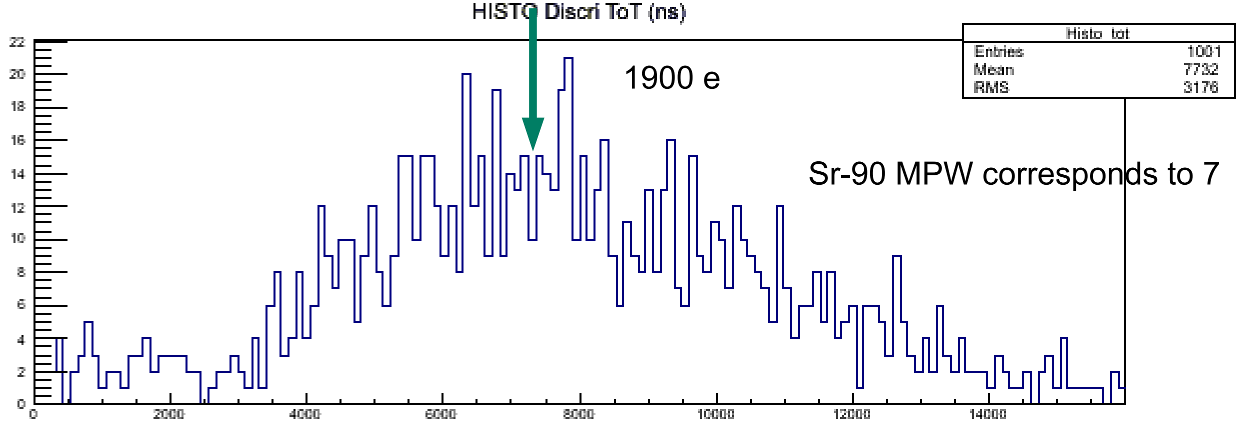
800mV corresponds to 6 us





1660e

Fe-55 peak corresponds to 6 us



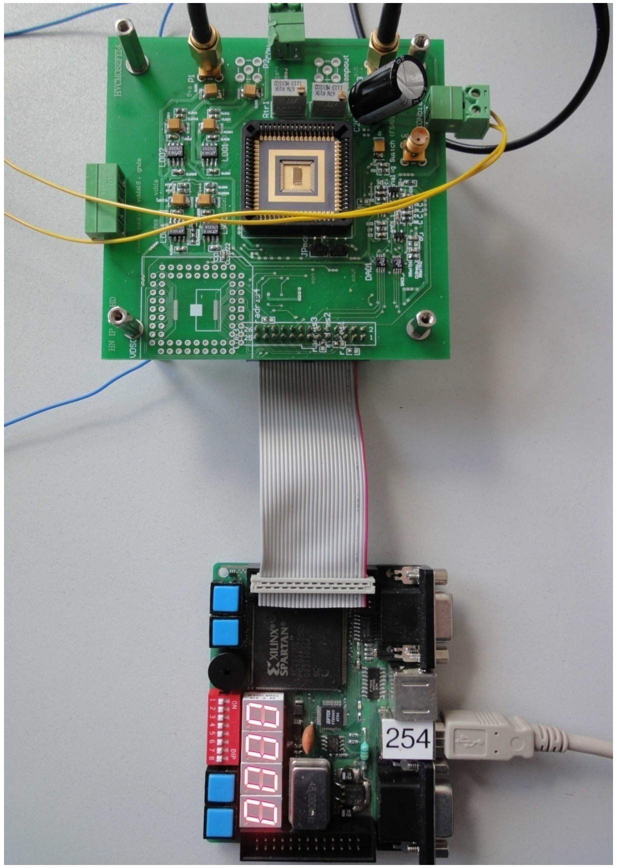
1900 e

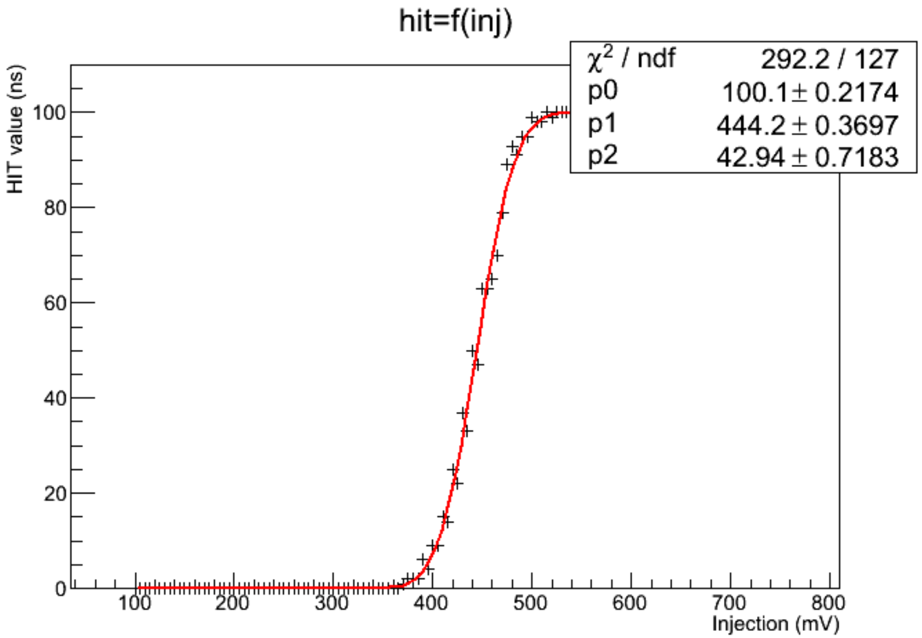
Sr-90 MPW corresponds to 7 us

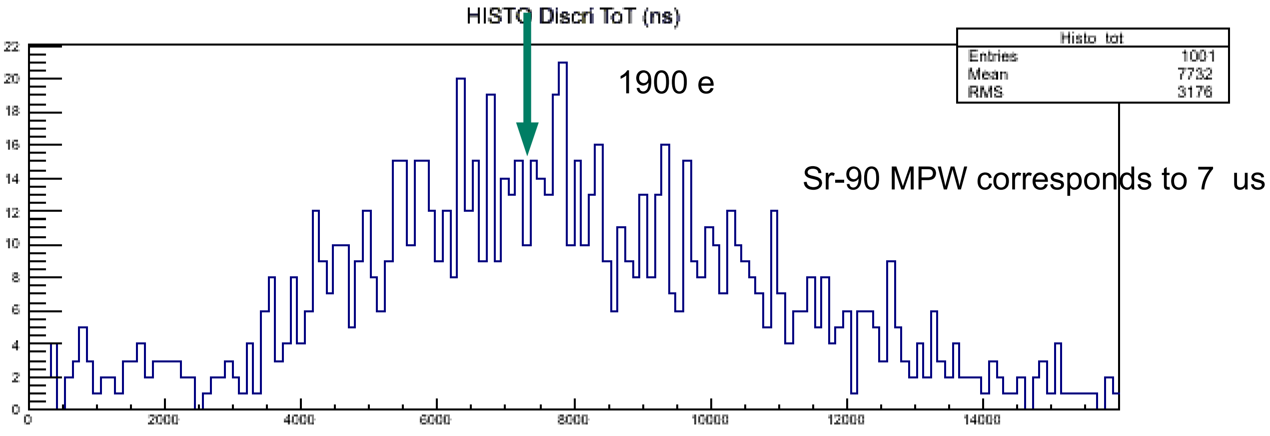
Sr-90 MPW corresponds to ~ 900mV injection amplitude

# HV2FEI4: characterisation

- standalone, by I. Peric (Mannheim)
- MPW for $^{90}$Sr at ~1900 $e^-$
  - would mean more than 20µm active depth?
  - corresponds to 900mV injection
- Noise: ~30-40mV → SNR: 900/40 = 22







1900 e

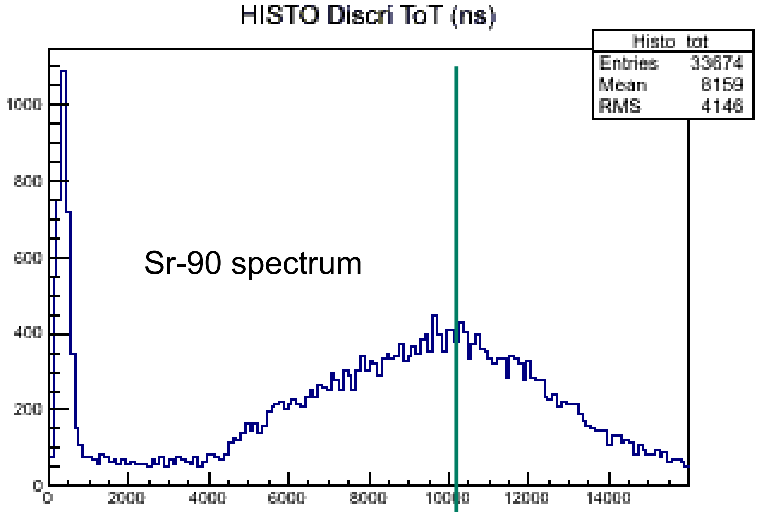
Sr-90 MPW corresponds to 7 us

Sr-90 MPW corresponds to ~ 900mV injection amplitude

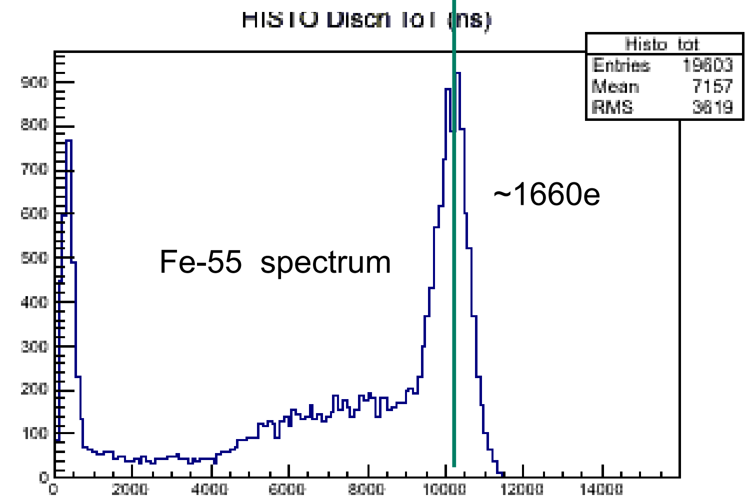
# HV2FEI4: irradiation

- First irradiations conducted at CERN/PS and with an x-ray tube
  - on special PCB allowing for remote operation, HV2FEI4 powered and read-out during irradiation

un-irradiated device



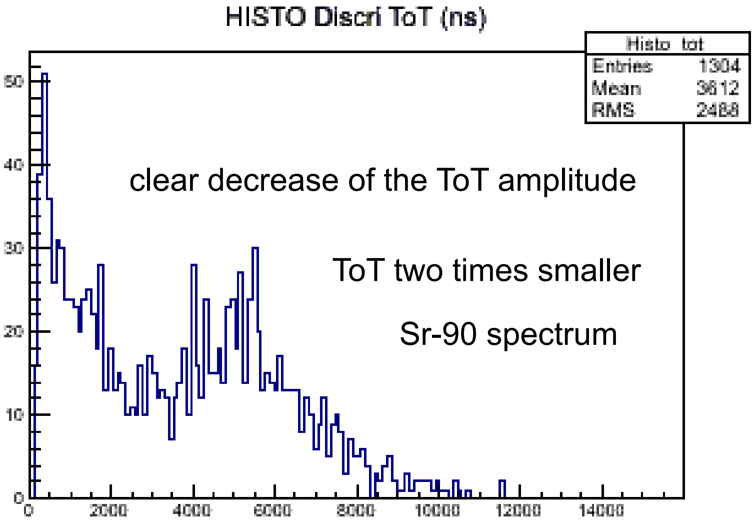
Sr-90 spectrum



Fe-55 spectrum

~1660e

CCPD9 irradiated at 80 MRad



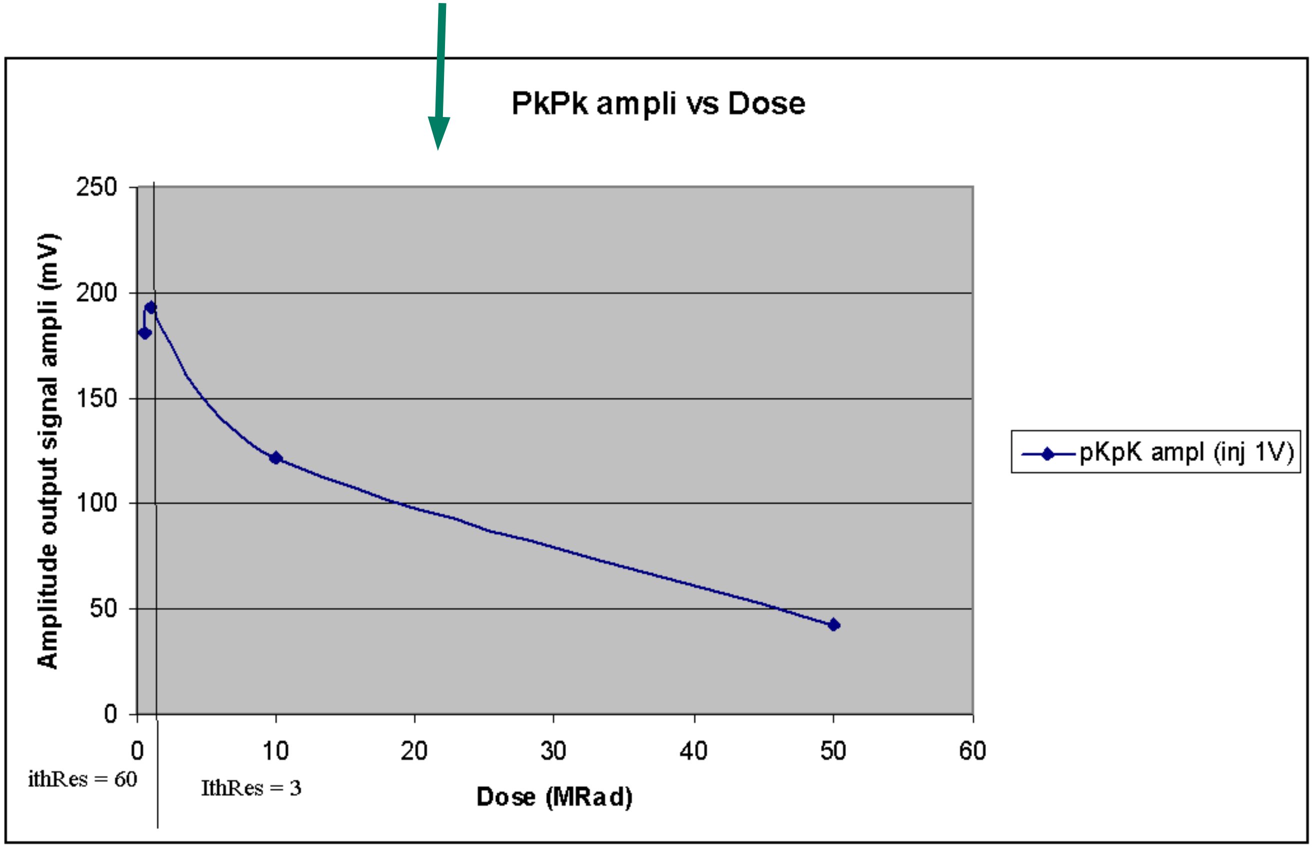
clear decrease of the ToT amplitude

ToT two times smaller

Sr-90 spectrum

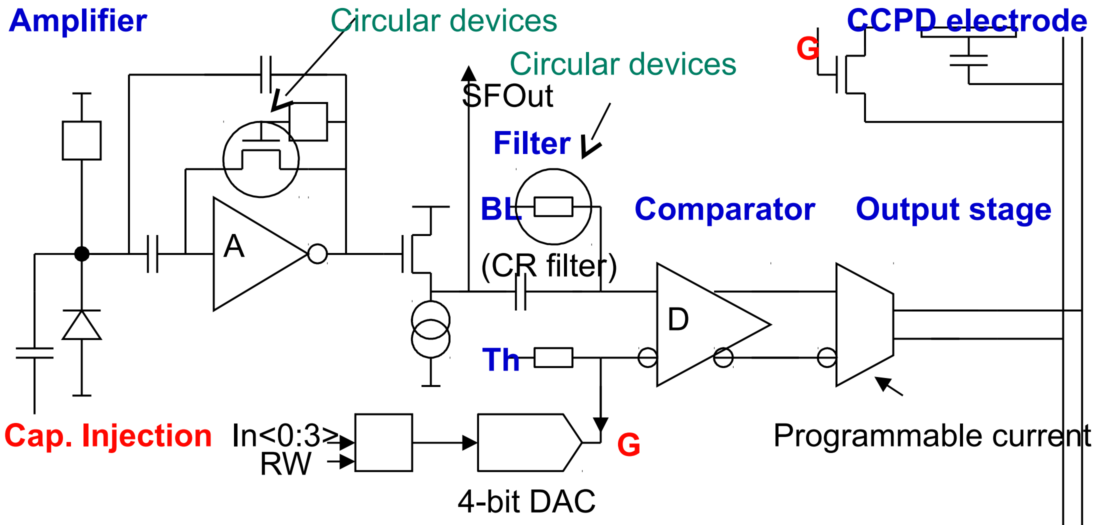
# HV2FEI4: irradiation

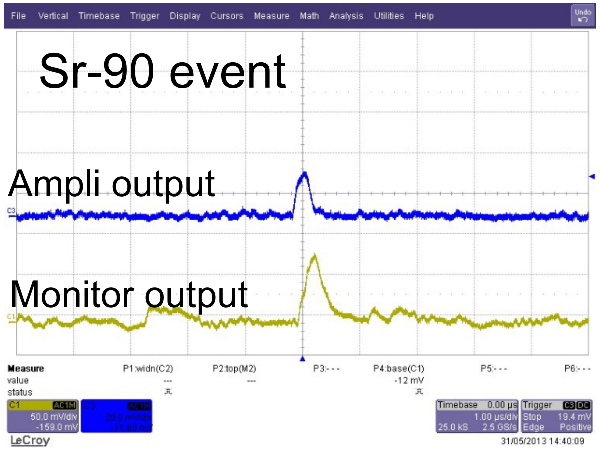
- First irradiations conducted at CERN/PS and with an x-ray tube
  - on special PCB allowing for remote operation, HV2FEI4 powered and read-out during irradiation
- clear radiation effects seen after proton and x-ray irradiation
  - drop in amplitude/amplification
  - also seen with test pulser input → electronics effect, rad-soft design



# Rad-hardness: consequences

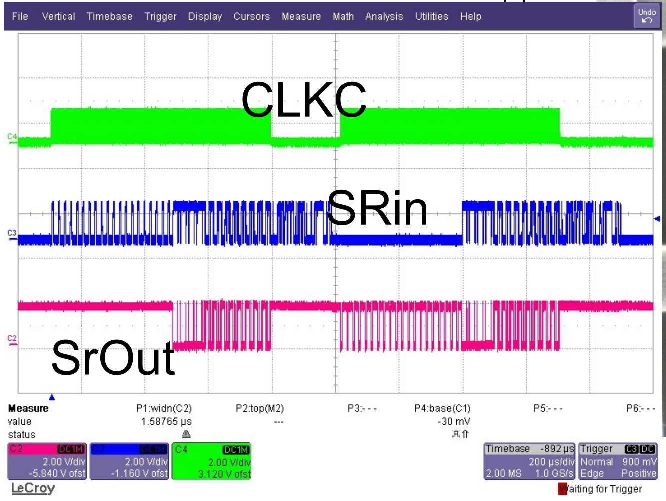
- deliberately chose “standard” design to see how far it would get
    - not far enough… → “harden” design by guard rings, circular transistors, …
- HV2FEI4_v2 was submitted in November and received recently
    - first measurements as expected, irradiation to follow





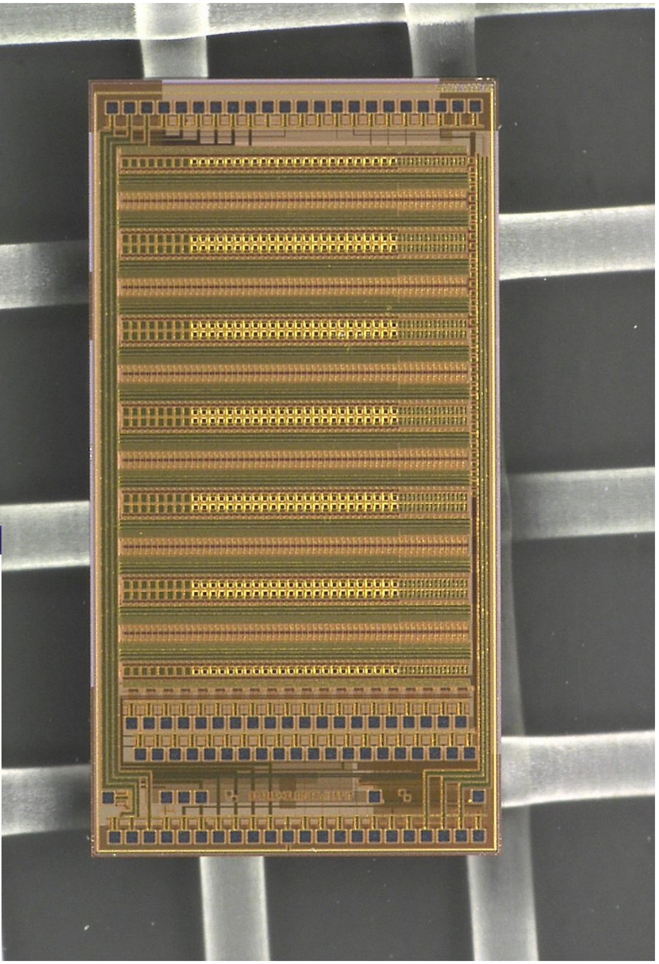
Measure P1:widn(C2) P2:top(M2) P3:--- P4:base(C1) P5:--- P6:---
value -12 mV
status

C1 50.0 mV/div -159.0 mV
Timebase 0.00 µs 1.00 µs/div 25.0 kS 2.5 GS/s
Trigger Stop 19.4 mV Edge Positive
31/05/2013 14:40:09



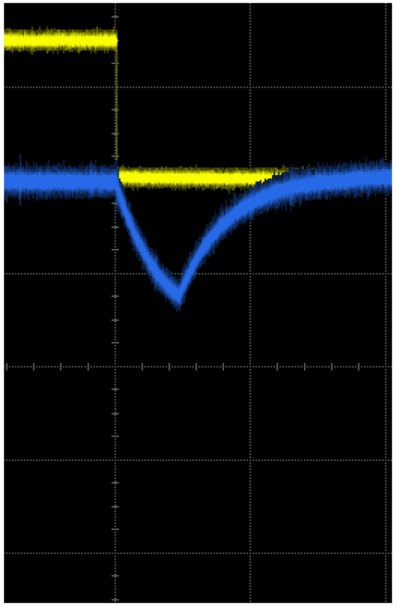
Measure P1:widn(C2) P2:top(M2) P3:--- P4:base(C1) P5:--- P6:---
value 1.58765 µs -30 mV
status

C2 2.00 V/div -5.840 V ofst
C3 2.00 V/div -1.160 V ofst
C4 2.00 V/div 3.120 V ofst
Timebase -892 µs 200 µs/div 2.00 MS 1.0 GS/s
Trigger Normal 900 mV Edge Positive
Waiting for Trigger



# HV2FEI4: strip readout

- ABCN readout being planned
- Beetle readout in place, but issues with noise/common mode pickup
  - also present if HV2FEI4 not powered...
- configuration works, “strips” can be switched on/off
- position-encoding works:
  - monitor output on scope
  - same principle on strip readout pads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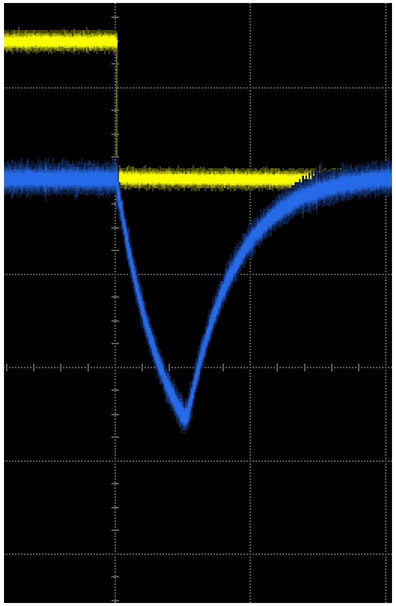
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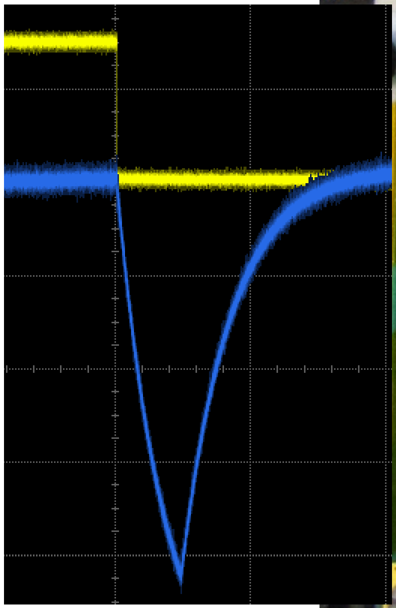
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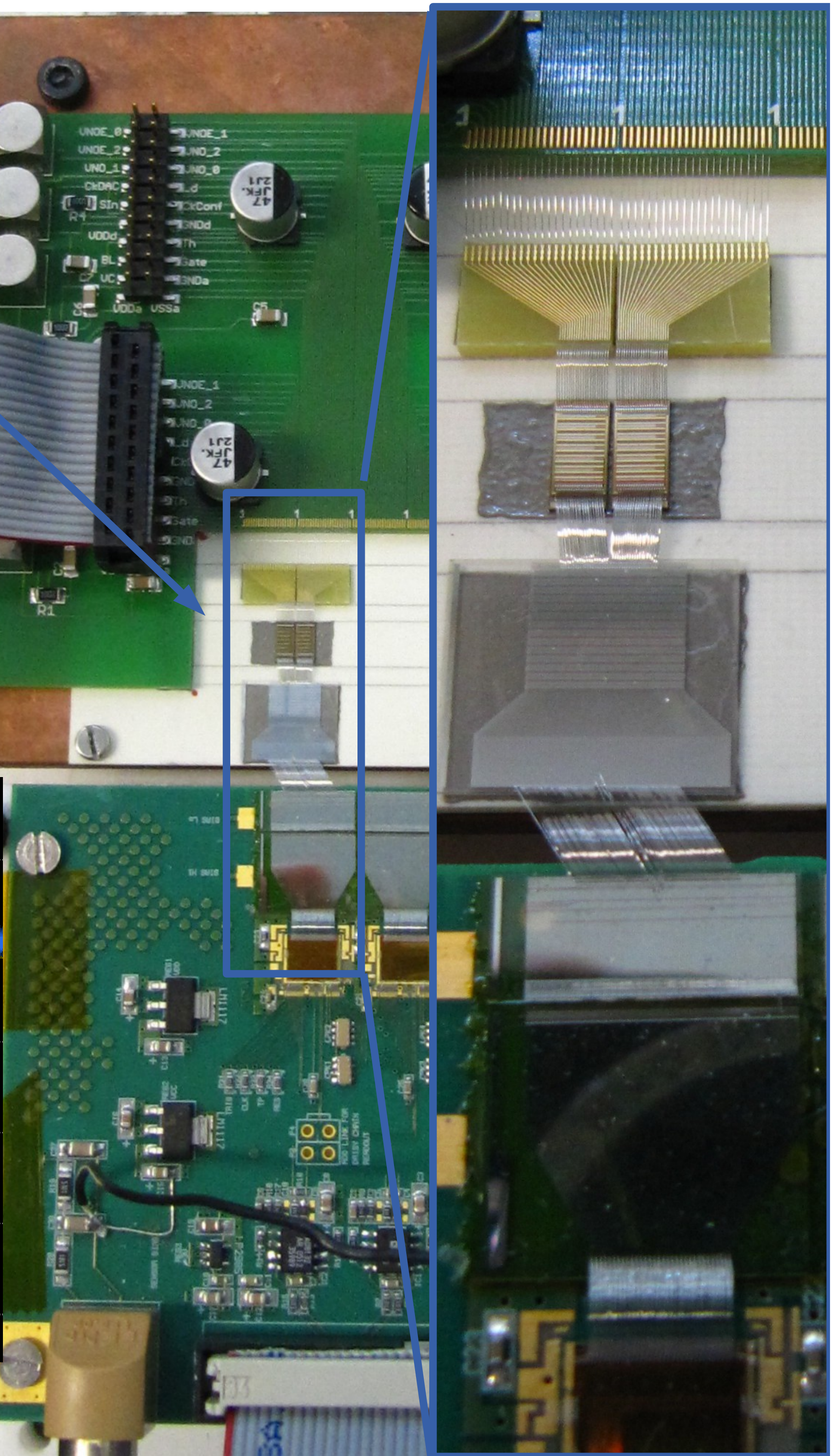
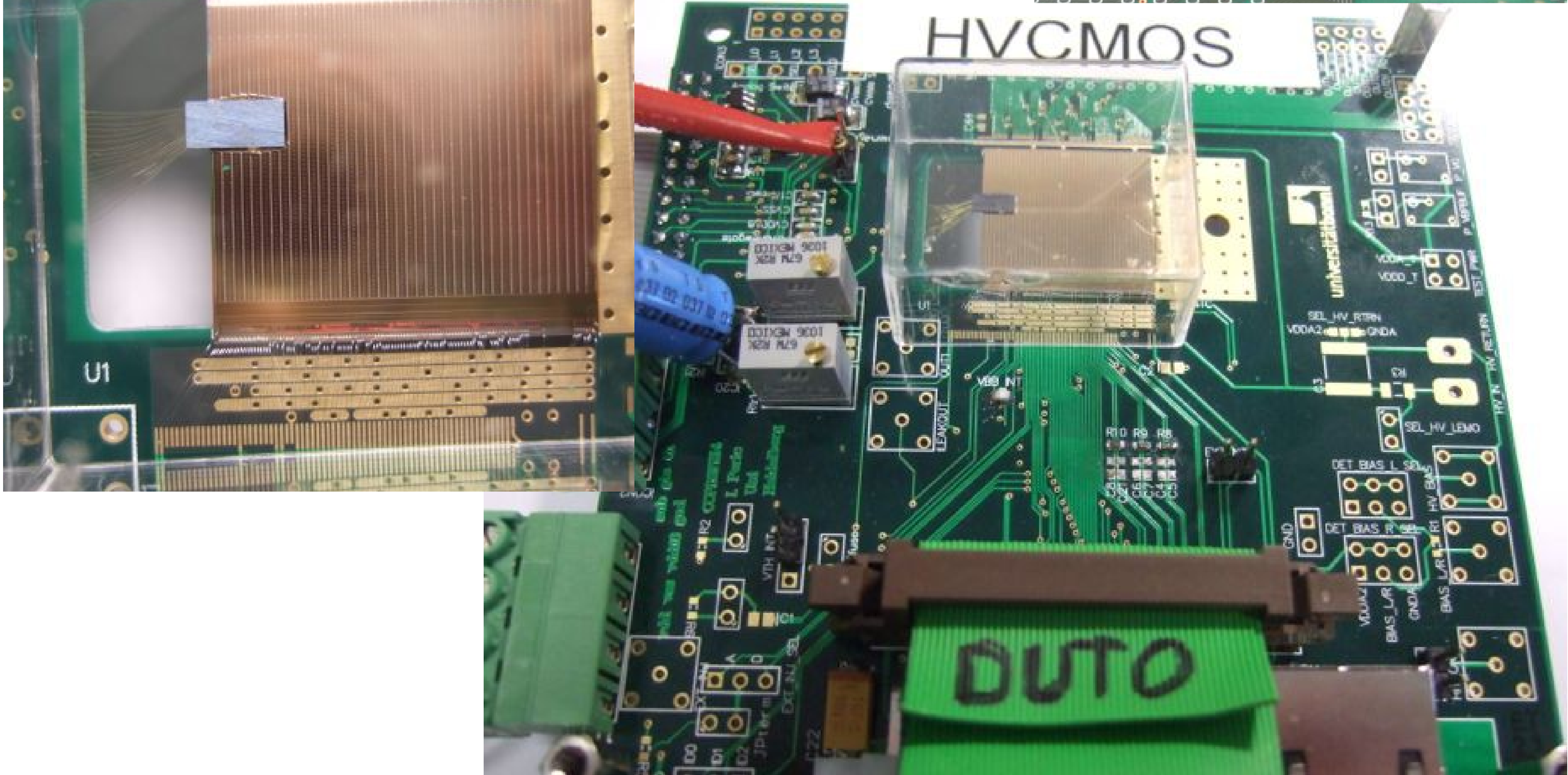


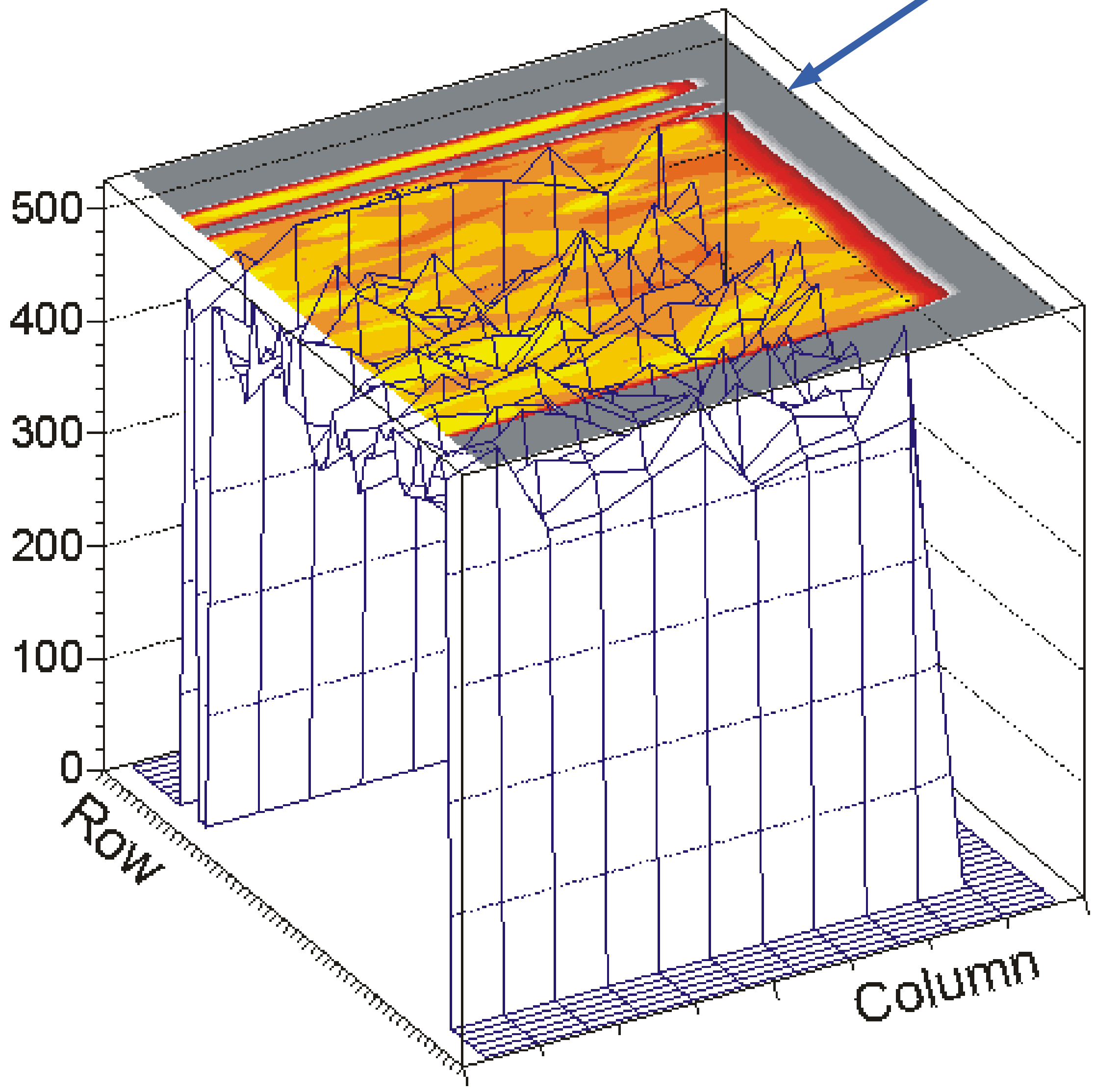
# HV2FEI4: Pixel readout

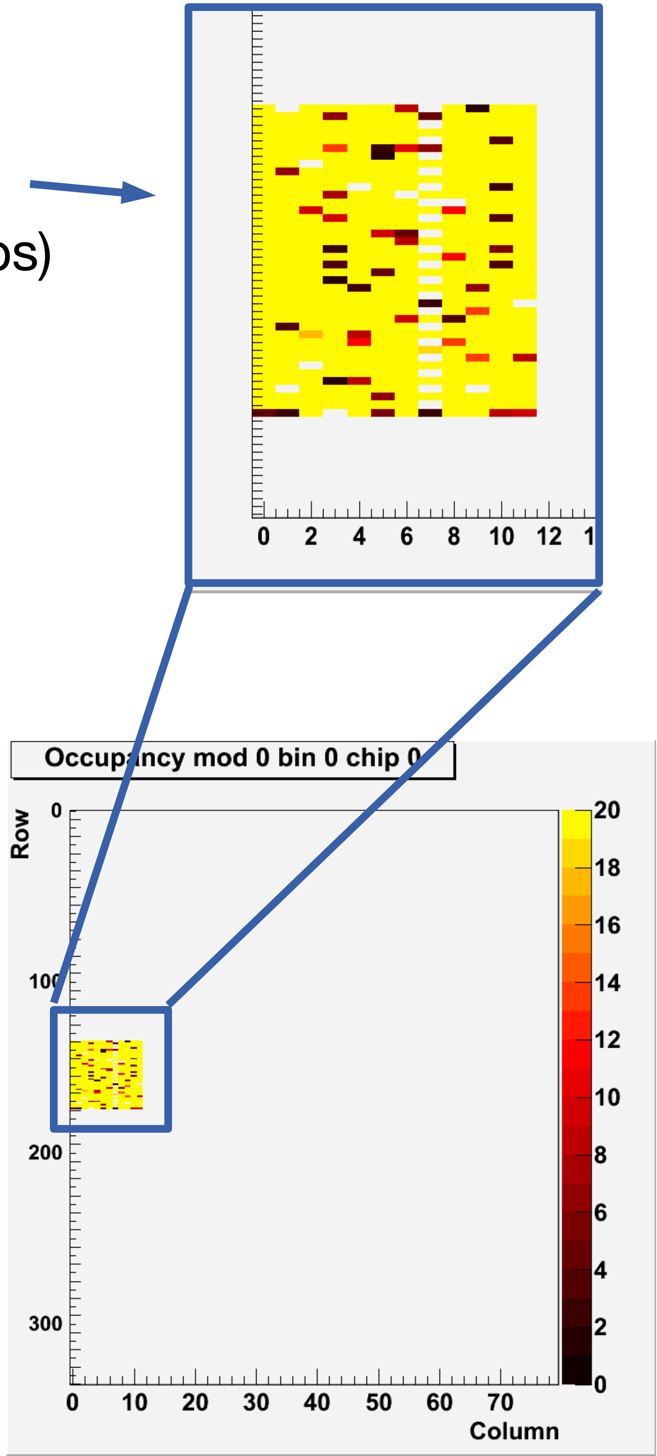
- Several HV2FEI4s glued to FE-I4A and FE-I4B
- HV2FEI4 wirebonds done through hole in PCB
  - could be bumps or TSVs later



# HV2FEI4: Pixel readout

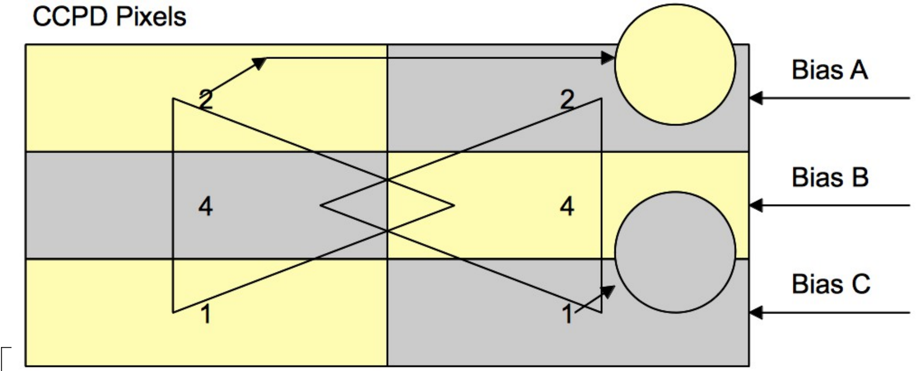
- First measurements:
  - FE-I4A (w/ bumps) sees HV2FEI4 being glued to it
  - Physics ($^{22}$Na source) is seen by FE-I4B (w/o bumps)

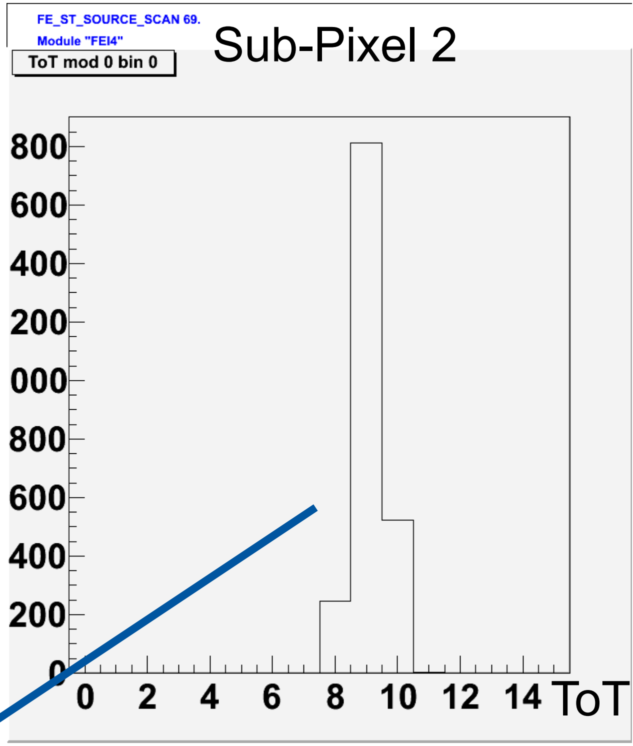


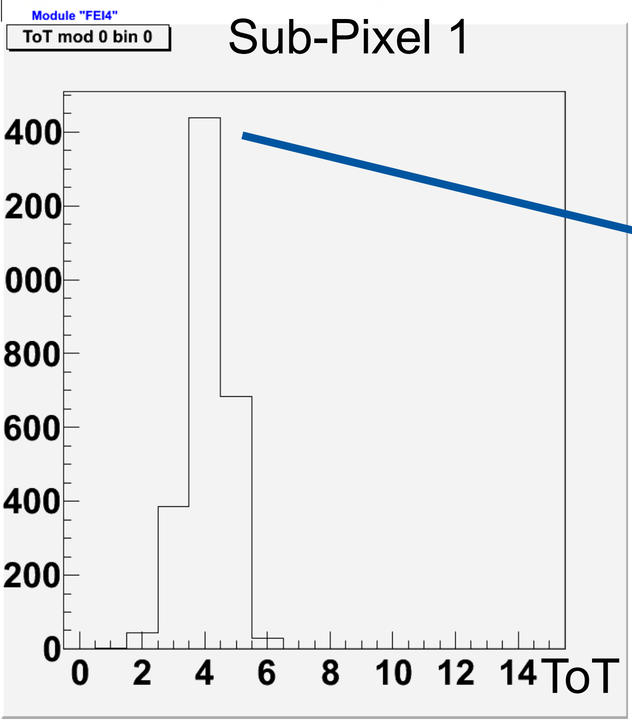


# HV2FEI4: Pixel readout

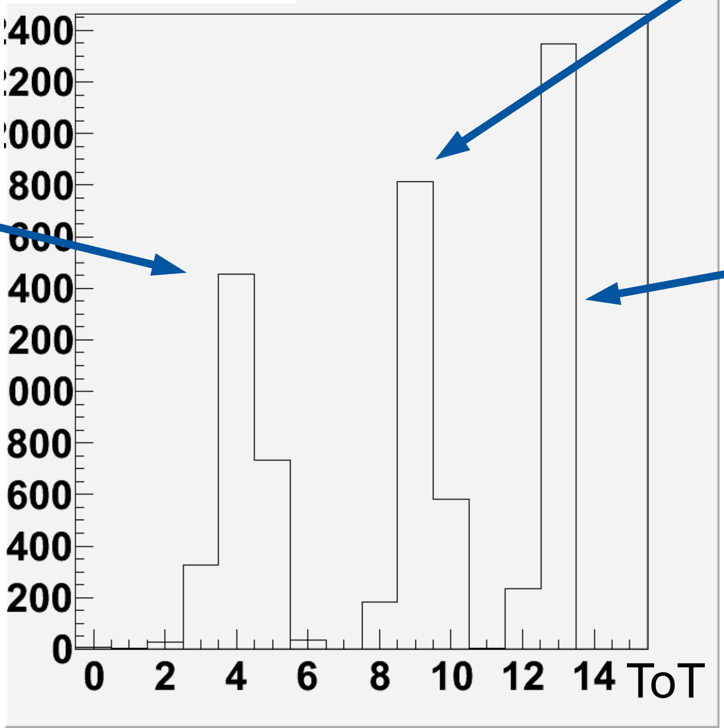
- ToT encoding:
    - 3 sub-pixels clearly distinguishable
      → sub-pixel encoding works!
    - dynamic ranges to be better matched

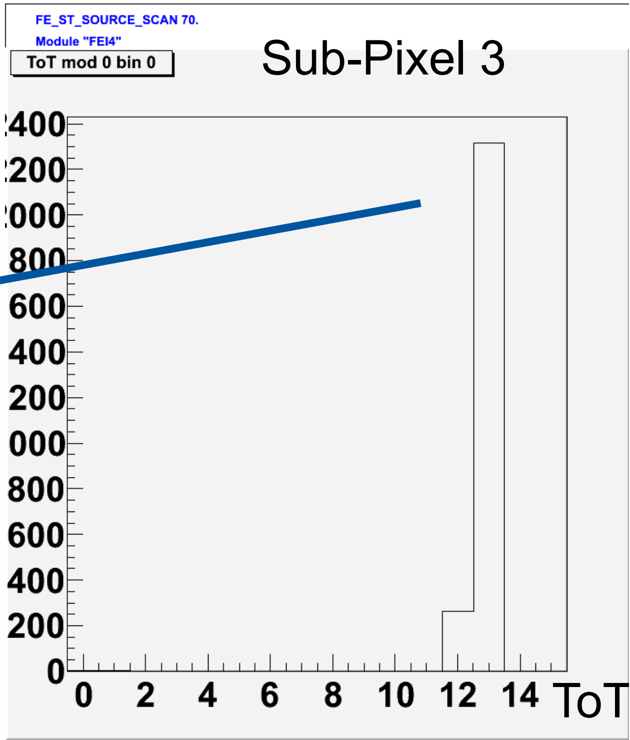






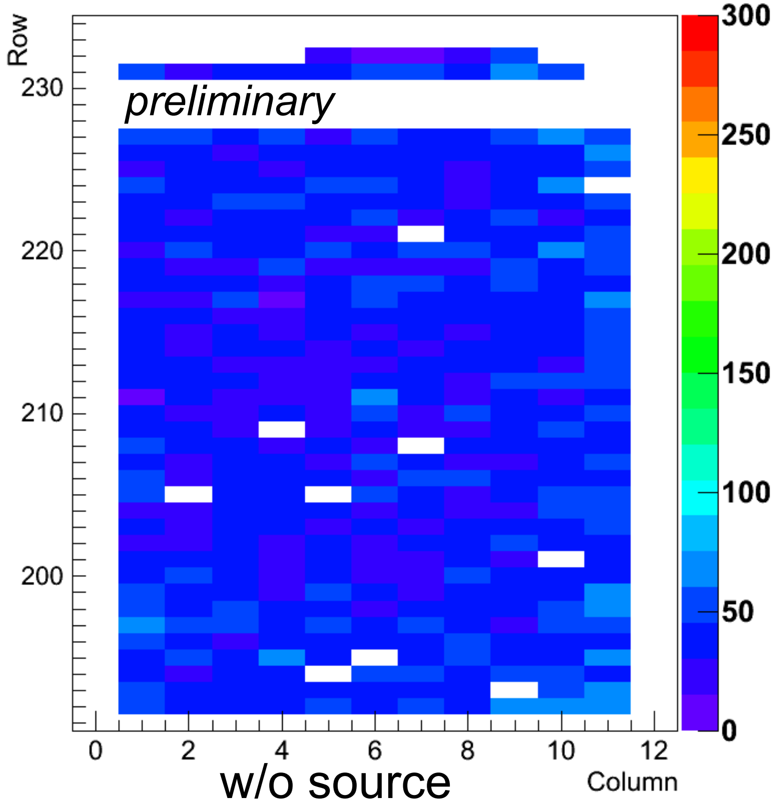
All on



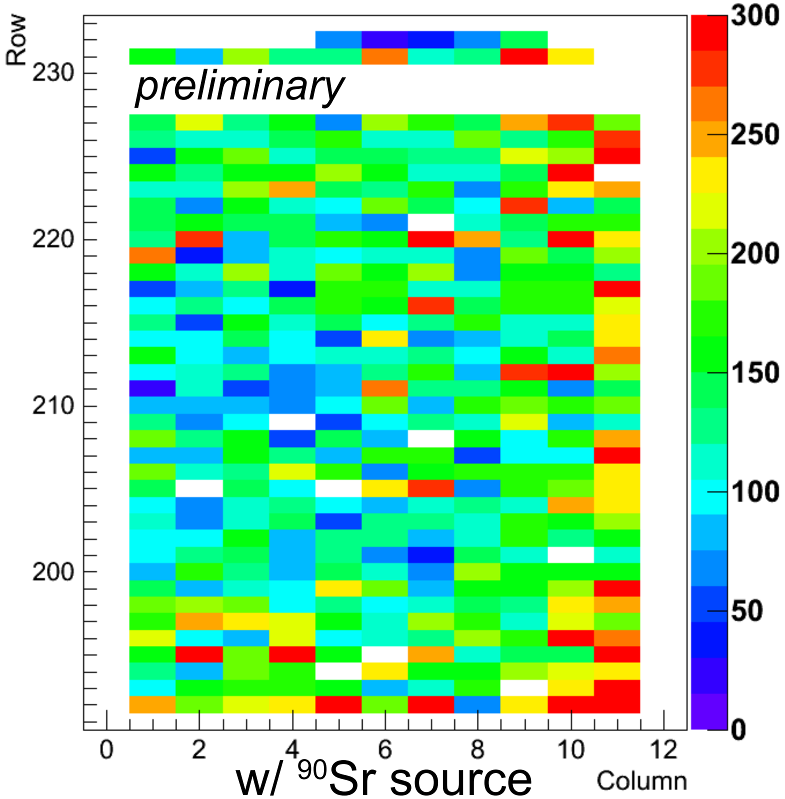


# n-irradiated behaviour: 1e16 $n_{eq}/cm^2$

- irradiation done at Ljubljana (thanks!) w/o biasing, low TID
- up to now measurements at room temperature (!), o(20) days of RT annealing
- for now with (only) -20V to -25V bias voltage
- noise occupancy at ~$10^{-10}$, but threshold currently uncalibrated
- below: about ~10 minutes exposure, self-trigger (!) source scan with and without $^{90}$Sr source



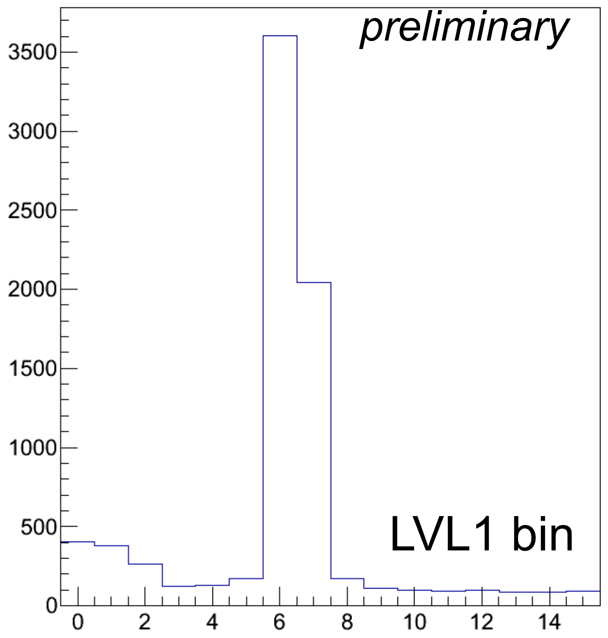
w/o source

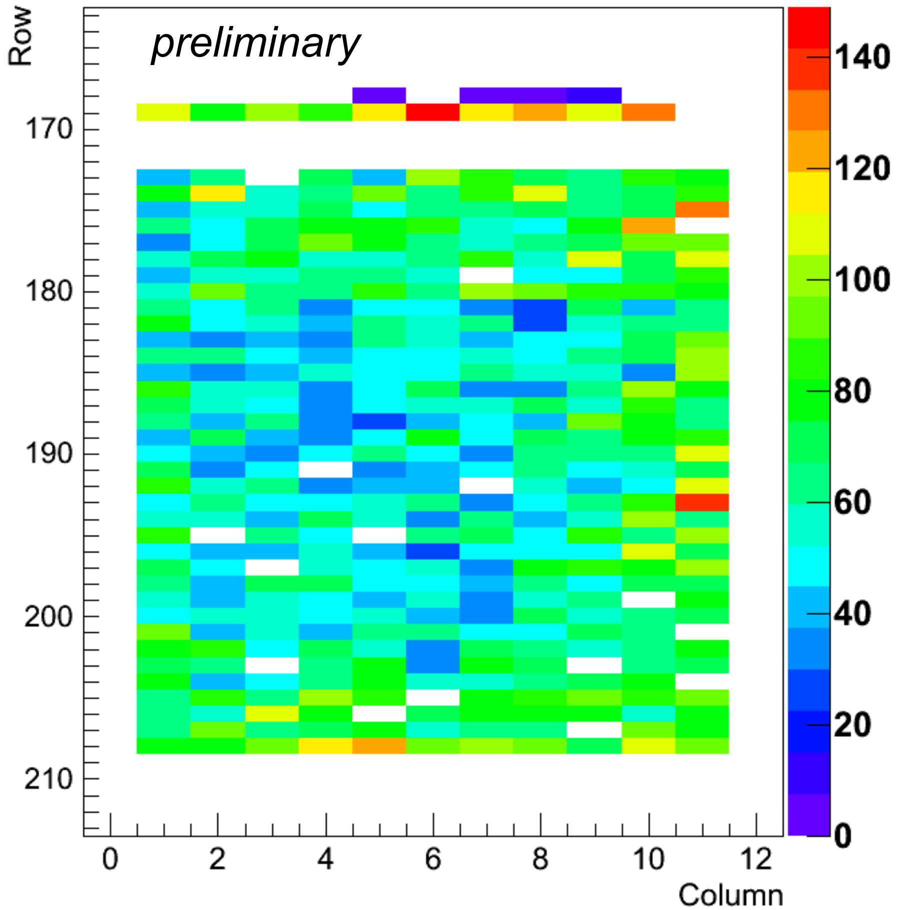


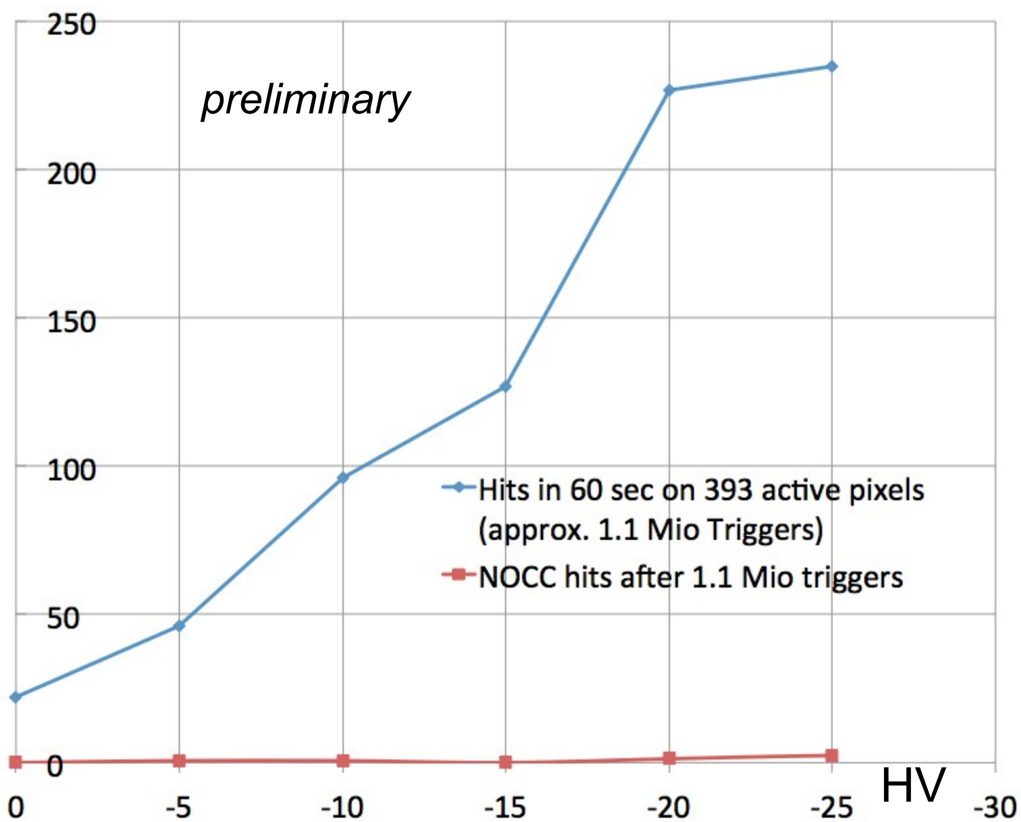
w/ $^{90}$Sr source

# Irradiated behaviour: 1e16 $n_{eq}/cm^2$

- measurements with scintillator trigger
  - makes sure we select MIP-like electrons
  - avoids “noise” triggers
  - rate rises with HV as expected, but (rate!) saturation not yet seen → go higher in HV
- next steps: calibration, cooled operation





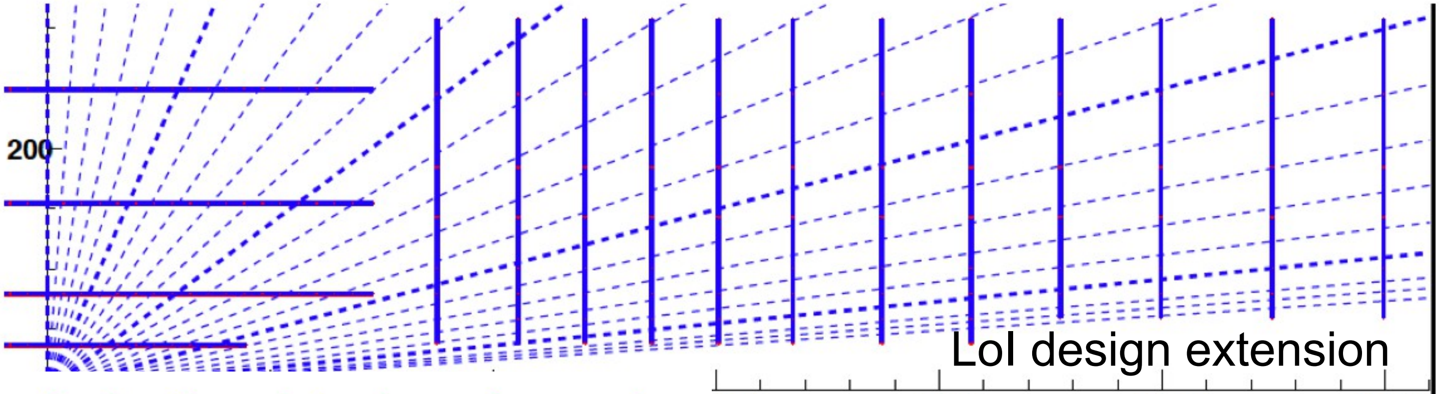


# Future plans

- More pixel assemblies being put together
  - some unirradiated for technology development
  - a bump-bonded one in preparation at Glasgow for comparison
  - more neutron-irradiated to look at (1e15 and 1e16 neq/cm2)
  - already one HV2FEI4_v2 pixel assembly existing, working on changes to the devices' configuration
- USBPix is being modified to enable configuration only with USBPix/STControl (M. Backhaus, U Bonn)
  - makes implementation of scans much easier
- further submissions are being discussed
  - dedicated to strip readout
    - optimised sub-strip pitch (50 μm? 25 μm?) in combination with z-resolution
  - dedicated to disks
    - square pixels preferred
    - 50x50 μm should be achievable with FE-I4
    - sensor candidate for “standard disks” and for very forward tracking

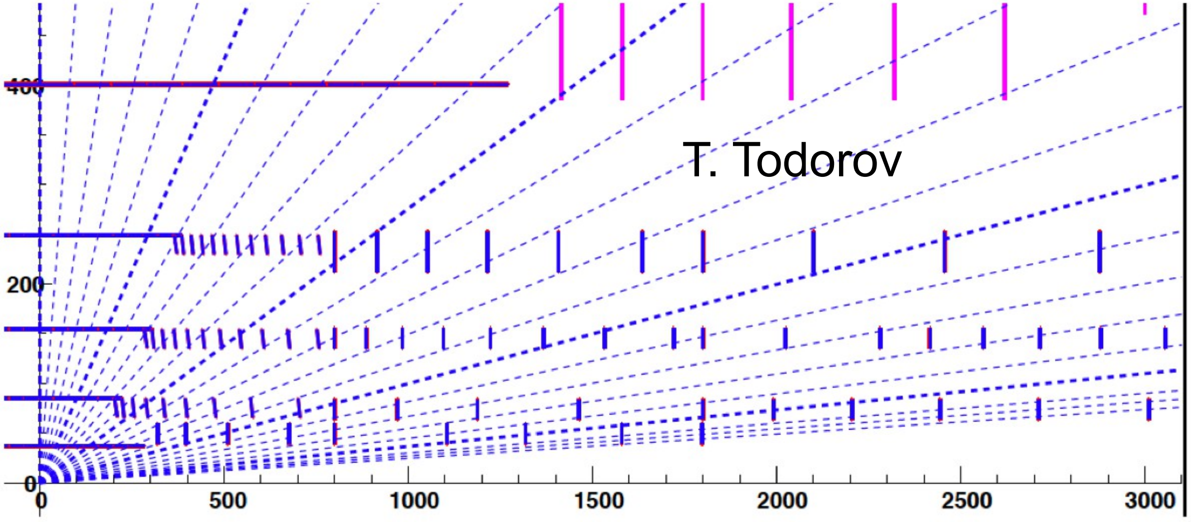
# Case study: Very forward tracking

- Limitation to pseudorapidity of eta = 2.5 inappropriate wrt VBF/VBS
- Design studies ongoing for an extension to eta~4 (phase 2 upgrade)
    - physics: Higgs self-coupling, vector boson scattering
    - layout: acceptable area increase
    - sensor challenges: mass production, rad-hardness at small radii, square pixels/small eta pitch preferred → HV-CMOS?

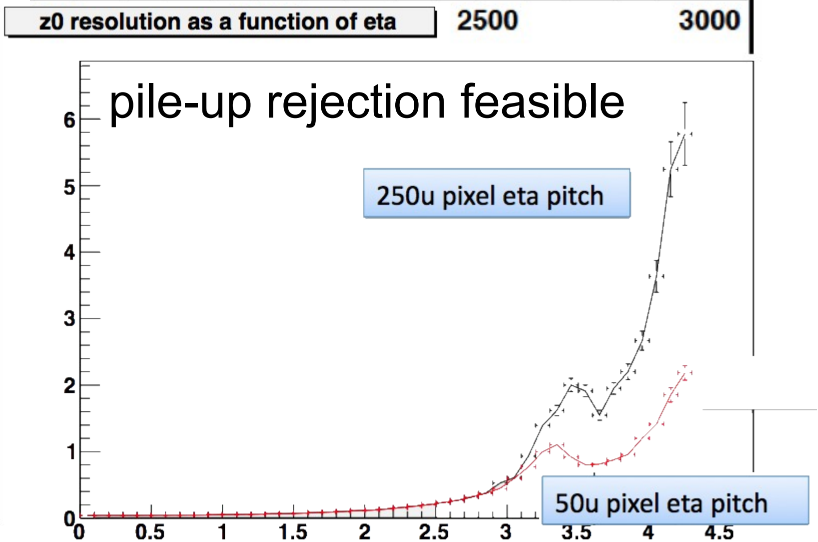


LoI design extension

Alpine stave design extension

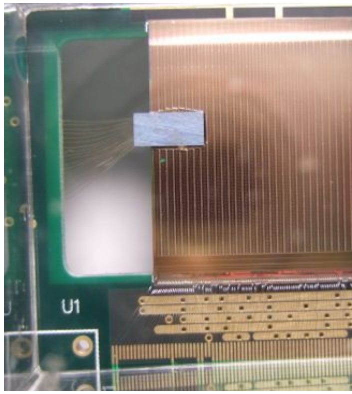


T. Todorov

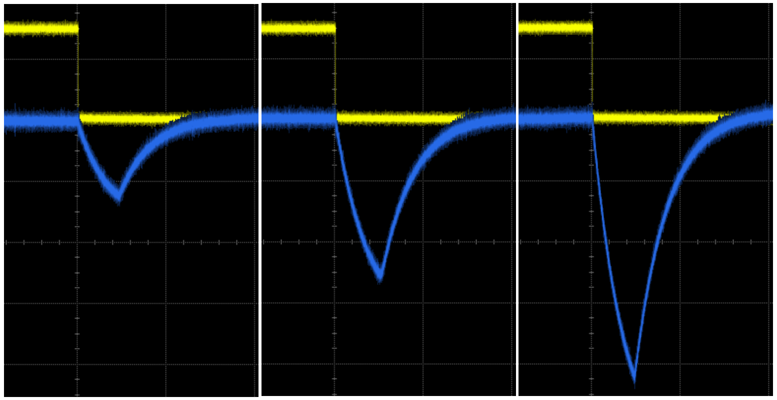


pile-up rejection feasible

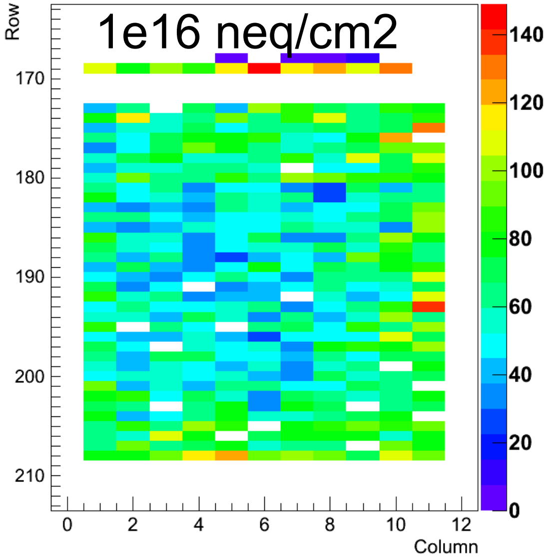
# Conclusions

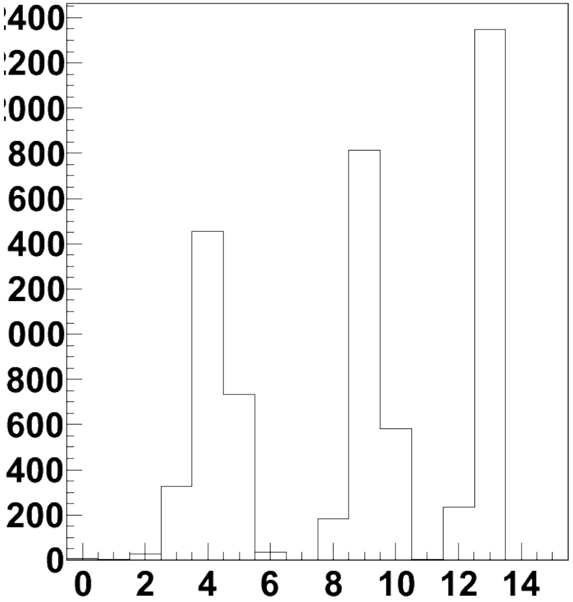


- HV-CMOS processes might yield radiation-hard, low-cost, improved-resolution, low-bias-voltage, low-mass sensors
- Process can be used for
  - 'active' n-in-p sensors with capacitive coupling (ATLAS)
  - drift-based MAPS chips (μ3e-experiment at PSI)
- First active sensor prototypes being explored within ATLAS
  - initial design too TID-soft, 2nd iteration being tested now
  - nevertheless, results with capacitively coupled pixel sensors look promising
  - "virtual" strip sensors – z-position encoding works



Row 0 Row 12 Row 23



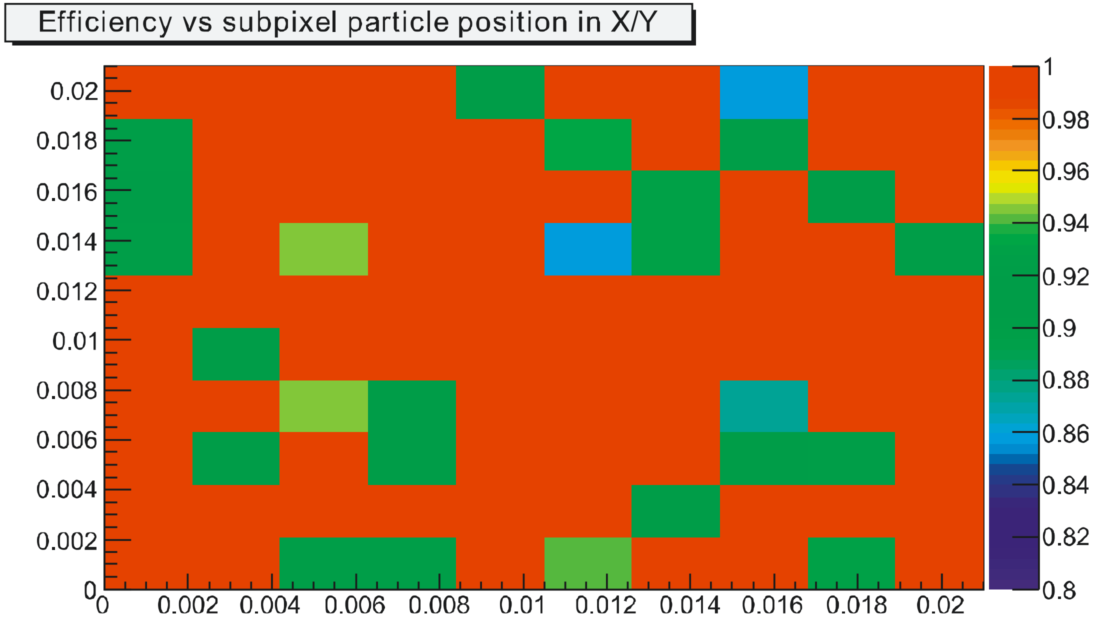


- Future submissions still in 2013 will aim towards geometrically realistic prototypes

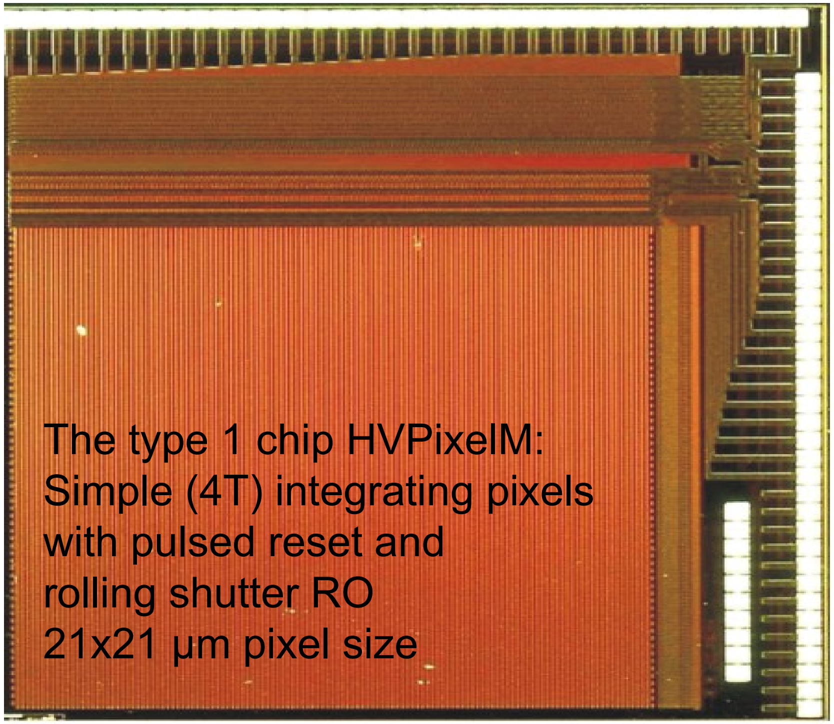
# Backup slides

# Test beam results: monolithic

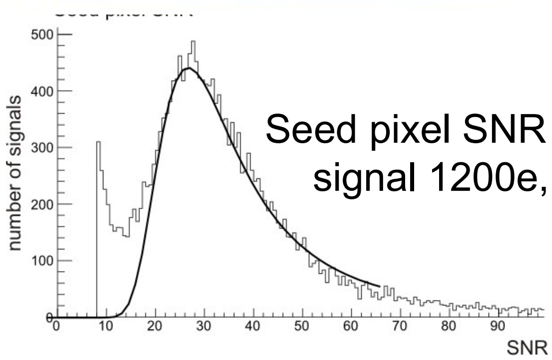
- excellent resolution
- very good S/N ratio
- efficiency limited by readout artifacts:
  - column-based readout
  - row not active during readout
  - data analysis did not correct for this
  - very small chip → low statistics



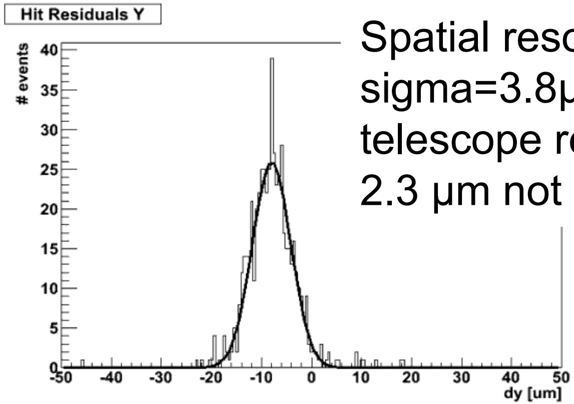
Efficiency vs. the in-pixel position of the fitted hit. Efficiency at TB: ~98% (probably due to a rolling shutter effect)



The type 1 chip HVPixelM:
Simple (4T) integrating pixels
with pulsed reset and
rolling shutter RO
21x21 µm pixel size



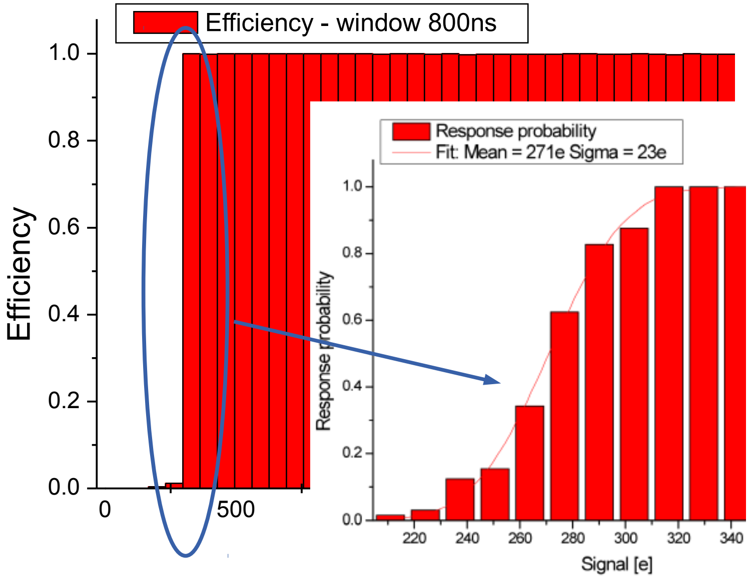
Seed pixel SNR 27, seed signal 1200e, cluster 2000e



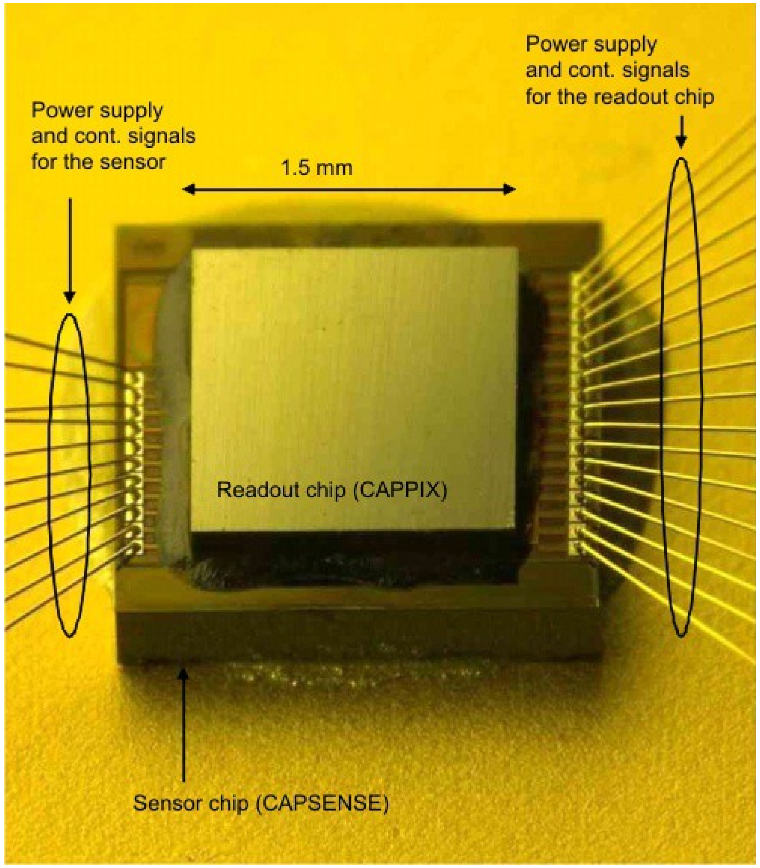
Spatial resolution:
sigma=3.8µm,
telescope resolution of
2.3 µm not subtracted

# CPPD prototype results

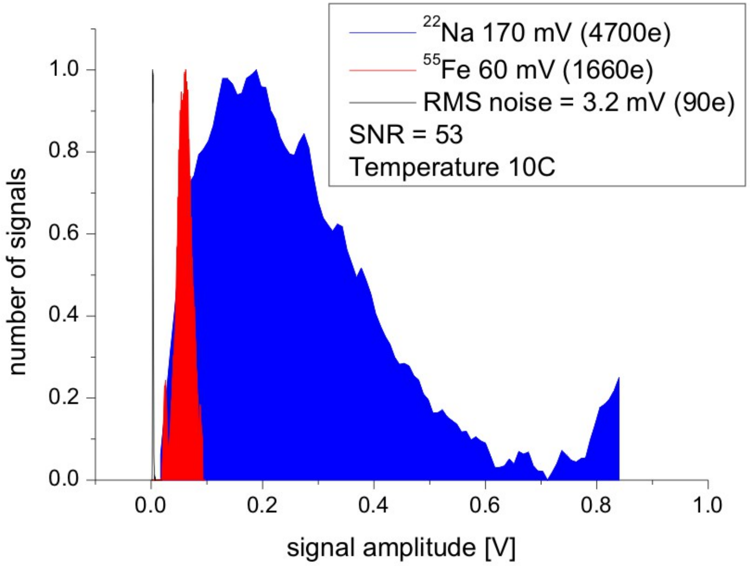
- excellent noise behaviour: stable threshold at ~330 electrons
- good performance also after irradiation



Detection efficiency vs. amplitude
Detection of signals above 330e possible with >99% efficiency.



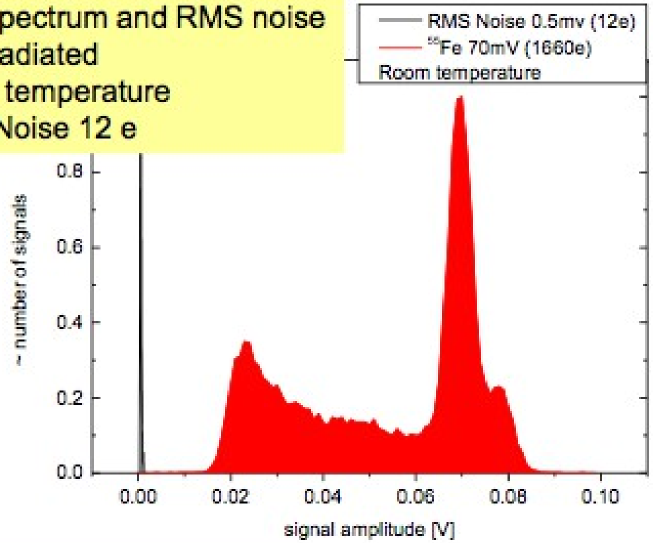
CAPPIX/CAPSENSE edgeless CCPD
50x50 μm pixel size



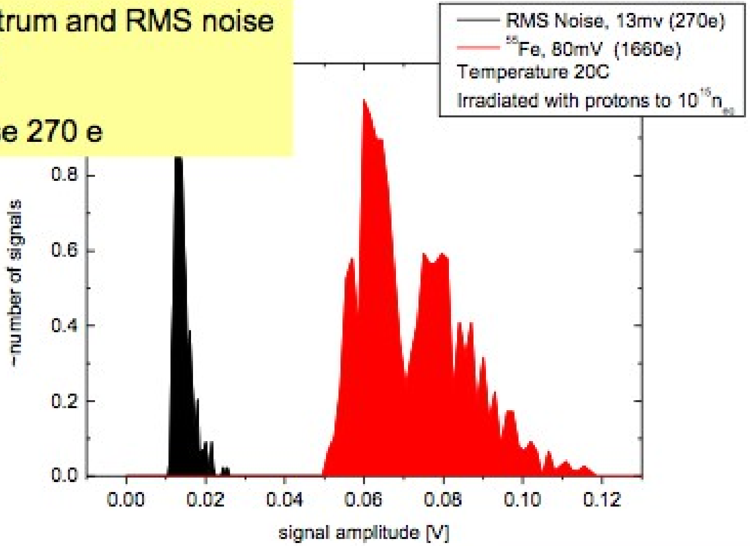
Signals and noise of a CAPSENSE pixel after $10^{15} n_{eq}/cm^2$

# CPPD prototype results

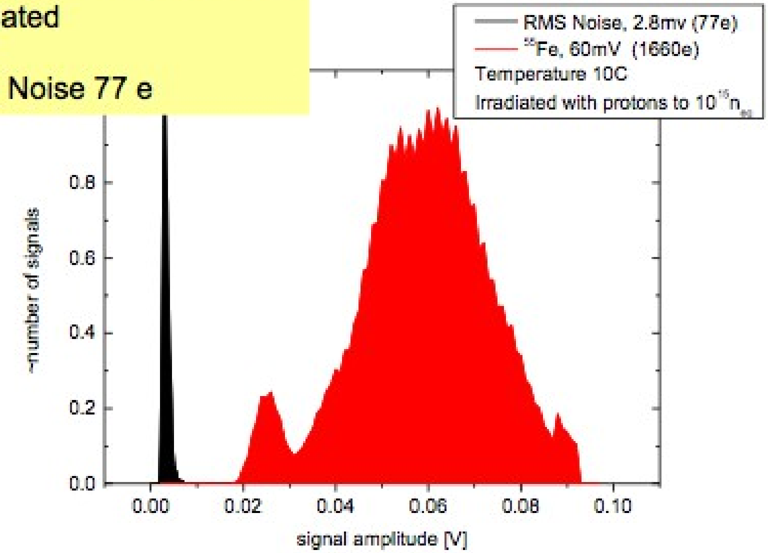
- Irradiation with 23 MeV protons: 1e15 neq/cm2, 150MRad
- FE-55 performance recovers after slight cooling



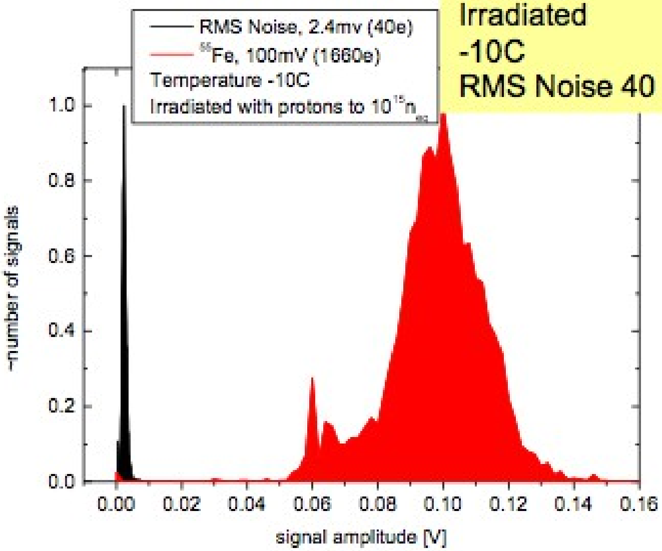
$^{55}$Fe spectrum and RMS noise
Not irradiated
Room temperature
RMS Noise 12 e



$^{55}$Fe spectrum and RMS noise
Irradiated
20C
RMS Noise 270 e



$^{55}$Fe spectrum, RMS noise
Irradiated
10C
RMS Noise 77 e



$^{55}$Fe spectrum, RMS noise
Irradiated
-10C
RMS Noise 40 e