



Update on SCP Slim Edges

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Acknowledgement:

*1) Technical Guidance and Support by
Marc Christophersen*, Bernard F. Philips*
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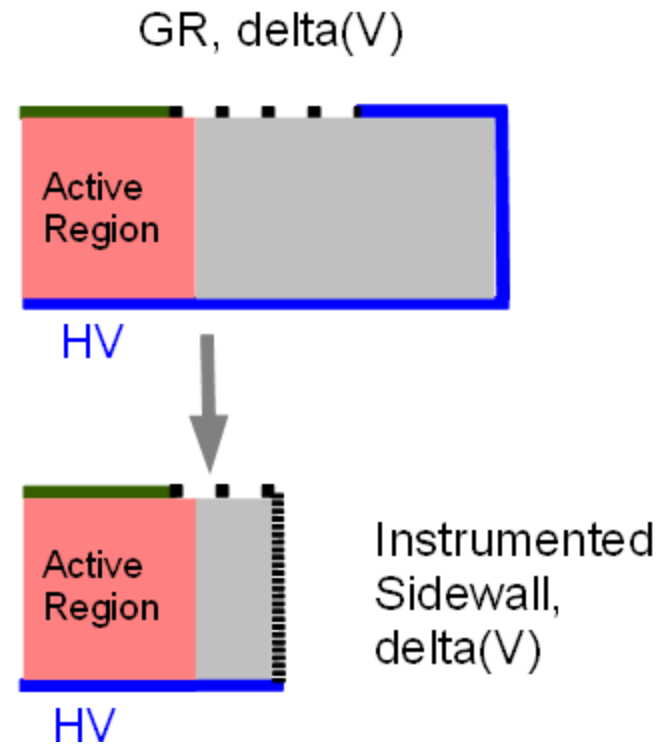
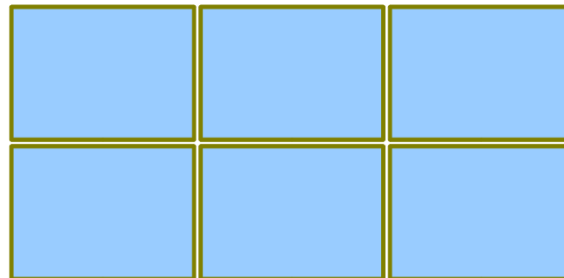
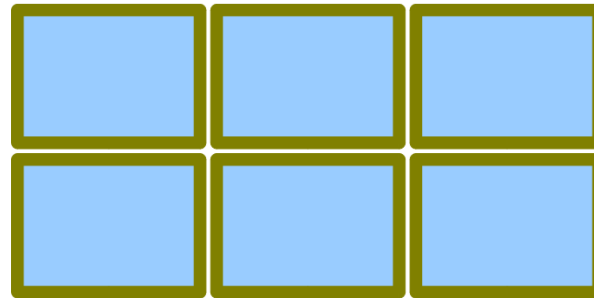
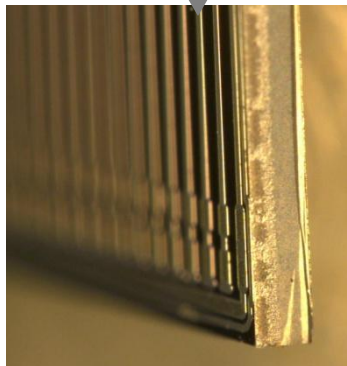
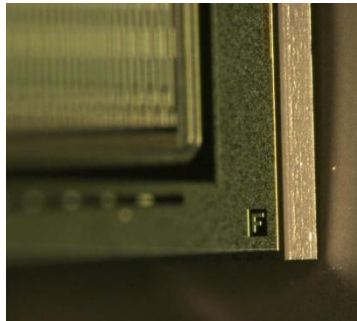
2) Our numerous collaborators from ATLAS and RD50!

Slim Edges -- Motivation



Basic Idea: To minimize ~1 mm wide inactive peripheral region. This is relevant for “tiling” (as opposed to “shingling”) of large-area detector composed of small sensors.

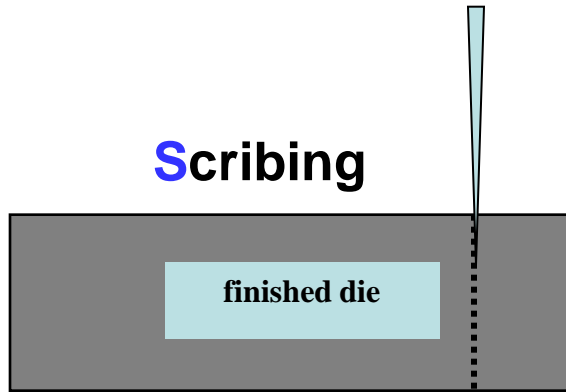
Basic Method: To instrument the sidewall in a close proximity to active area, such that it's resistive.



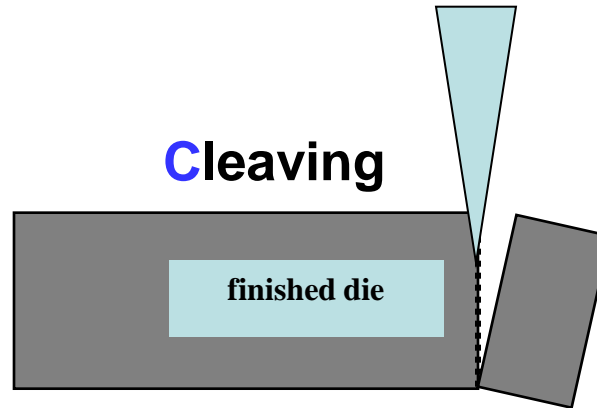
Method -- SCP Treatment



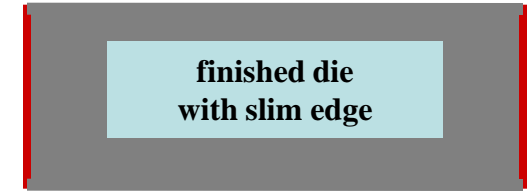
Scribing



Cleaving



Passivation



- Diamond stylus
- Laser
- XeF₂ Etch
- DRIE Etch

- Tweezers (manual)
- Loomis Industries, LSD-100
- Dynatex, GTS-150

Native Oxide
+ Radiation
or:

N-type

P-type

- Native SiO₂ + UV light or high T
- PECVD SiO₂
- PECVD Si₃N₄
- ALD “nanostack” of SiO₂ and Al₂O₃
- ALD of Al₂O₃

All Treatment is post-processing & low-temp
(Etch-scribing can be done during fabrication)

Basic requirement: 100 wafers (for rectangular side cleaving) with reasonably good alignment between sensor and lattice.

Current Efforts



We had a lot of technical development, with different fabrication options explored. For details, see recent publications:

- M. Christophersen et al., "Alumina and Silicon Oxide/Nitride Sidewall Passivation for P- and N-Type Sensors", NIM A 699 (2013) 14
- M. Christophersen et al, "The effect of different dicing methods on the leakage currents of n-type silicon diodes and strip sensors", Solid-State Electronics 81 (2013) 8.
- M. Christophersen et al, "Scribing-Cleaving-Passivation for High Energy Physics Silicon Sensors", Proceedings of Science, accepted for publication.
- V. Fadeyev et al, "Scribe-cleave-passivate (SCP) slim edge technology for silicon sensors", NIM A (2013) – in press. DOI: <http://dx.doi.org/10.1016/j.nima.2013.03.046>

An interesting development is slim edge implementation as a part of low-R submission. → V. Benitez talk.

Recent work is focused on two aspects of device performance:

- CCE near the edge
- Radiation hardness

Asides:

- Application for proton tomography.
- Inter-strip with alumina passivation.

Charge Collection Testing



Sensor Type	Origin	Edge-Active area Distance [um]	Signal Readout	Beam	Ref
P-type strips	PPS (CIS)	~200	Binary (PTSM)	⁹⁰ Sr	V. Fadeyev <i>et al</i> Pixel 2012, NIM A in press
N-type strips	GLAST (HPK)	~200	Analog (ALiBaVa)	⁹⁰ Sr	R. Mori <i>et al.</i> 2012 JINST 7 P05002
P-type strips	PPS (CIS)	150	Analog (ALiBaVa)	Focused X-ray	R. Bates <i>et al.</i> , 2013 JINST 8 P01018
P-type 3D pixels	IBL (CNM)	50	FE-I3 & FE-I4	CERN Test Beam	S. Grinstein <i>et al.</i> , RESMDD12 G. Pellegrini <i>et al.</i> , Pixel 2012, NIM A in press
P-type strips	PPS (CIS)		Analog (ALiBaVa)	⁹⁰ Sr	

In all cases CCE on the edge was within few % of CCE on other electrodes
 → BUT: all un-irradiated devices.

New development: MPI study has device irradiation in progress. **See Anna Macchiolo's presentation on Wednesday.**

1. 2010 Proton Irradiation Studies @LANL



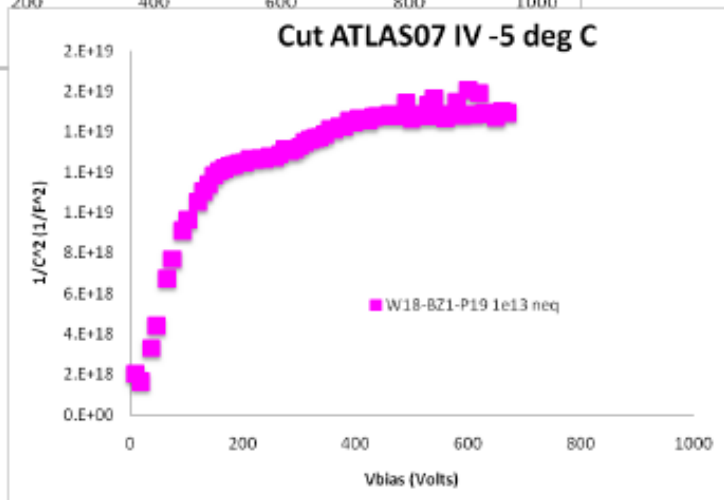
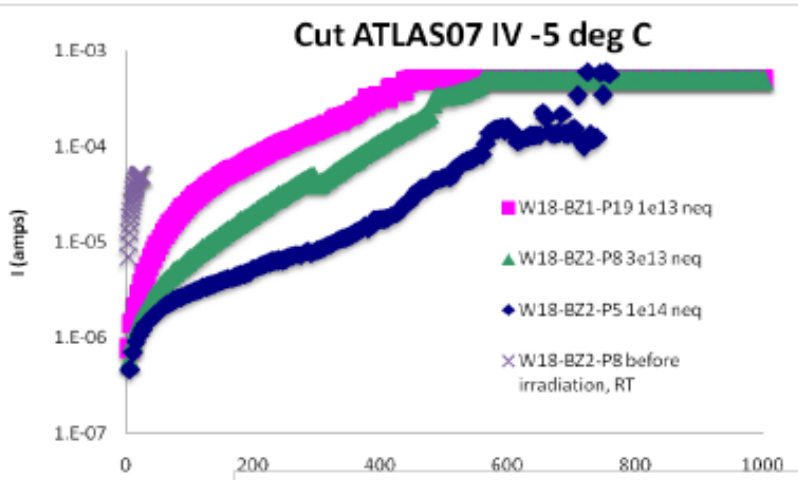
S-C only: No Passivation

P-type HPK (ATLAS07)

These sensors did not work after cleaving (initial trial without sidewall passivation). Breakdown at ~few Volts. There is an empirical evidence that the breakdown improves after irradiation.

We put these sensors in proton beam to see if they would indeed improve.

Leakage is initially dominated by the edge current, which is reduced with fluence. At 10^{14} neq, $I(\text{edge}) < I(\text{bulk})$.



Comparison of expected and observed currents at 200 V

Area [cm ²]	1		
Alpha	4.00E-17		
Thickness [cm]	0.03		
T factor	16		
Irradiation	1.00E+13	3.00E+13	1.00E+14
I_expect (200V)	7.50E-07	2.25E-06	7.50E-06
I_observe(200V)	7.39E-05	2.02E-05	5.16E-06
observe/expect	98.57	8.99	0.69

Observation #1 on S-C only p-type:
High fluence irradiation -> resistive edge!

2. 2011 Proton Irradiation @LANL

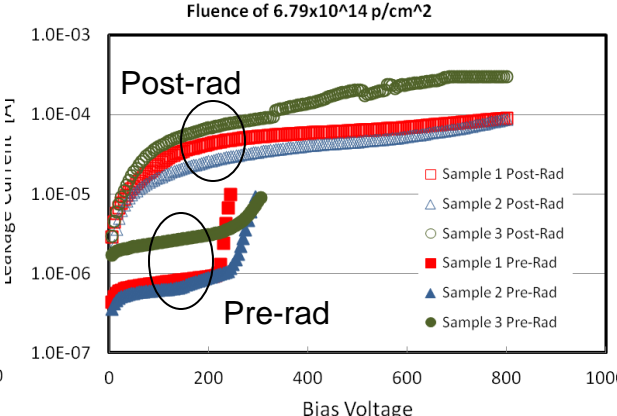
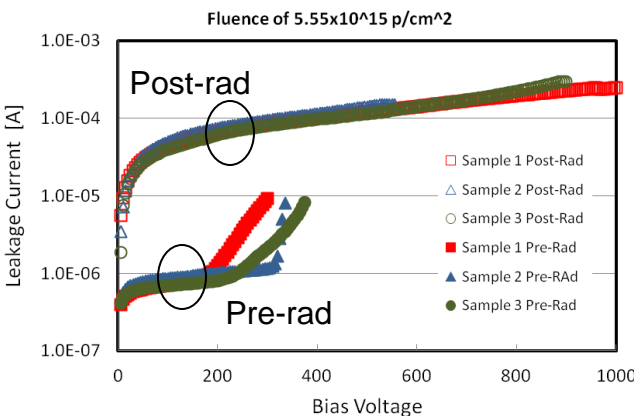
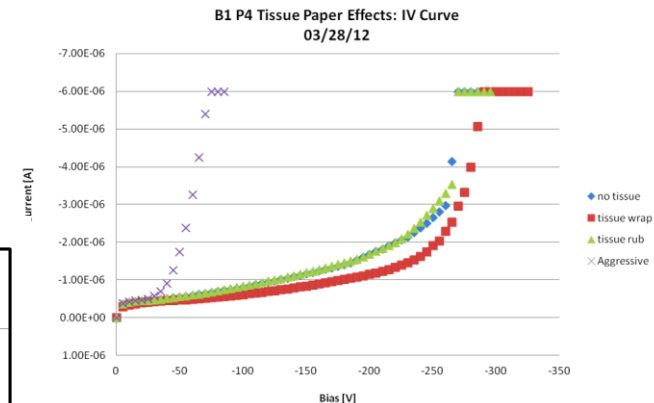


Irradiated 12 SCP processed p-type strip devices (CIS courtesy A. Macchiolo) at LANL (thanks S. Seidel). Results are in-conclusive:

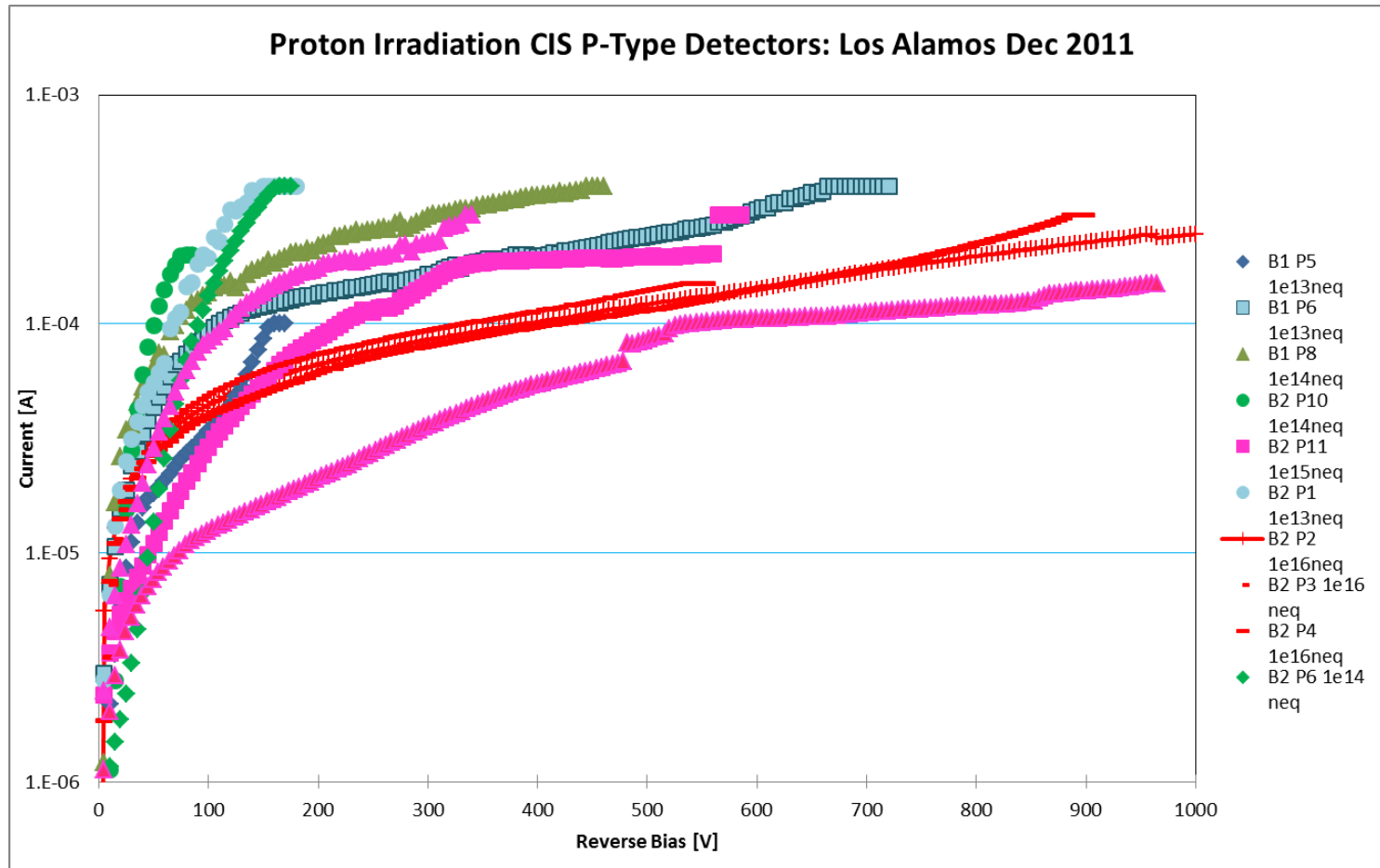
- + Breakdown voltages extended post-rad
- + High fluence devices (3/3 for $1e16\text{neq}$, 3/3 for $1e15\text{neq}$) show expected post-rad leakage current
- Lower fluence devices (1/3 for $1e13\text{neq}$ and 1/3 for $1e14\text{neq}$) show earlier breakdown!

Sensor	Before Irradiation	After Irradiation		Fluence	No Guard Rings
	V(break) at $\sim 10\ \mu\text{A}$	V(break) at $\sim 100\ \mu\text{A}$			
B1 P5	30	460		10^{13}	1
B1 P6	290	165		10^{13}	1
B2 P1	410	80		10^{13}	3
B1 P8	15	90		10^{14}	5
B2 P10	310	80		10^{14}	5
B2 P6	390	100		10^{14}	1
B2 P8	300	>800		10^{15}	4
B2 P9	310	335		10^{15}	5
B2 P11	250	>800		10^{15}	2
B2 P2	305	390		10^{16}	1
B2 P3	340	330		10^{16}	3
B2 P4	380	425		10^{16}	3

A parallel investigation of the robustness of the passivation layer revealed a possible susceptibility to rough handling. There is no proof that this has skewed the irradiation results.



2. 2011 Proton Irradiation @LANL



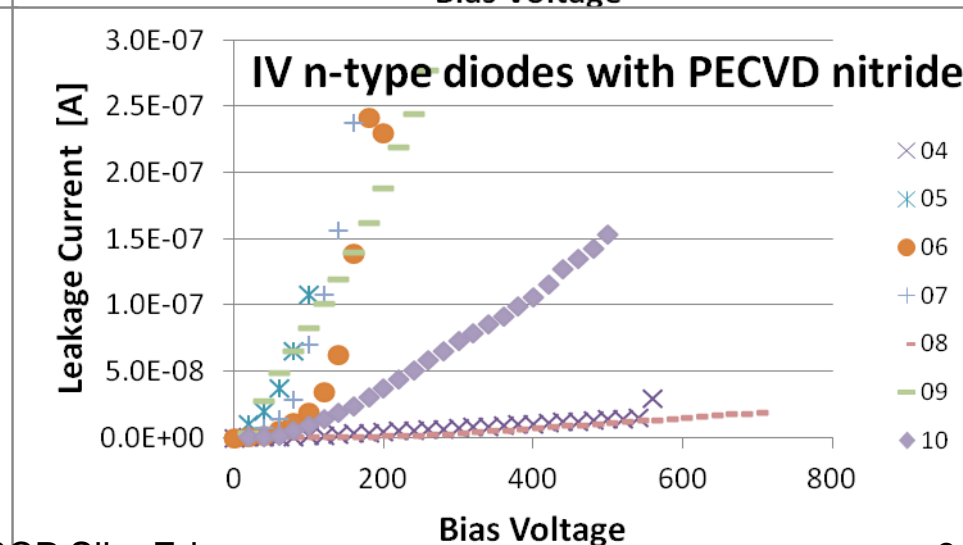
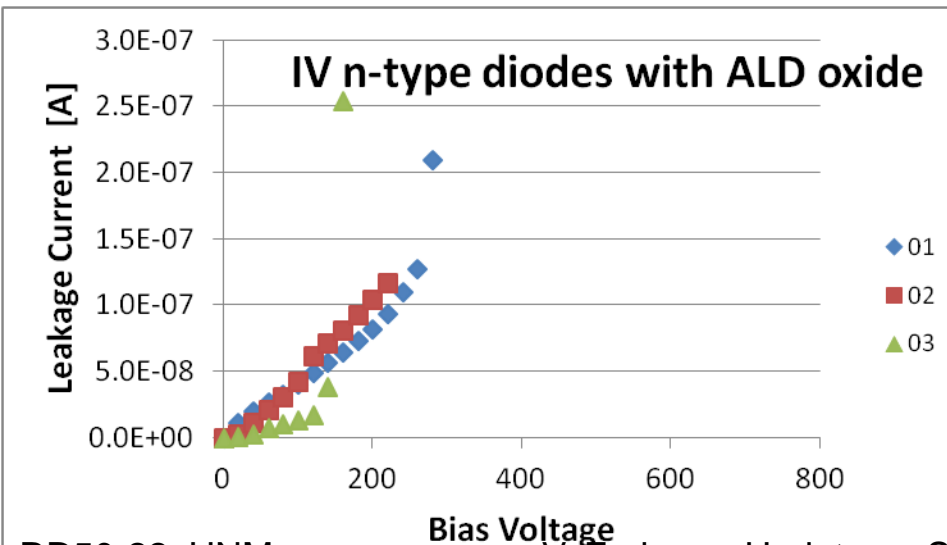
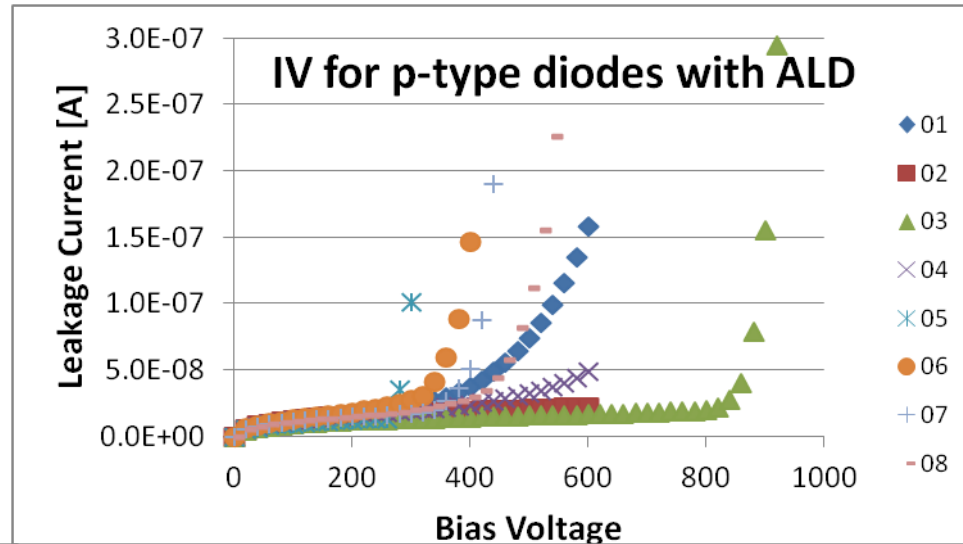
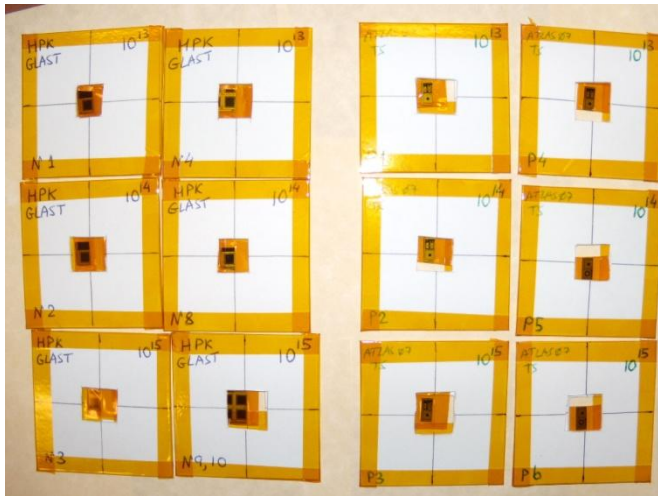
Observation #2 on S-C-P p-type:
Low fluence ($\leq 1e14$): high edge current
High fluence irradiation ($\geq 1e15$): resistive edge!

3. 2012 Proton Irradiation @CERN

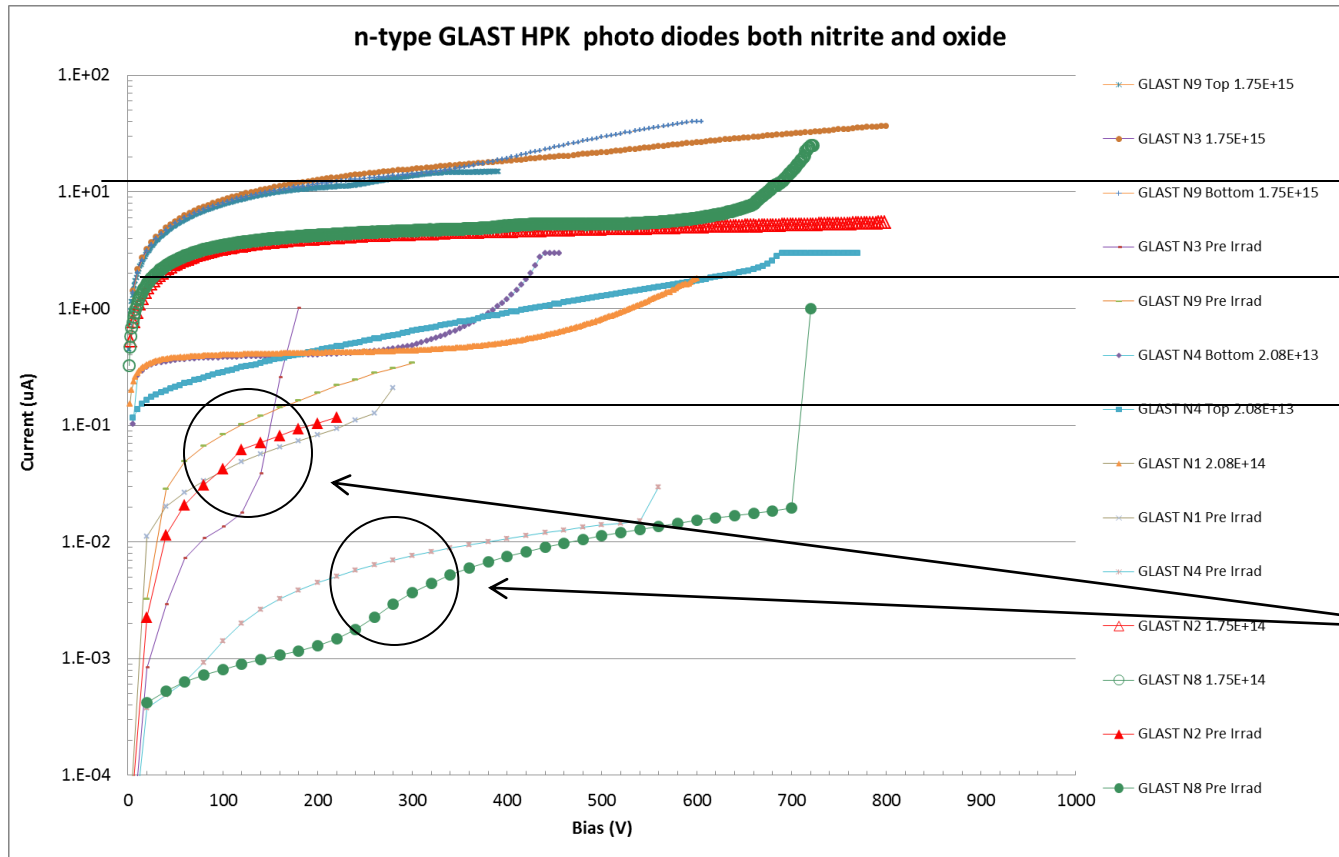


A round of irradiations at SPS (huge help from G. Casse & M. Glaser):

- p-type diodes from ATLAS07 Test Structures
- n-type diodes from Fermi/GLAST Test Structures, with both PECVD nitride and ALD oxide



n-type GLAST HPK Photo Diodes both nitrite and oxide passivation



Expected current [uA] @ -5 C

13.3

1.33

0.16

Pre-rad

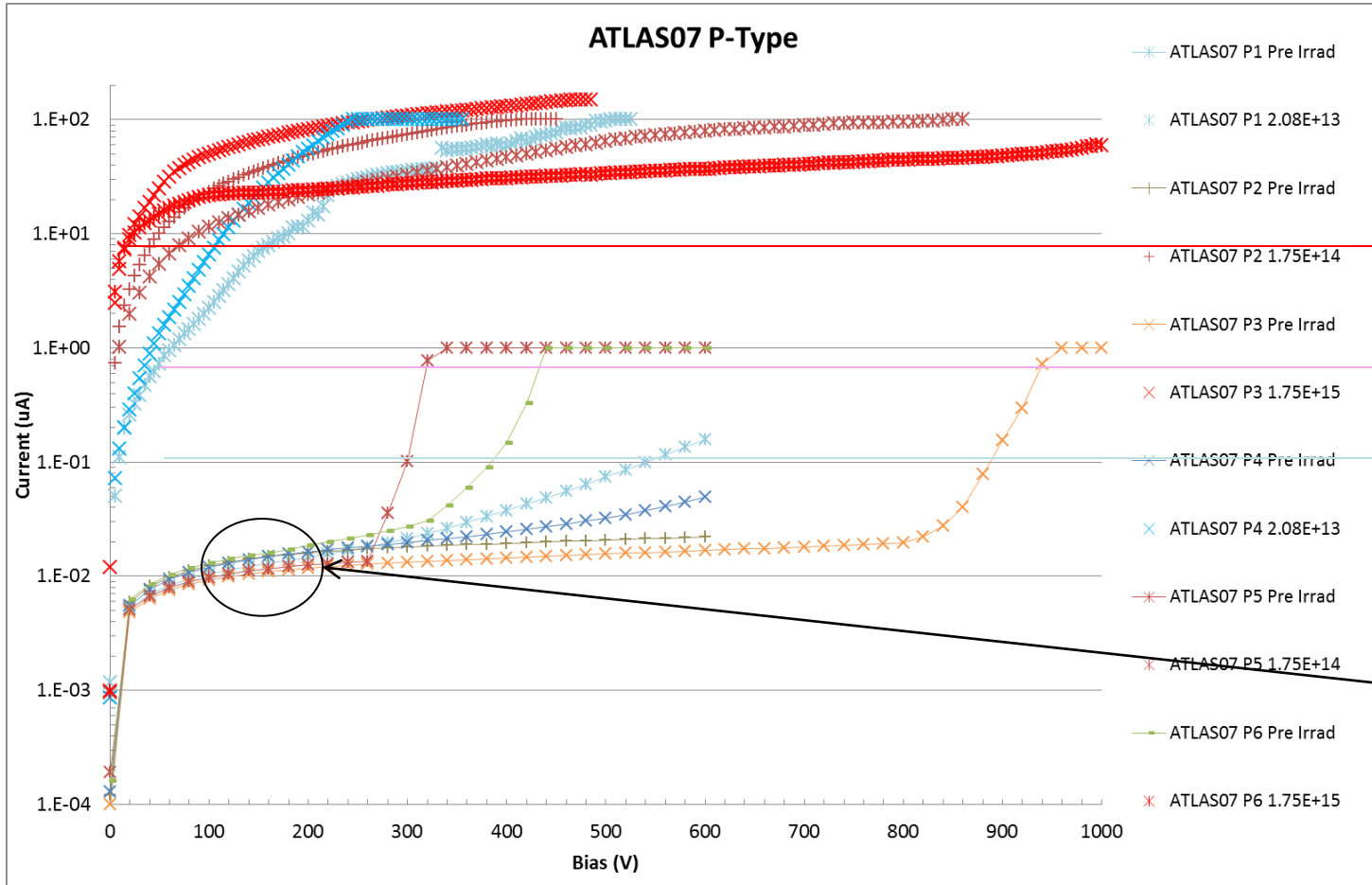
Observation #3 on S-C-P n-type:

low fluence ($1e^{13}$, < inversion) edge isolation due to passivation (Nitrite/nanostack)

High fluence ($>1e^{14}$, > inversion): resistive edge

...No dependence on type of passivation, leakage current close to bulk expectation

p-type ATLAS07 HPK Photo Diodes



Expected current [uA] @ -5 C

8

0.8

0.1

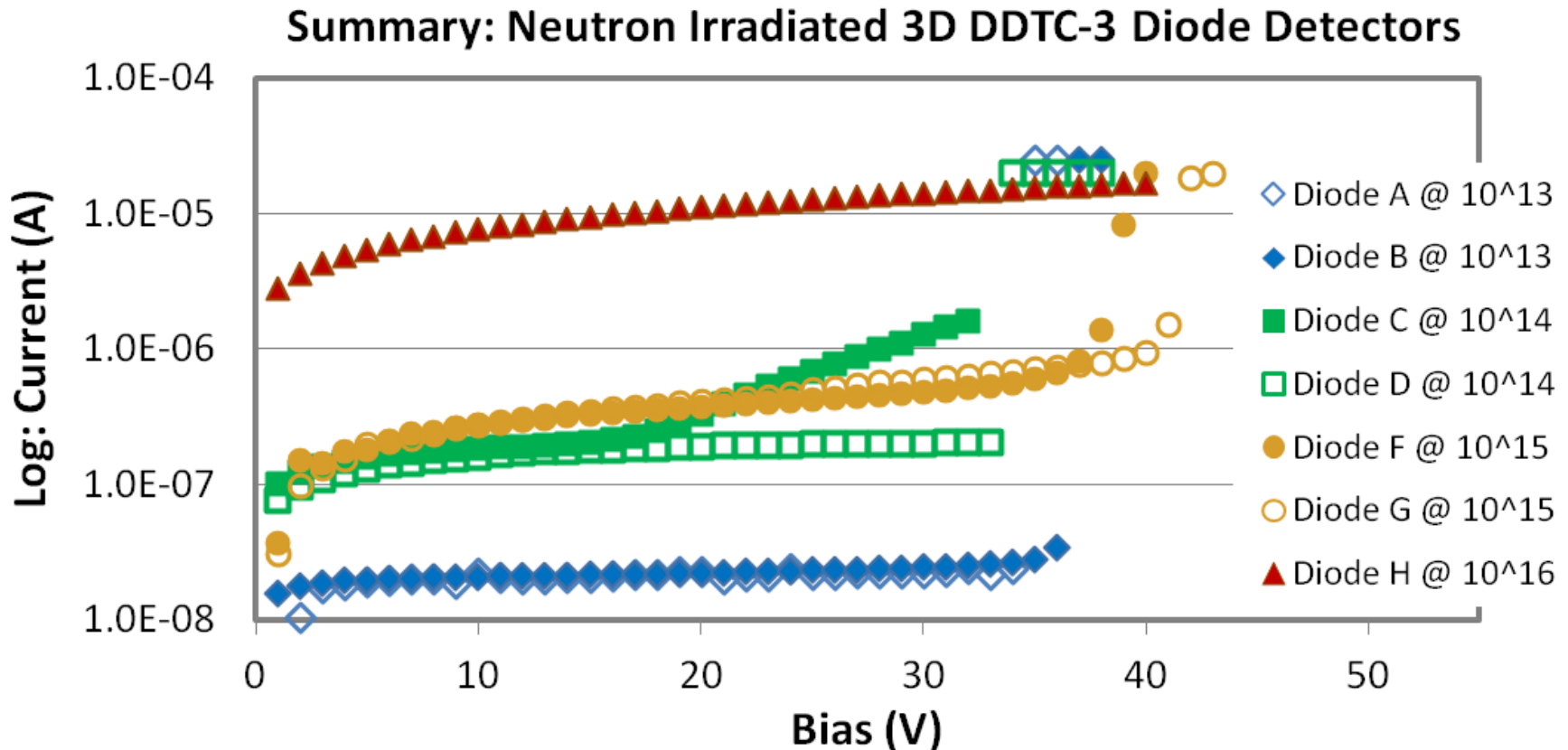
Pre-rad

Observation #4 on S-C-P p-type:
 Leakage currents do not scale with fluence
 low fluence (< 1e14): reduced edge performance
 high fluence (>1e14): resistive edge

p-type 3D sensors irradiated at Ljubljana, PI G.-F. Dalla Betta



VERY preliminary, data collection in progress



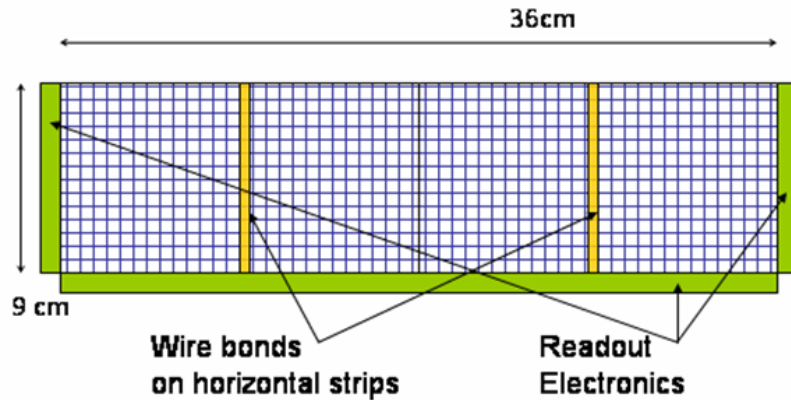
Observation #5 on S-C-P p-type:

3D neutron-irradiate sensors show approximate scaling with fluences:
no high currents for low fluences !

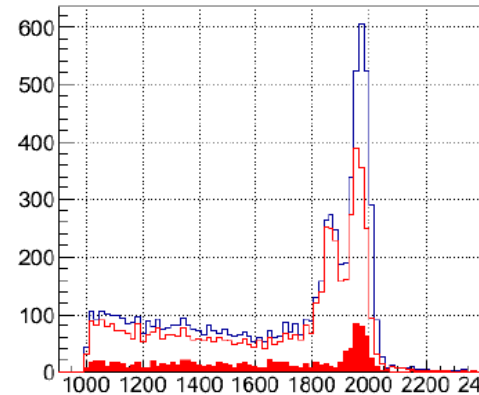
S-C-P treated SSD in pCT Tracker



Large area coverage requires tiling of 4 sensors, having ~ 1mm inactive edges which create image artifacts.



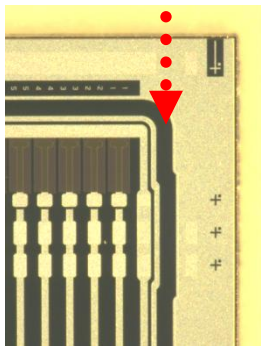
Overlapping sensors introduces artifacts requiring additional, non-uniform energy corrections



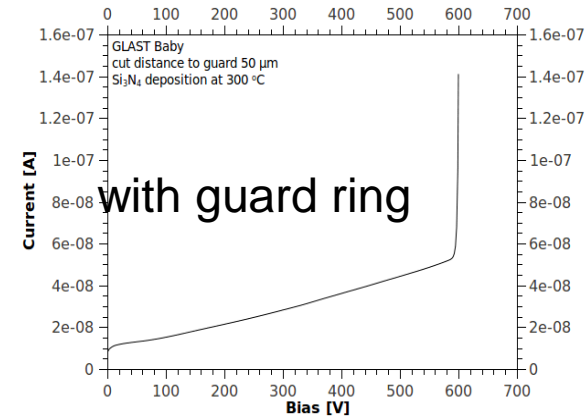
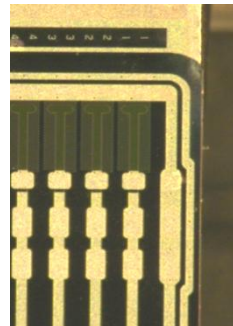
For Tiling with no Overlap: “Slim Edges”

Si SSD with 900 μ m dead edge

Cut within 50 μ m of Guard Ring



S-C-P:
Scribing (XeF_2)
+ Cleaving
+ Passivating (N_2 PECVD)

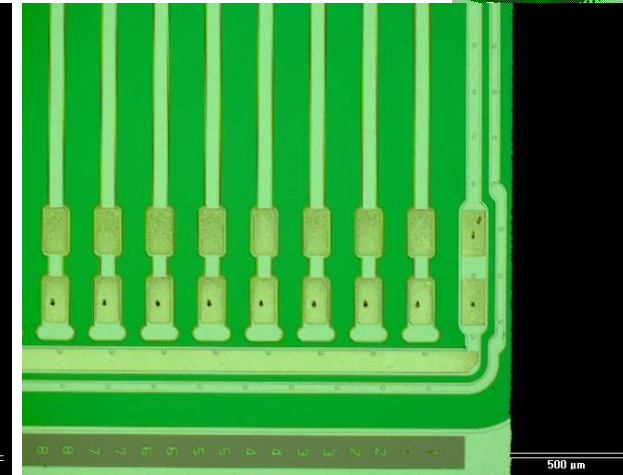
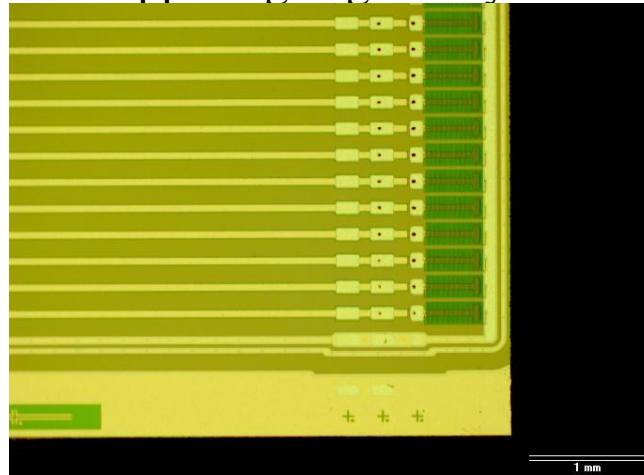
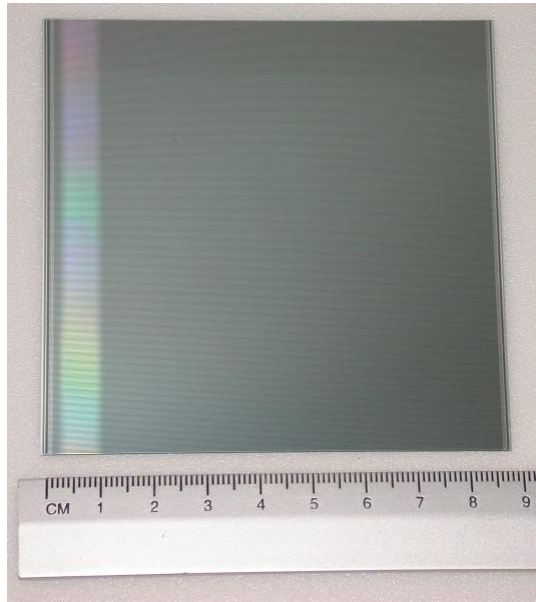


M. Christophersen et al.,
SSE 81, (2013) 8–12

S-C-P treated 9 cm x 9 cm HPK SSD (ex GLAST)

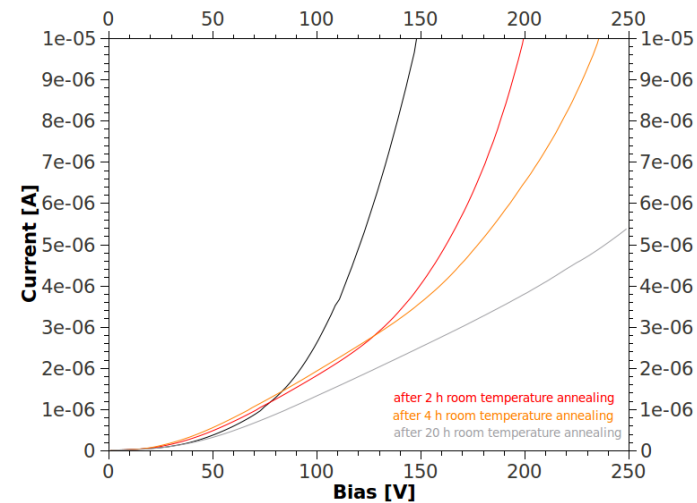
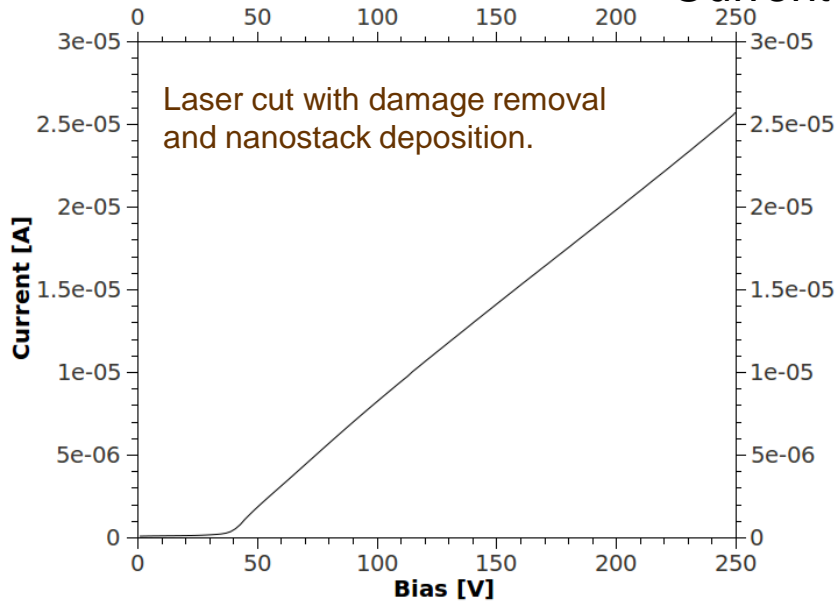


Cut 2 opposing edges only



Diced sensors => hard to cleave. But can tolerate higher currents. Can replace cleaving by laser cut. Current test (G. Pellegrini): dicing, etching, nitride.

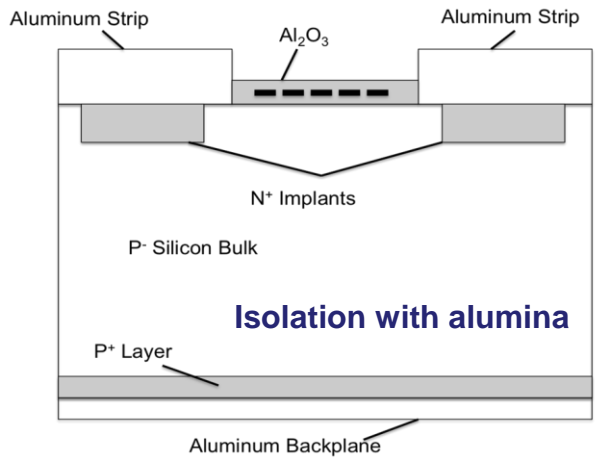
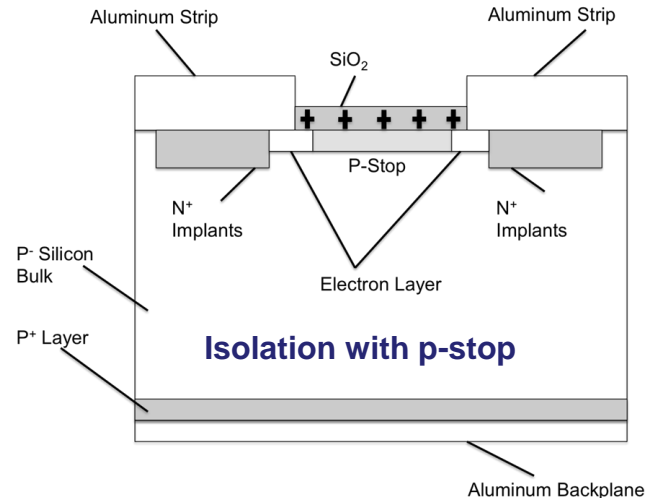
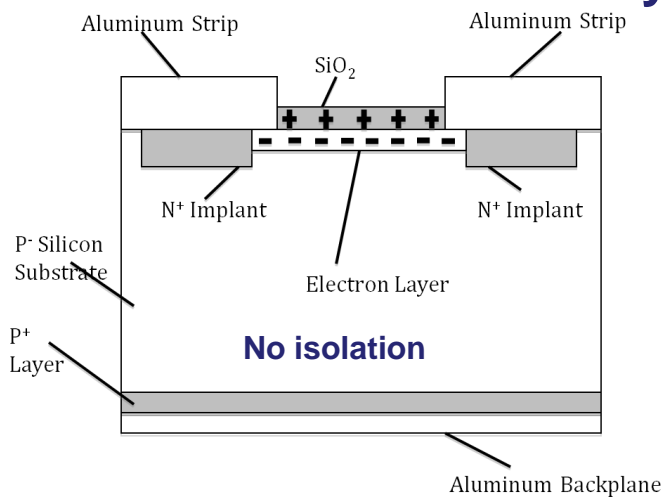
Observe considerable annealing effects!



Inter-strip Isolation with Alumina Passivation



The idea is to use the *negative interface charge* formed on the boundary of **alumina** and silicon for interstrip isolation on **p-type** devices (NRL). This is quite analogous to isolation with *positive interface charge* formed by **Si oxide** with silicon for **n-type** devices.



Test of IS with Alumina

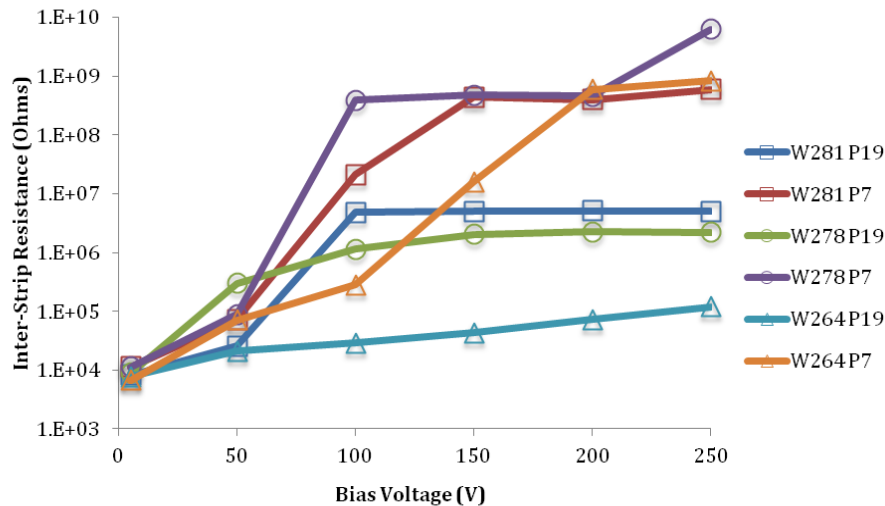


ATLAS07 (p-type) without inter-strip isolation reprocessed at NRL:

- stripped off the oxide layer
- deposited of alumina.

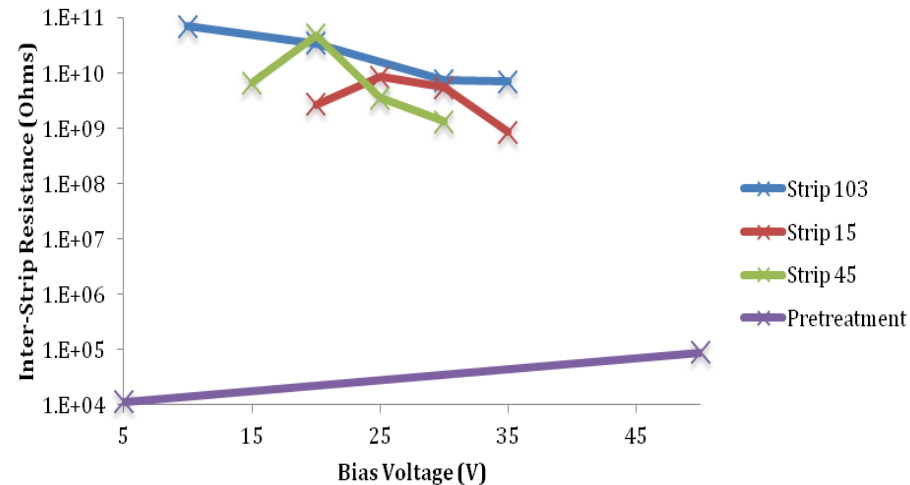
Observe high IS resistivity at lower bias voltage, characteristic of intrinsic isolation.

Inter-Strip Resistance as a Function of Bias Voltage



before

Inter-strip Isolation ATLAS07 BZ1 W278 P07



after

Conclusions and Future Work



- Had multiple studies of CCE near the edge on un-irradiated sensors. So far no issues.
- Will be interesting to see results from MPI studies on irradiated devices.

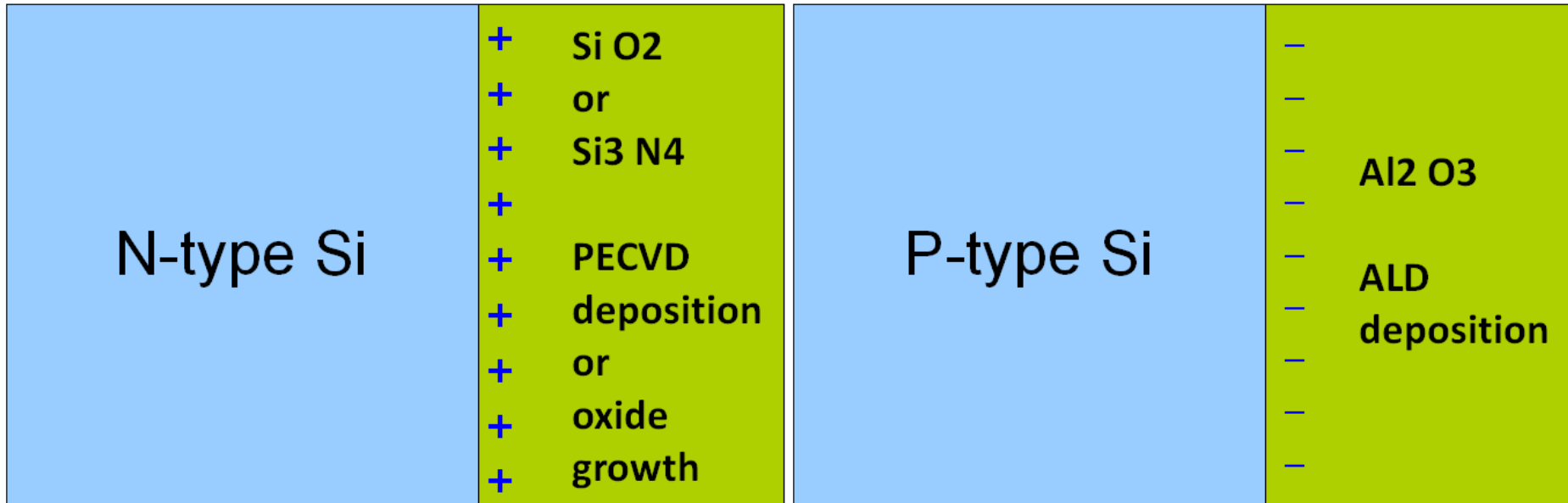
- N-type devices seem to be rad-hard. This is expected, since the properties of the sidewall after irradiation should be similar to the case of top surface on conventional sensors. (Same passivation, similar surface properties.)
- There is an issue with rad hardness on p-type devices for fluences $<10^{14}$ neq/cm².
- This has to be related to properties of dielectric (alumina) after irradiation. There is a project, lead by G. Pellegrini (CNM) to fabricate MOS-like structures with alumina to find more details about it.
- Studies of neutron-irradiated p-type 3D sensors are in progress. Preliminary data indicate no issues. This is either due to different field geometry or non-ionizing dose.

- There is an on-going effort to make an instrument with SCP treated devices!
- Alumina passivation works as inter-strip isolation method for p-type devices.



Back-Up Slides

Passivation Options



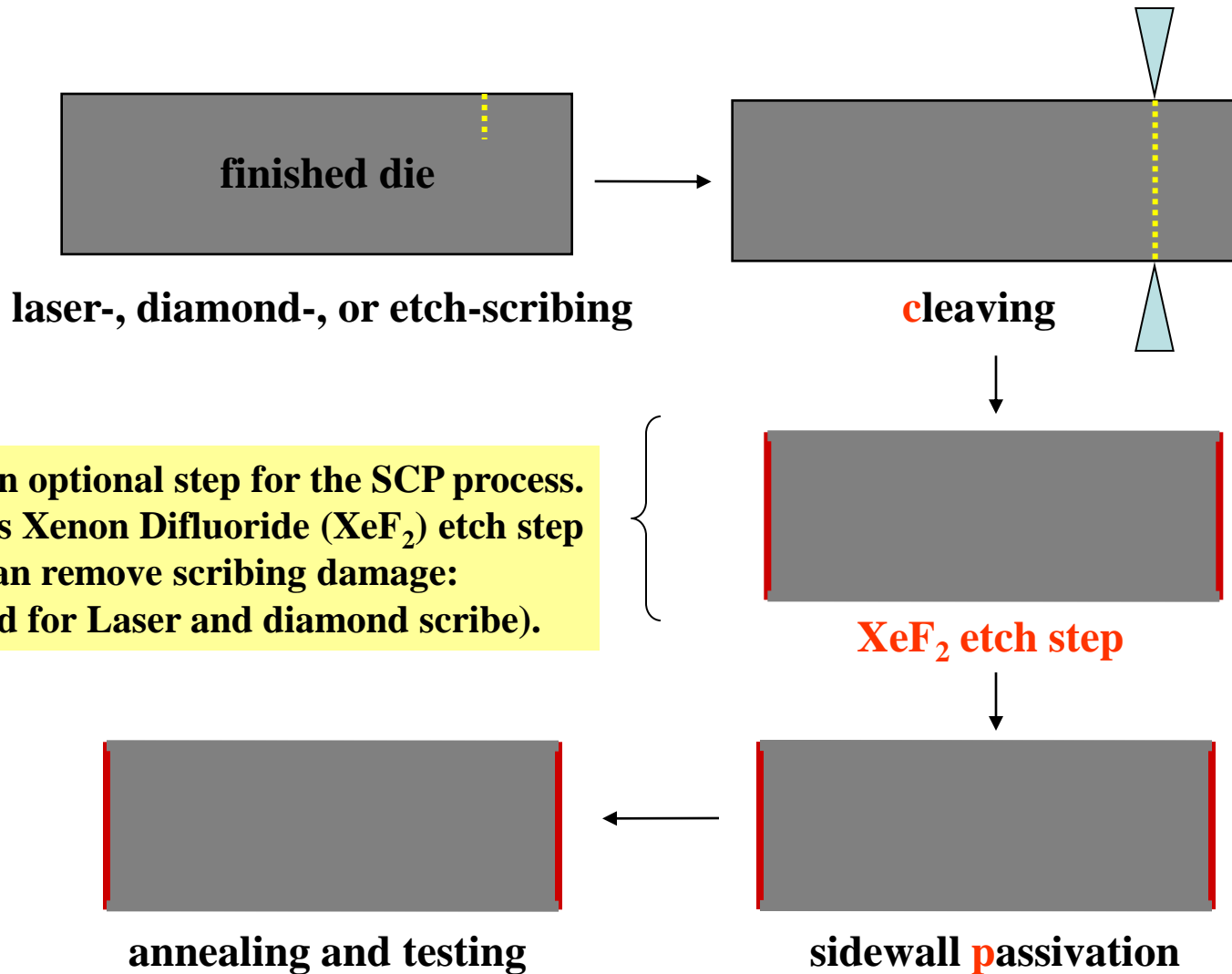
Interface charge

Interface charge

Surface passivation makes the sidewall resistive. N- and p-type devices require different technologies.

- For n-type devices one needs a passivation with *positive* interface charge. SiO₂ and Si₃N₄ layers works well.
- For p-type material a passivation with *negative* interface charge is necessary. We found that Al₂O₃ works in this case.

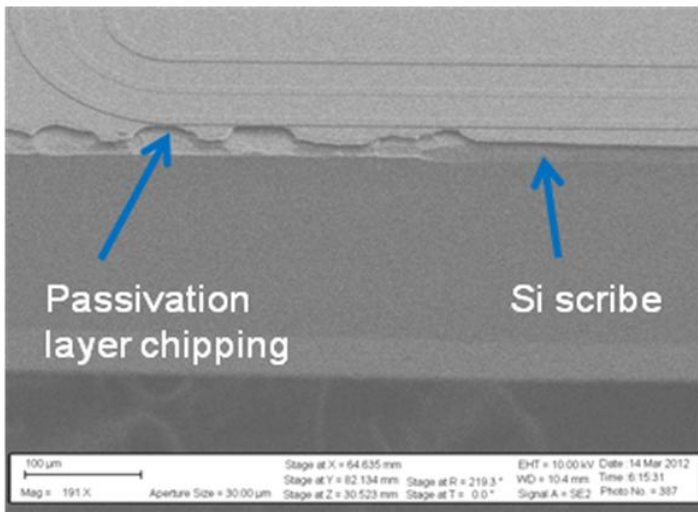
SCP Treatment (Cont)



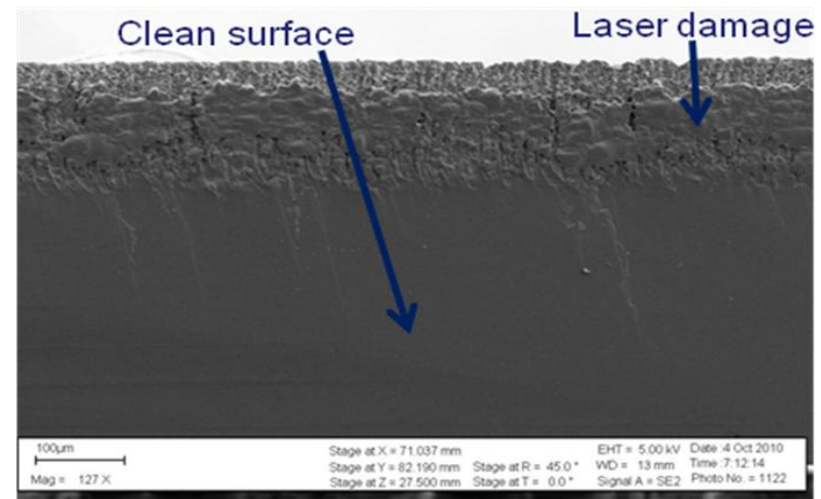
Scribing Technologies: Diamond-, Laser-, and Etch-based



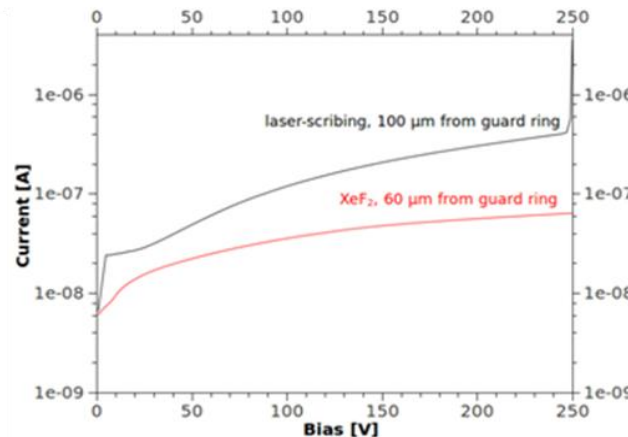
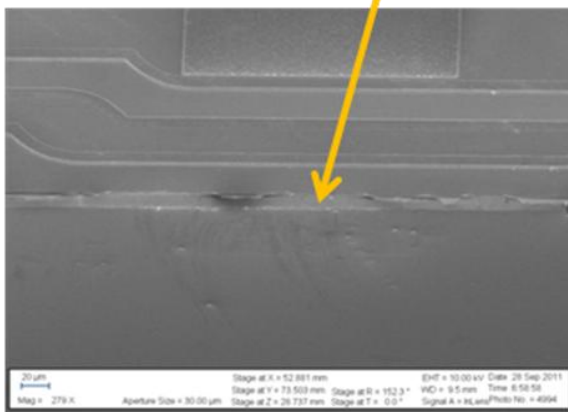
Diamond scribing



Laser scribing



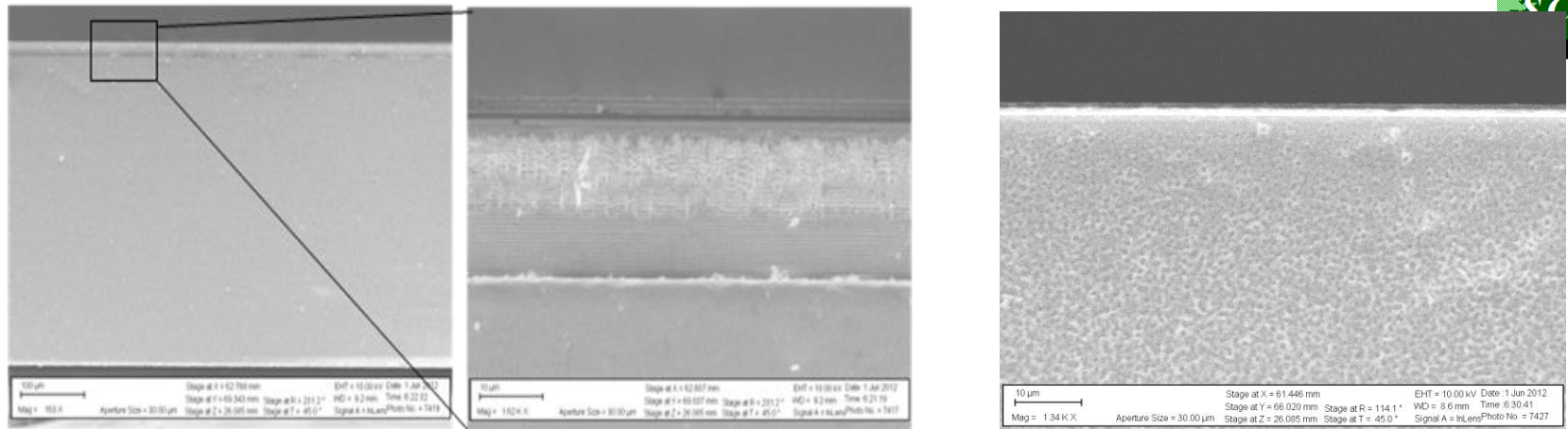
XeF₂ "scribe" with depth ~ 5 μm



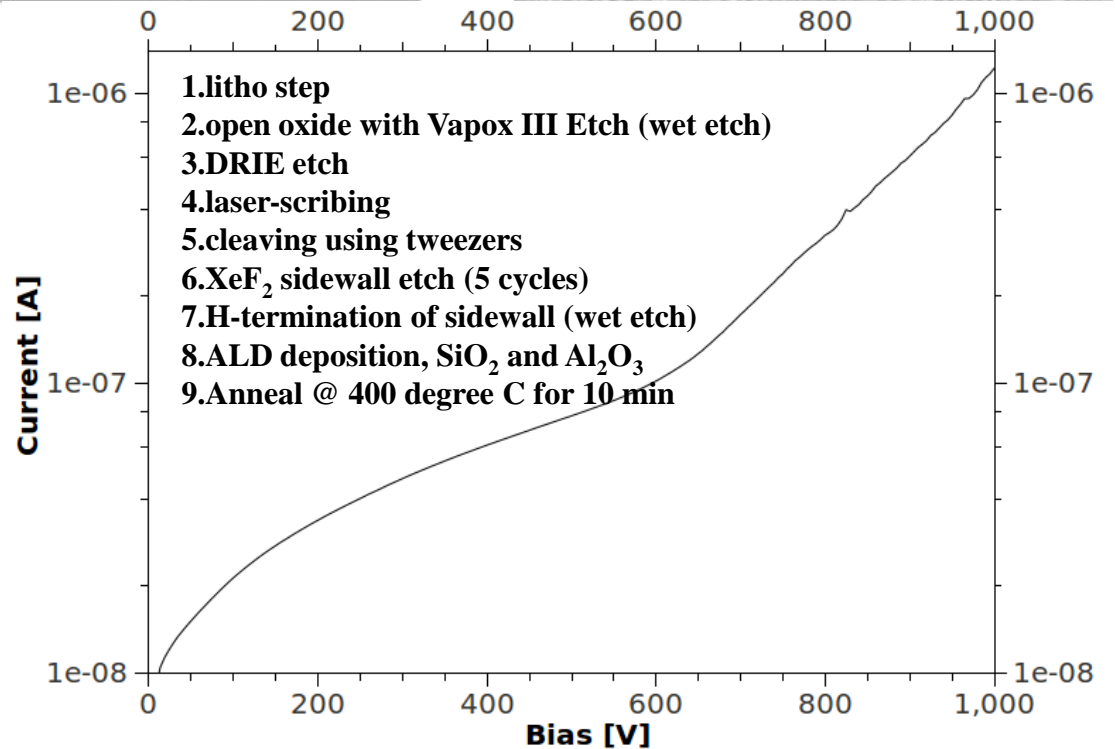
Issues:

- **Diamond scribing:** surface chipping of existing passivation (=> to do again in future runs)
- **Laser scribing:** some degree of damage due to affected region of the sidewall
- **XeF₂ etching:** cleaving by industrial machines is difficult

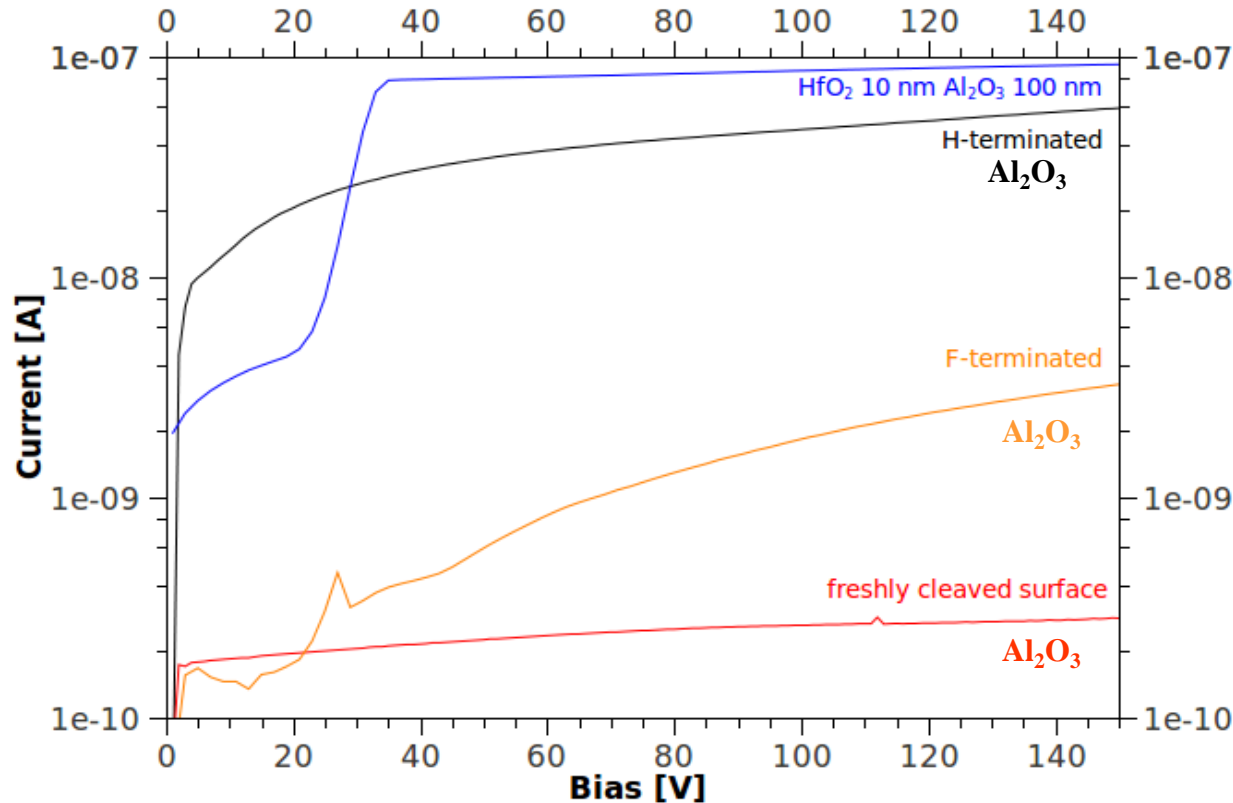
Scribing Technologies: DRIE



DRIE-based trenching as scribing has a promised of being a “universal” production solution without shortcomings of the other methods.



Effect of Surface Termination – P-Type Si



- After all the handling, we need to remove a native oxide. That is done w/ HF and leads to the “H-termination”, which can’t be passivated with alumina Al₂O₃.
- Need to covert the H-termination into F-termination which in combination with alumina ALD should work. Know they chemistry!
- The hunt for on ideal surface termination for p-type Si is still on.

Progress with Passivation (N-type Diodes)



PECVD process has been developed by industry as a wafer process => Small height of the chamber in a typical machine.

This worked well for small size samples, that could be positioned vertically, or slanted. For large sensors this is not quite applicable => replace by ALD method.

Study with HPK Fermi/GLAST diodes. The plain ALD SiO₂ is worse than the best case of PECVD Si₃N₄.

But a “nanostack” of ALD SiO₂ (10 nm) and Al₂O₃ (50 nm) works well. Parameters are from G. Dingemans et al, J. Appl. Phys. 110, 093715 (2011); doi: 10.1063/1.3658246

