Progress on the Low Resistance Strip Sensors and Slim Edges Combined RD50 Experiment

CNM (Barcelona), SCIPP (Santa Cruz), IFIC (Valencia)

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- Next steps

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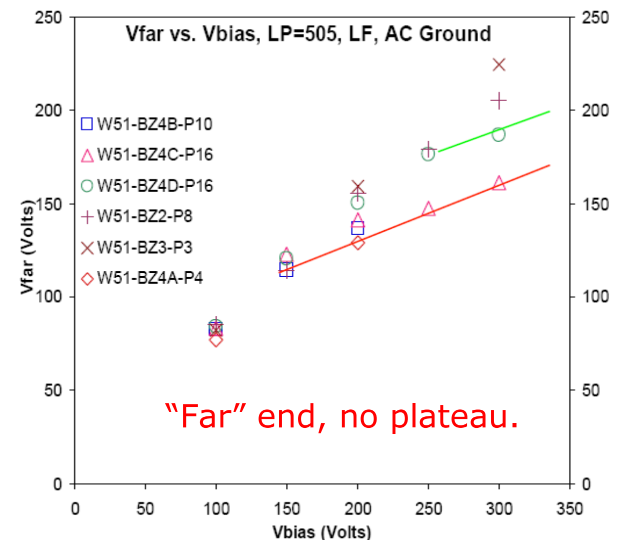
The project

Motivation

- In the scenario of a beam loss there is a large charge deposition in the sensor bulk and coupling capacitors can get damaged.
- Punch-Through Protection (PTP) structures used at strip end to develop low impedance to the bias line and evacuate the charge.
- Placement of the resistor between the implant and bias rail (“transistor effect”).
- Measurements with a large charge injected by a laser pulse showed that the strips can still be damaged.
- The ***implant resistance*** effectively isolates the “far” end of the strip from the PTP structure leading to the large voltages

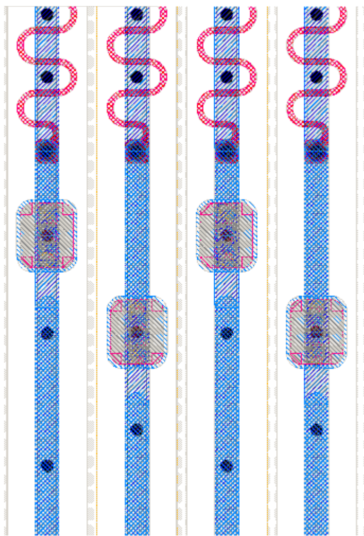


C. Betancourt, et al. “Updates on Punch-through Protection” ATLAS Upgrade week, Oxford, March 31, 2011.

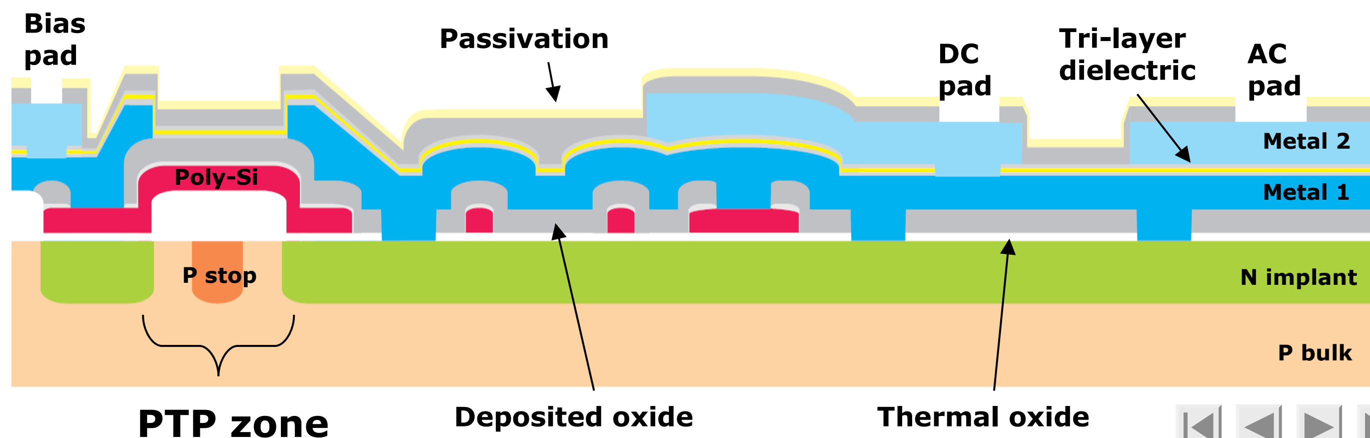
H.F.-W. Sadrozinski, et al. “Punch-through protection of SSDs”, Nuclear Instruments and Methods in Physics Research A 699, p31-35, 2013.

Proposal

- To reduce the resistance of the strips on the silicon sensor.
- Not possible to increase implant doping to significantly lower the resistance. Solid solubility limit of the dopant in silicon, besides practical technological limits (~ 1 x 10^{20} cm^{-3})
- Alternative: deposition of Aluminum on top of the implant:
  $R_{\square}(Al) \sim 0.04\ \Omega/sq \rightarrow R(Al) \sim 20\ \Omega/cm$

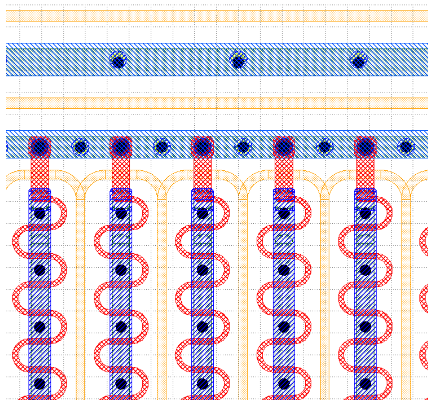


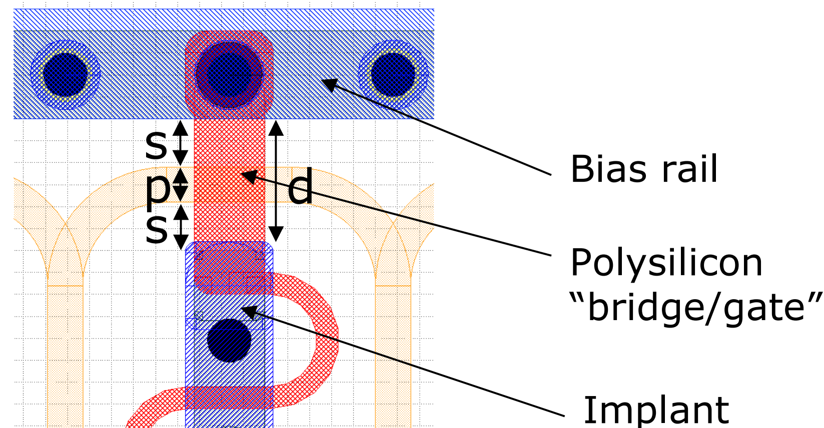
- The coupling capacitance for LowR sensors is defined by a tri-layer oxide deposited at low temperature (PECVD).



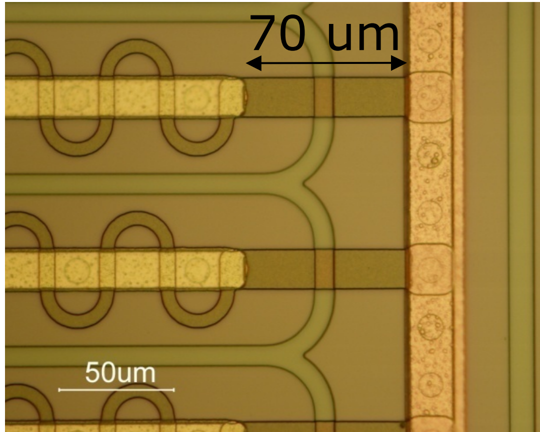
PTP designs

- Reduce implant distance to bias ring to favor punch-through effect at low voltages
  - Not tried before at CNM
  - Very dependent on surface effects (difficult to simulate)
- Poly resistor between the implant and bias rail ("transistor effect")
- Compromise between Punch-Through effect and early breakdown
- Design of experiments varying p, s → d

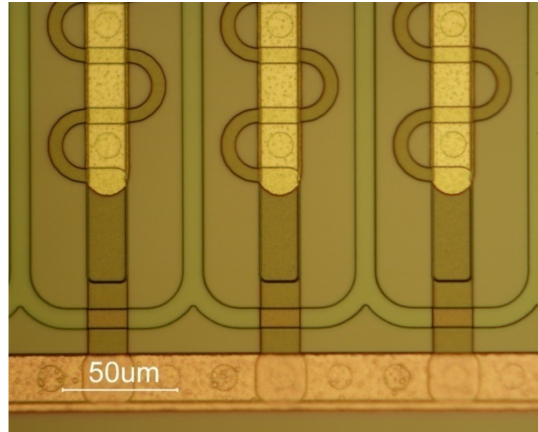




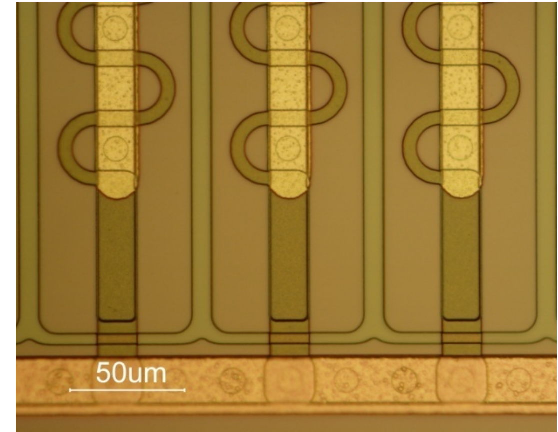
PTP designs



- d = 70 um
- p = 8 um
- s = 31 um



- d = 32 um
- p = 8 um
- s = 12 um



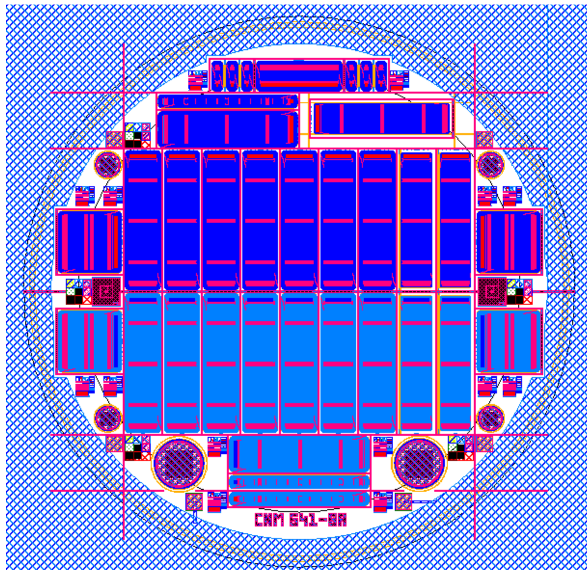
- d = 16 um
- p = 4 um
- s = 6 um

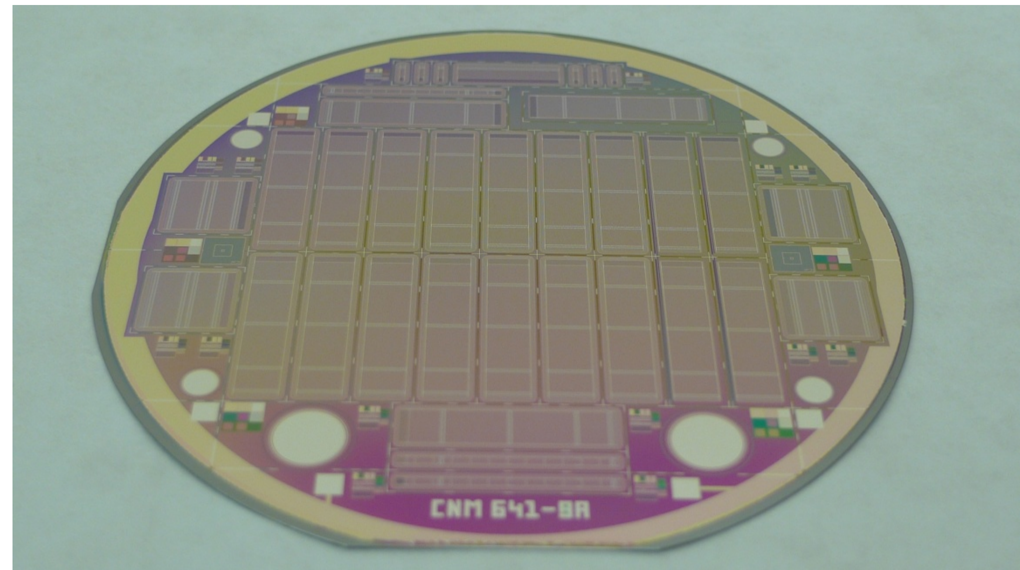
		N – P separation (um)		
		12	8	6
P-stop width (um)	8	32	24	20
	6	30	22	18
	4	28	20	16

- 9 different cases.
- ATLAS07 specifications were considered.
- One standard ATLAS07 geometry as reference.

Wafer layout

- 10 mini ATLAS-barrel-like sensors
  - ✓ 64 channels, ~2.3 mm long strips
  - ✓ Metal strip on top of the implant and connected to it to reduce R_{strip}
  - ✓ Each sensor with a different PTP geometry (with poly bridge)
- 10 extra standard sensors for reference (no metal on implant)
  - ✓ Identical to the ones above but without metal strip
- Extra test structures





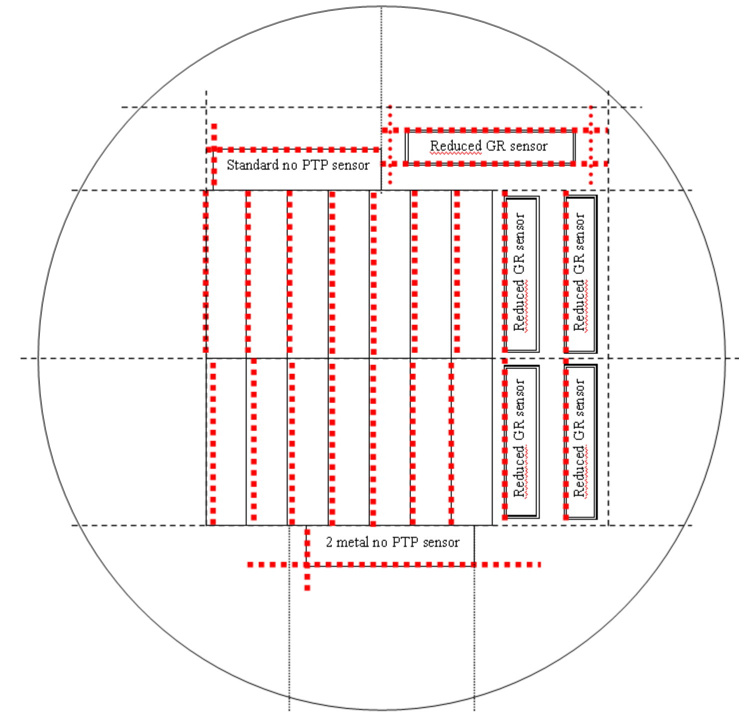
Slim edges experiment

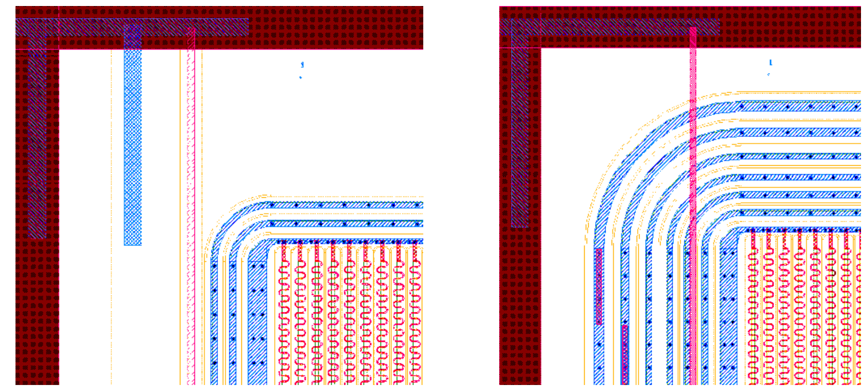
- Extra wafers in the batch for Slim Edges experiment.
- New mask designed for Aluminum removal in the back side to act as mask for DRIE.
- Si deep etch from the back.

- Trenches 30 um wide and:
  - Opt 1: 10 μm deep etch
  - Opt 2: ~200 μm deep etch
  - Opt 3: XeF_2 etch at NRL

- ALD deposition of Al_2O_3 after etching to passivate surface inside the trench.

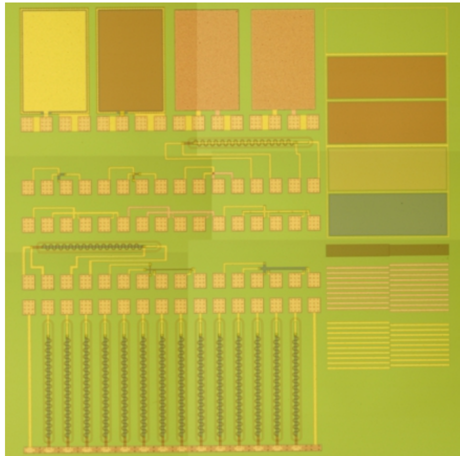
- Several trench experiments:
  - 2 guard rings sensors and trench cut close to the last guard ring
  - Cut at different guard rings
    - 2 sides cut
    - 4 sides cut





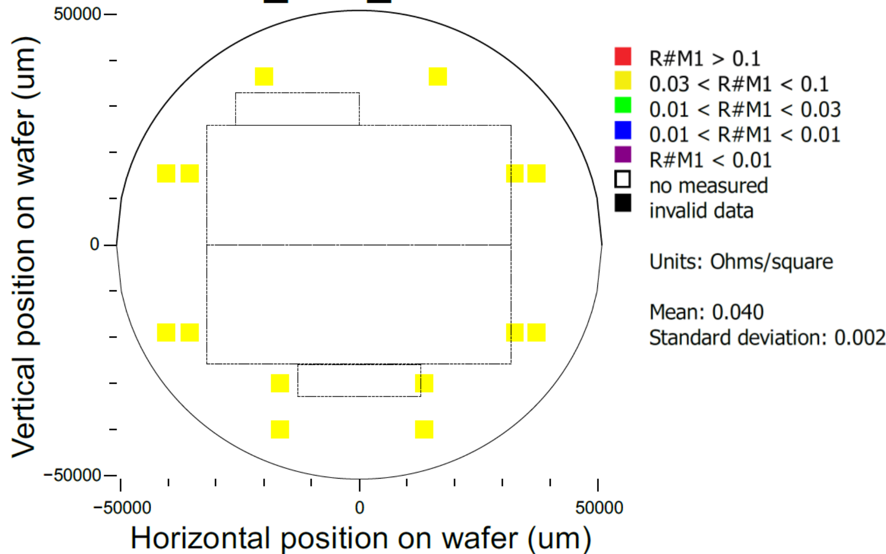
Low Resistance Strip Sensors experiment status

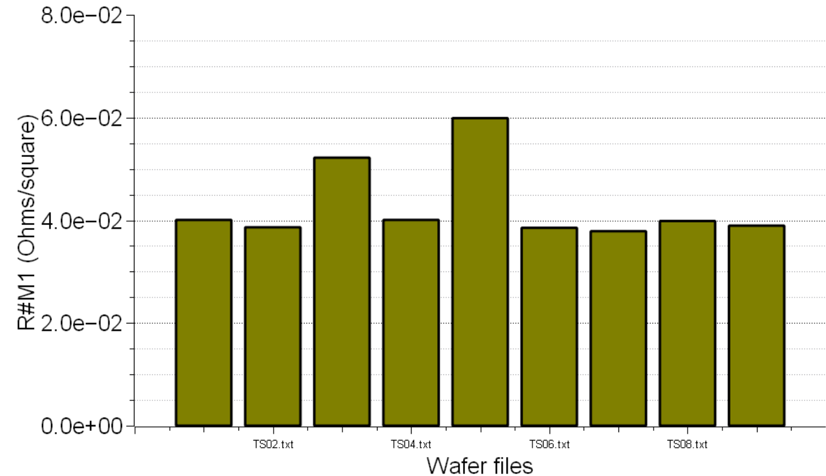
Technological measurements



- Technological test structure.
- Allows to measure:
  - Square resistance.
  - Contact resistance.
  - Bias resistors.
  - Capacitors.
- Data show low parameter variations.
  - Bias resistors higher than expected.

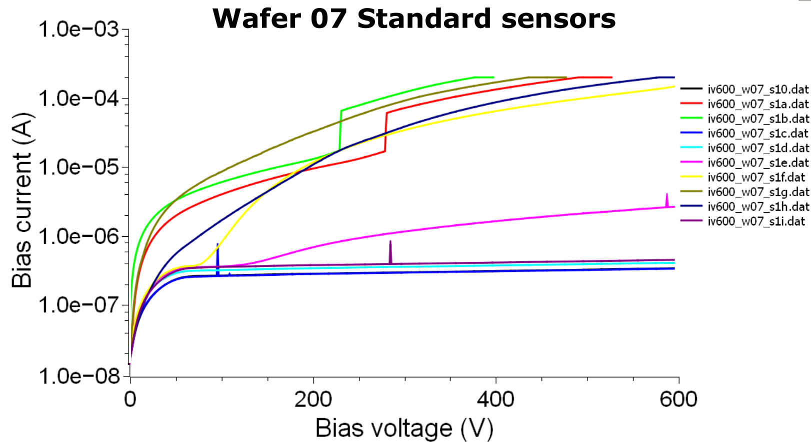
	Mean	Standard deviation
$C_{coupling\ standard}$ (pF/cm)	53,7	0,1
$C_{coupling\ LowR}$ (pF/cm)	28,8	4,2
$R_{Metal\ 1}$ (Ω/cm)	22,6	7,9
R_{Metal1_N+} (Ω/cm)	18,4	2,3
$R_{Metal\ 2}$ (Ω/cm)	14,1	3,2
$R_{implant\ N+}$ (KΩ/cm)	14,2	0,07
R_{Bias} (MΩ)	2,94	0,52

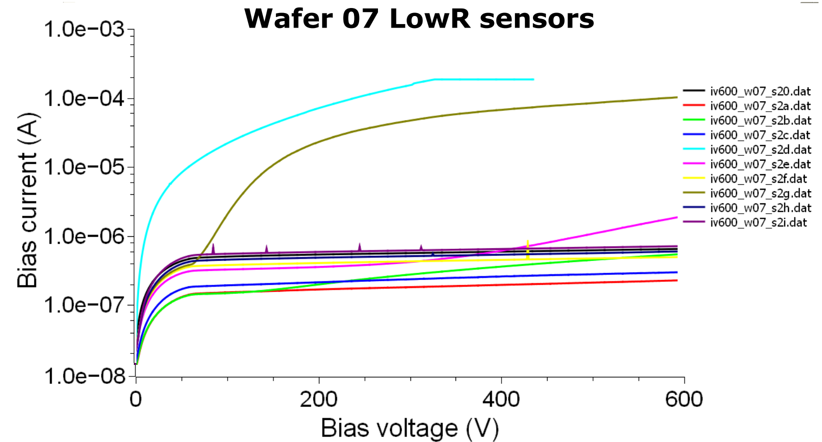




Sensor measurements

- For IV measurements, sensors were biased from 0 V to 600 V in 1 V steps. Current compliance equal to 200 uA was set.
- Both standard and LowR sensor show similar behavior.

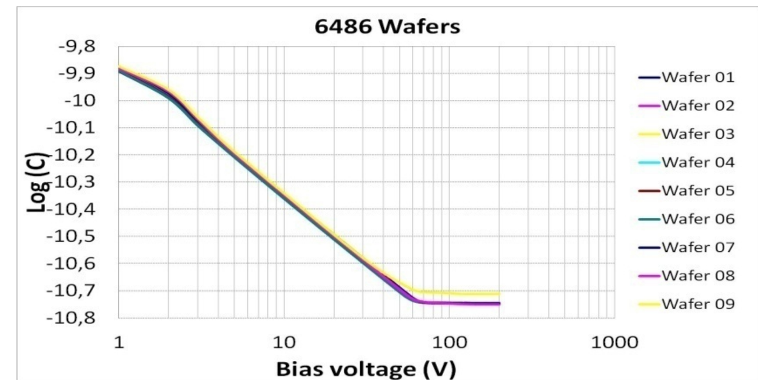




- For CV measurements, pad diodes placed on the wafer were biased from 0 V to 200 V in 1 V steps.
- A probe contacted to the active area and connected to a LCR meter (500 mV @ 10 KHz) to obtain the capacitance.

V_{FD} = 61,5 V ± 2 V

- Two wafers have been already cut and sent to Santa Cruz.

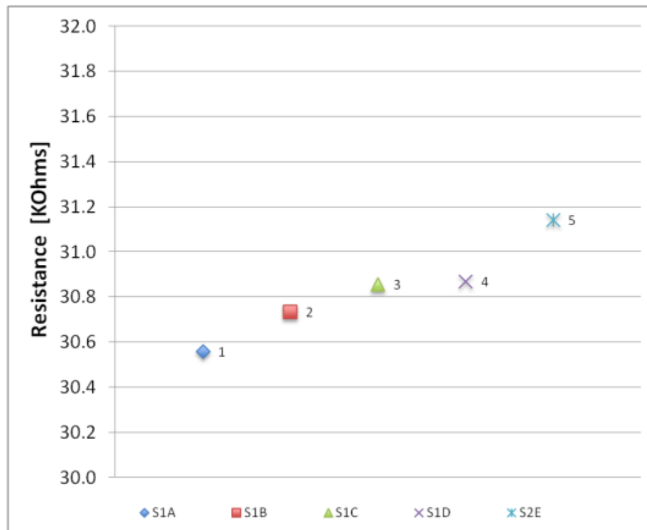


Santa Cruz measurements: Strip resistance

- Low resistance chip biased at 100 volts
- Probe set to ground on dc pad
- DC sweep with 2 mV step from -20mV to 20mV

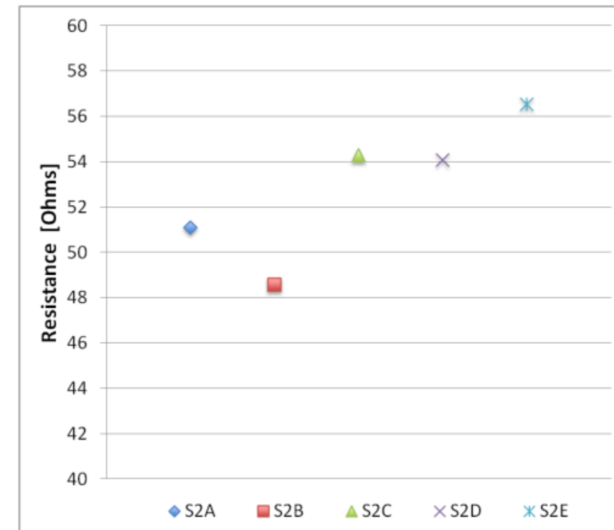
- Resistances of standard sensors

  Average resistance is 30.8 KOhm, or 10 KOhm / cm.
  ATLAS07 (HPK) devices had 15 KOhm/cm.



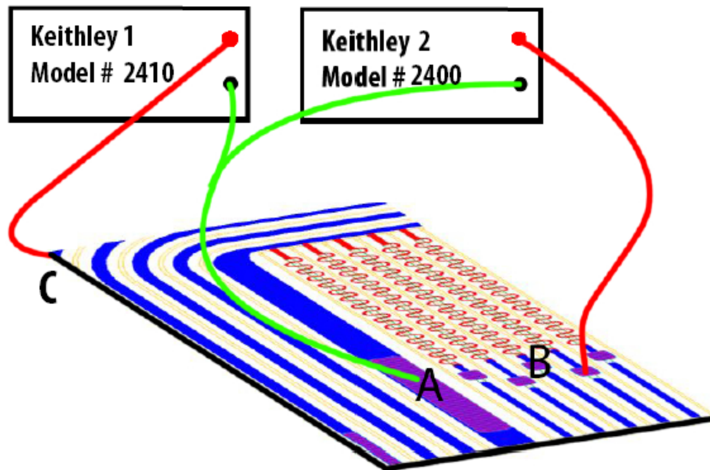
- Resistances of LowR sensors

  Low resistance chip biased at 100 volts
  Average resistance is 52.9 Ohm, or 17 Ohm / cm.



Santa Cruz measurements: PTP setup

- Equipment setup



- 1. Keithley 1 biased the sensor by applying a potential difference to the sensor backplane (C) which was grounded using the bias ring (A).
- Keithley 2 executed a DC sweep by applying a potential difference to the DC Pad (B) which is also grounded by the bias ring (A).

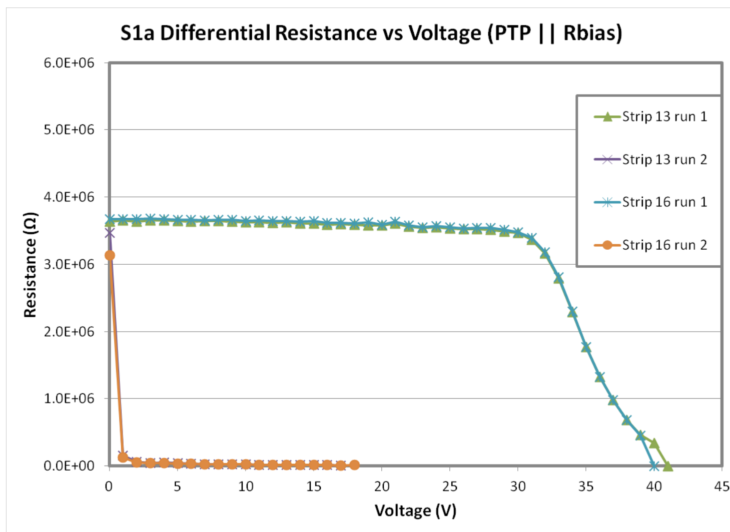
Testing properties:

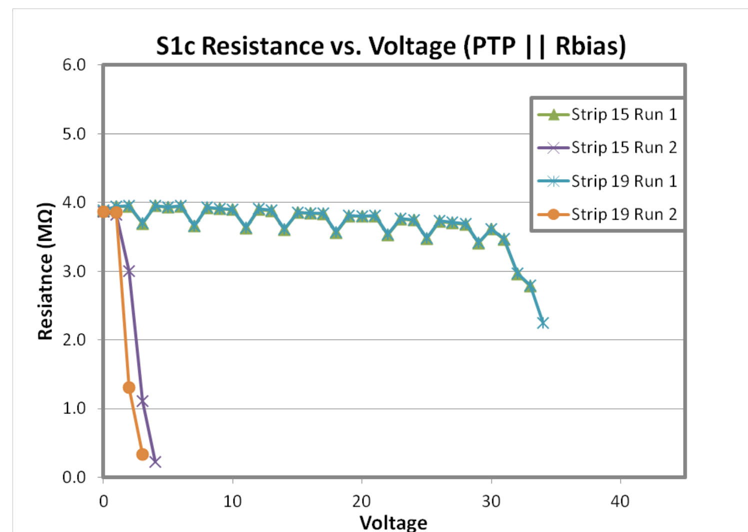
- Bias voltage supplied by Keithley 1: was -200 V. Current compliance was set to 10 uA.
- The DC sweep ranged from 0 to -40 V in 1 volt steps with a 1 second delay. The current compliance was set to 1 mA.
- Observed variables: I_{PTP} and V_{PTP} from Keithley
- The PTP structure resistance is calculated by $R_{PTP} = \Delta V/\Delta I$

Santa Cruz measurements: PTP results

- S1a (16 um PTP distance) was chosen for the first test.
- The 1st measurement has some scatter, but 2nd and 3rd strips are very consistent, with the transition voltage of about 35 V. In all 3 cases the 2nd run had vastly different transition voltage.

- S1c (20 um PTP distance) chosen s1c for the 2nd test.
- This test is also different in how the voltage was removed after the scan. During the 1st scan, we cut-off the voltage supply abruptly (a standard procedure). Thinking that this might cause problems, we removed the voltage gradually after the scan, at the rate of 1V/sec.

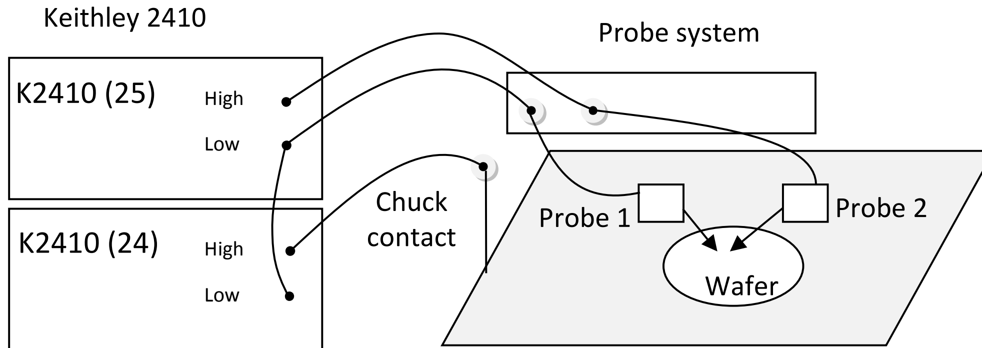


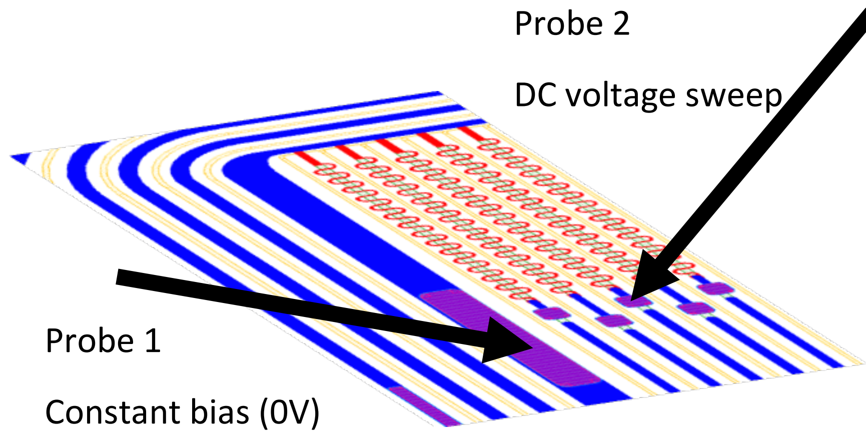


- The transition voltage indicated in the 2nd test is at about the same value of 35 V. This indicates that the transition is due to oxide breaking rather than the PTP turn-on.

PTP measurements (CNM)

- Equipment setup





- Room temperature ≈ 22 ºC
- N_2 flow over wafer to remove moisture.

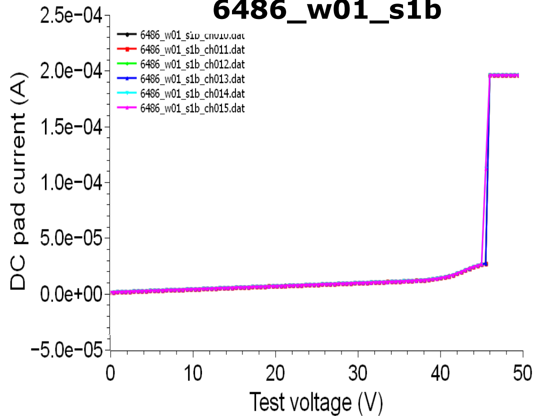
- Constant bias:
  Vchuck = -100 V
  Vbias = 0 V
  Measure bias leakage current (200 uA compliance)

- DC voltage sweep:
  Vdc = 0 V to 50 V
  0,5 V steps
  Measure leakage current at DC pad (200 uA compliance)

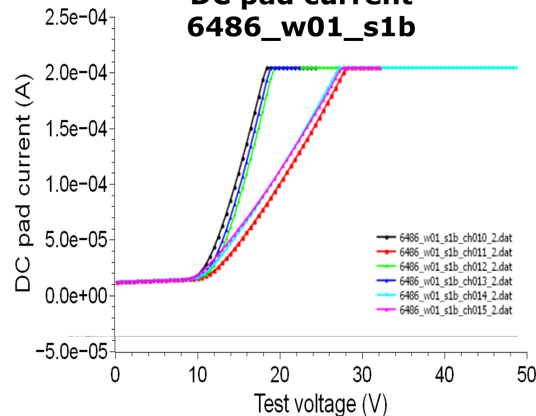
- Vtest = Vdc-Vbias
  Reff= ΔVtest/ΔIdc
  |Idc| ≈| Ibias|

PTP measurements: Standard sensors

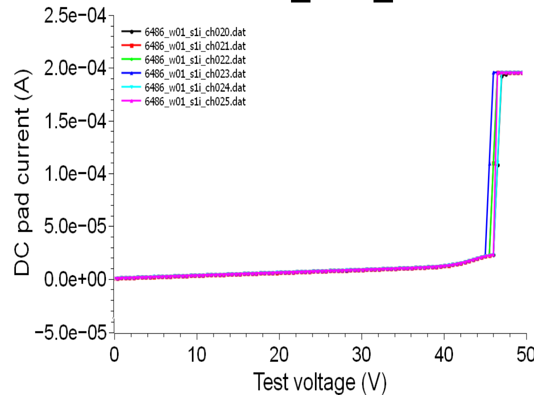
d18_p06



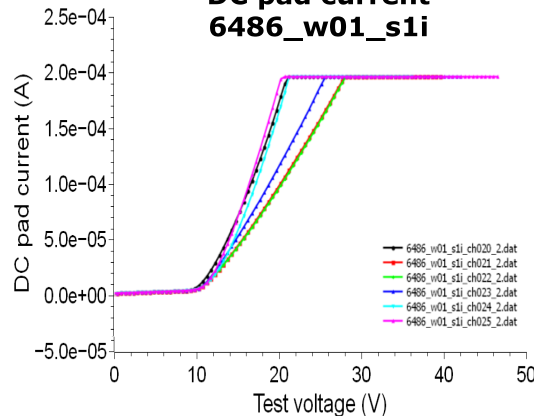
Second measurement



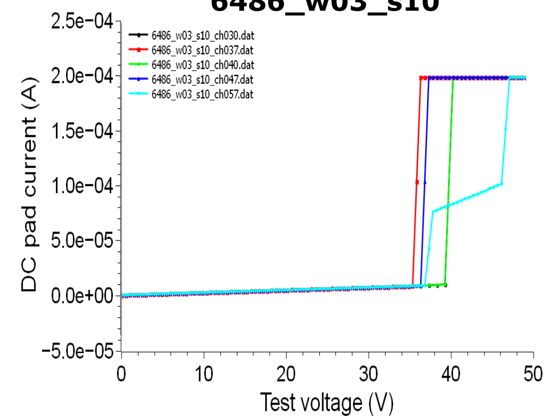
d32_p08



Second measurement



d70_p08

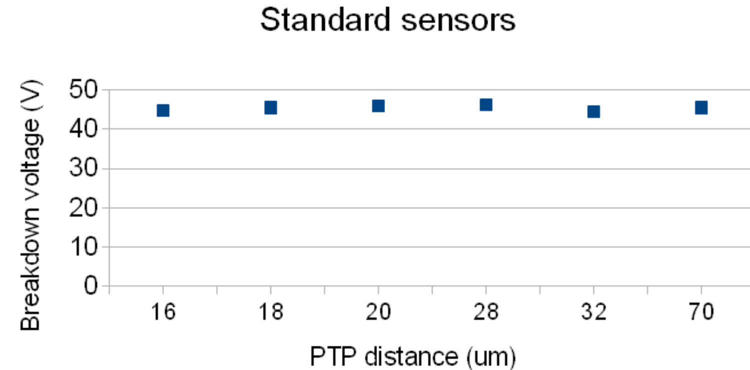


- Breakdown is observed systematically.
- Second (and more) measurement shows it is a non reversible effect.

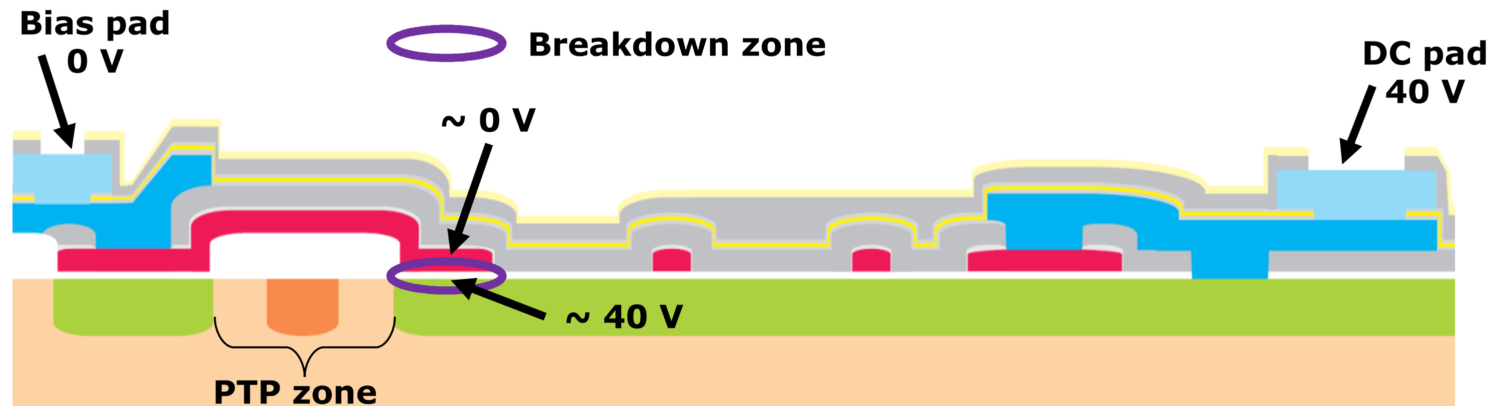
PTP measurements: Standard sensors

- High currents are not generated in the PTP zone, but in the thin thermal grown oxide.

- Breakdown occurs between strip implant and Polysilicion bias resistor.
- Breakdown is independent of PTP structure geometry, but dependent of oxide thickness.



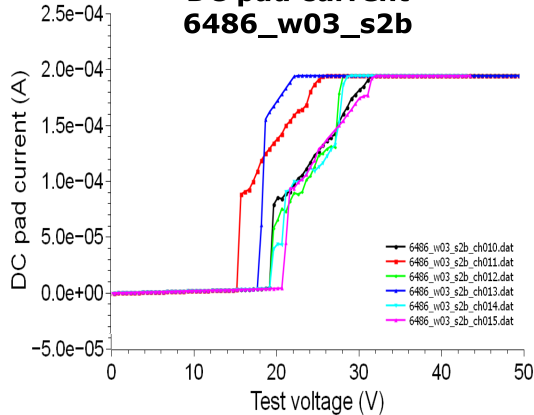
- V_B = 42,6 ± 4 V



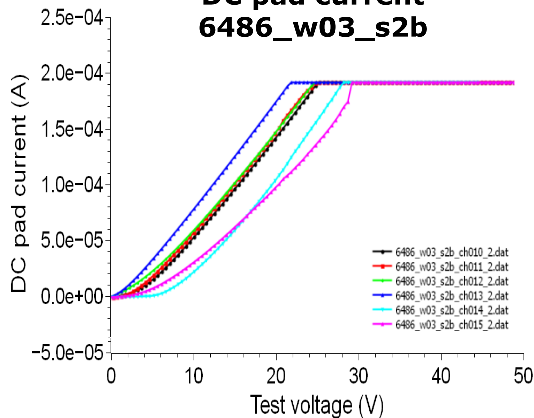
- Breakdown occurs around 42 V, which is the value of V_B for the thermal oxide of ~40 nm thickness.

PTP measurements: LowR sensors

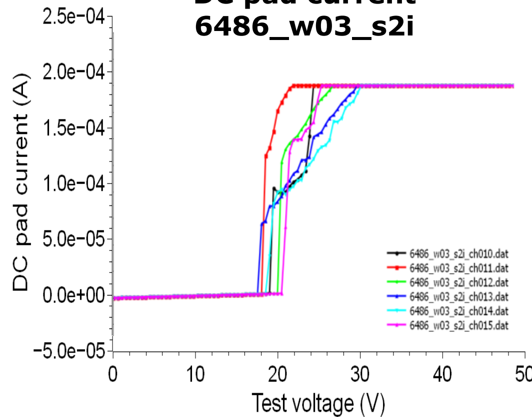
d18_p06



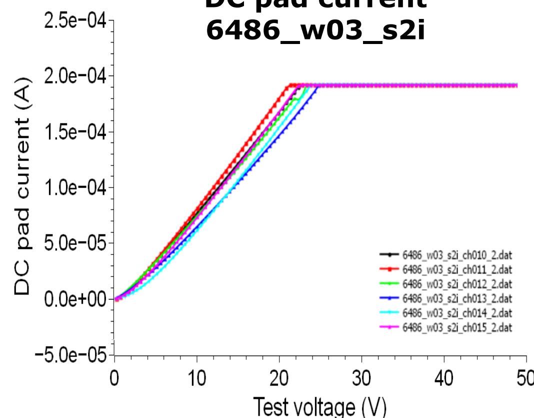
Second measurement



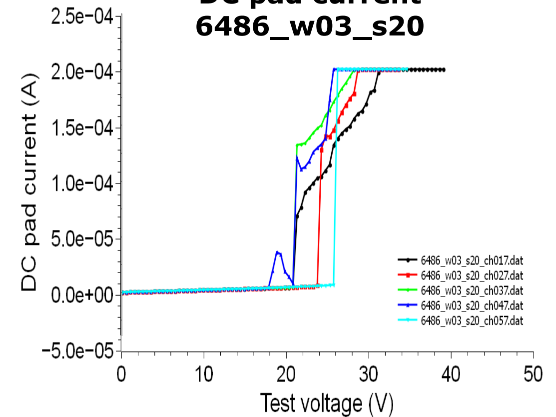
d32_p08



Second measurement



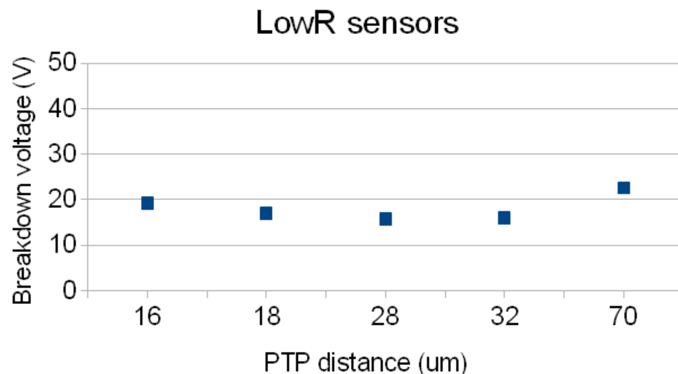
d70_p08

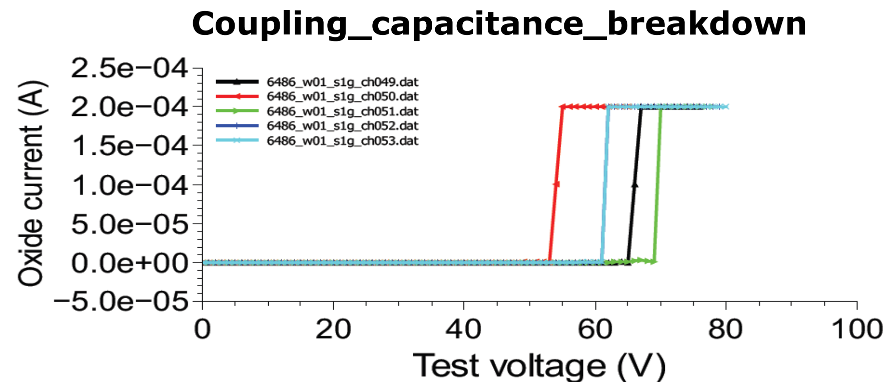


- Similar behavior to standard sensors
- Breakdown at different voltage but still independent of PTP structure geometry.
- Breakdown does not happen in the same zone.

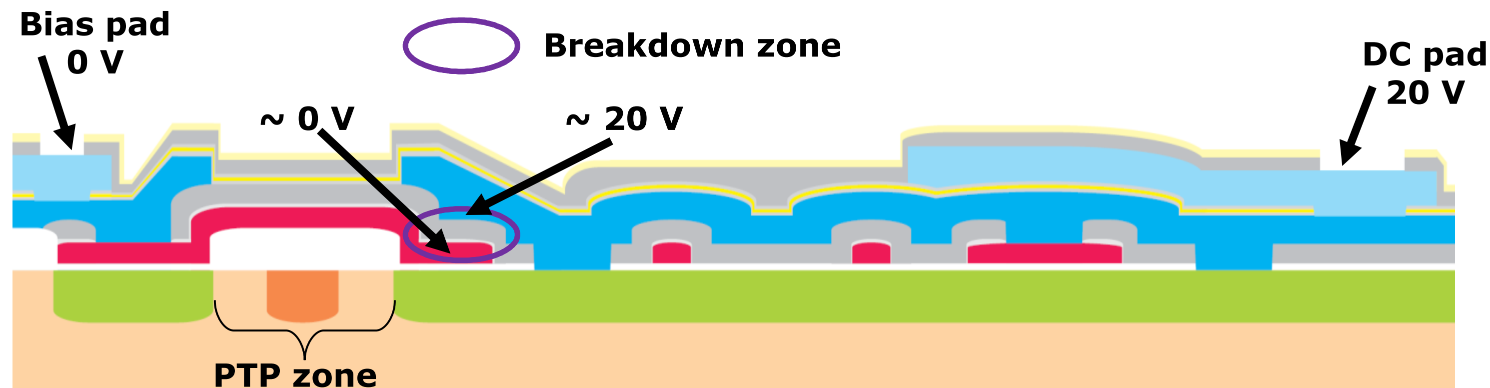
PTP measurements: Low R sensors

- Breakdown occurs between the Polysilicion bias resistor and the metal over it.
- Oxide composed by a thermal oxide (~20 nm) and a deposited oxide (~100 nm).





- $V_B = 20 \pm 3$ V
- $V_B = 62 \pm 6$ V ~ $V_{B_oxide_40nm} + V_{B_oxide_20nm}$



- Breakdown occurs around 20 V. Although the deposited oxide thickness is ~100 nm, pinholes reduce V_B.

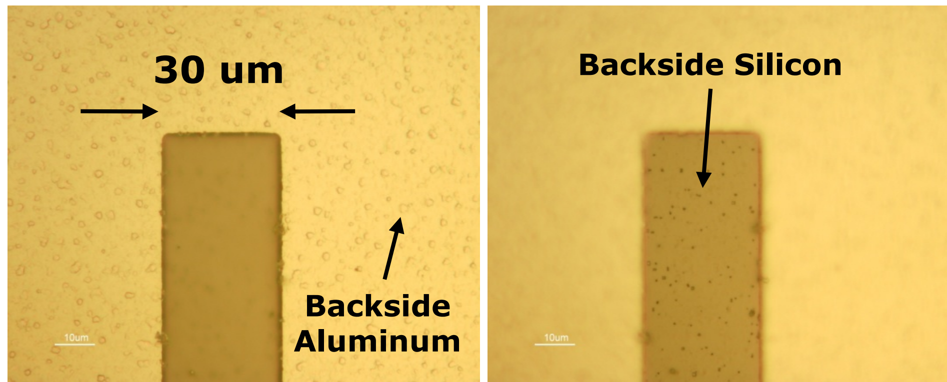
Next steps: Low R strip sensors

- Changes are needed in order to solve the oxide breakdown problem.
- A thicker thermal oxide will be grown in order to increase coupling capacitance breakdown up to 100 V.
- A multi-layer deposited oxide will be placed over Polysilicon to eliminate pinholes.
- Metal masks designs to be updated in order to reduce the risk of damage in deposited oxides when metals are etched.
  - Remove metal over Polysilicon is being considered for some cases.
- A new fabrication process will start soon.
- In the meantime, fabricated sensors can still be used to perform other measurements: signal shape comparison, interstrip isolation comparison, laser-based charge injection for the non-double metal sensors, slim-edges experiment ...

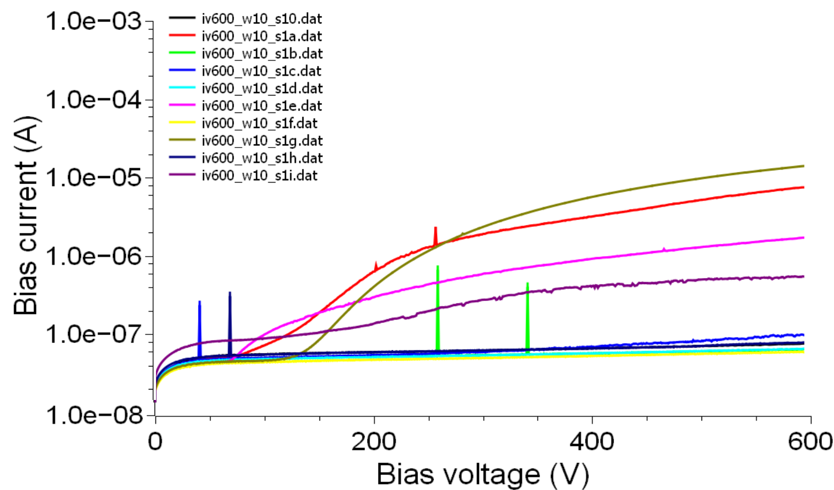
Slim Edges experiment status

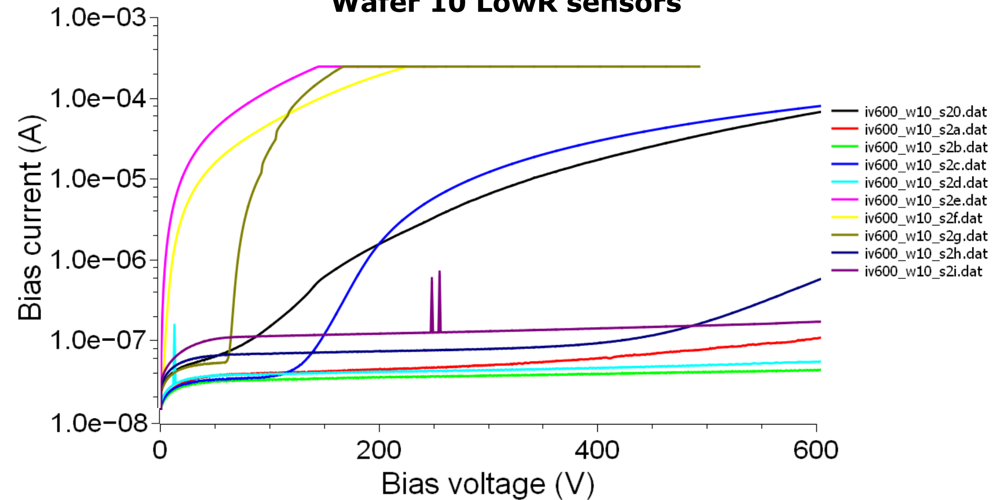
Slim-edges sensor measurements

- Case 1: Back Aluminum etch



- Before trenches can be done, 30 um wide backside Al paths must be etched.
- Process was completed without incidents.
- One wafer was taken from clean room to perform measurements.
- Sensor measurements are similar to non-etched wafers.
  - Wafer sent to NRL

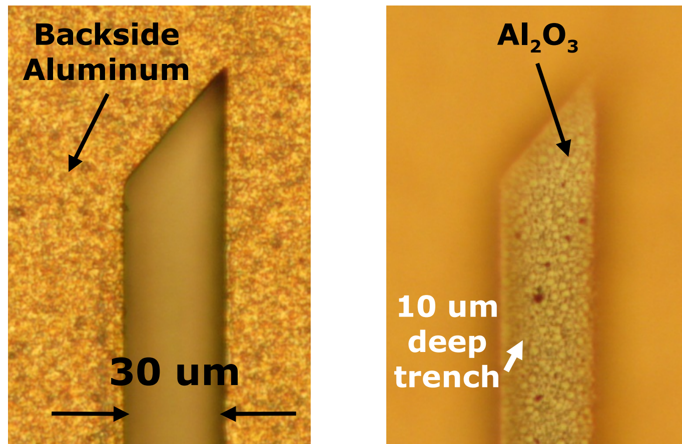




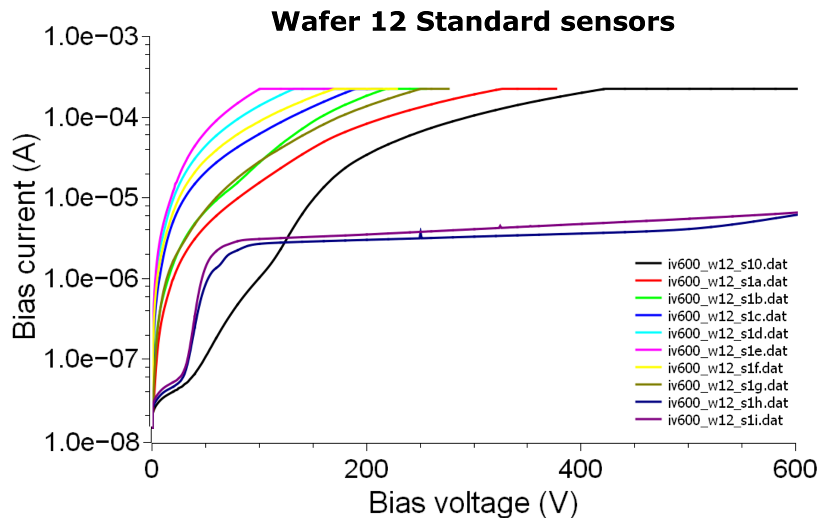
- No difference seen on sensors with etched Al

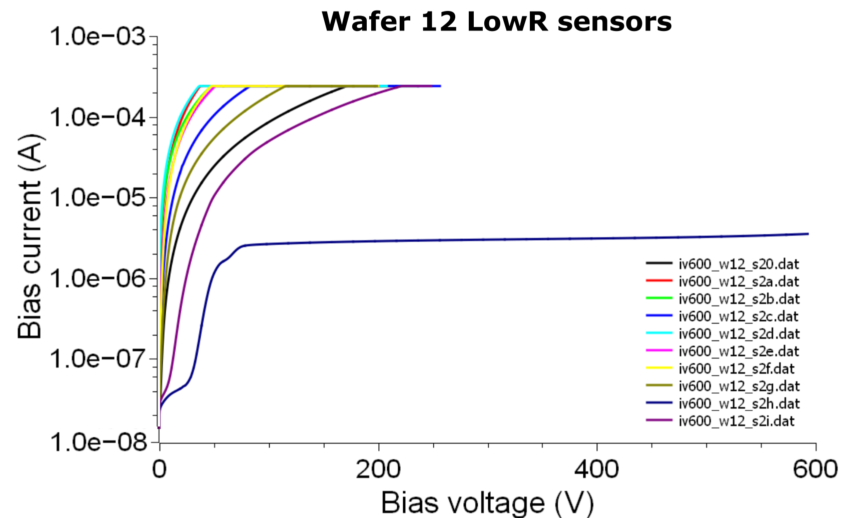
Slim-edges sensor measurements

- Case 2: 10 um deep trench



- After back Al was etched, 10 um deep trenches were etched in Silicon.
- 50 nm thick Alumina deposited after trenches were done. And later removed from surface but kept inside trenches.
- One wafer to perform measurements.
- Sensor current leakage is generally worse to non-etched wafers.
- No correlation between trench distances to active area and bias sensor current.

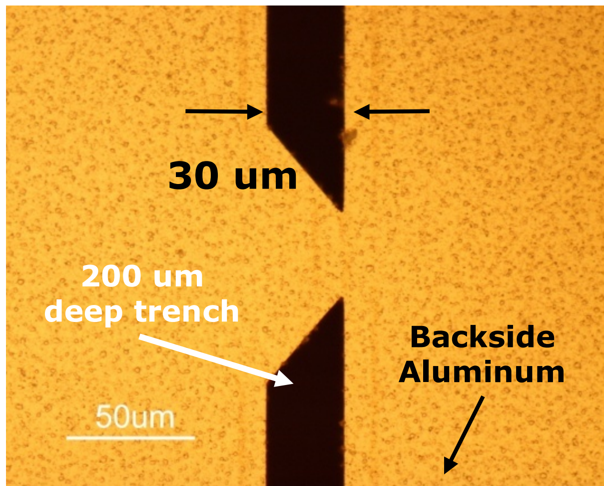




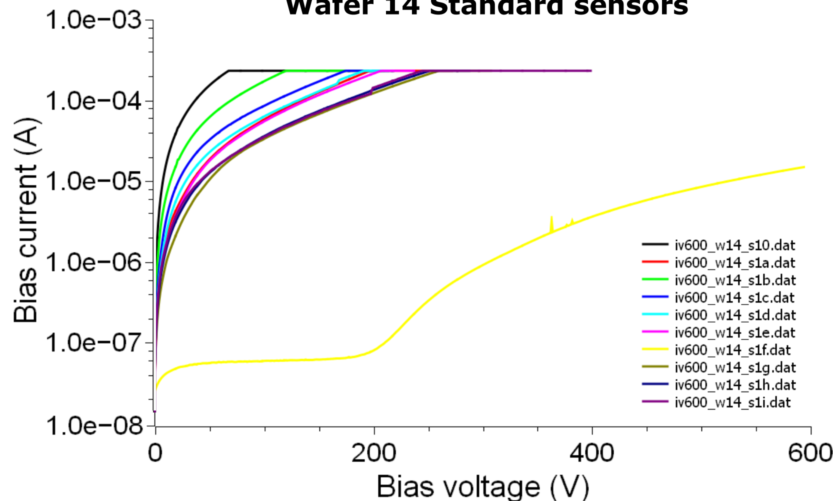
- Sensors with trenches not under guard rings show best performance

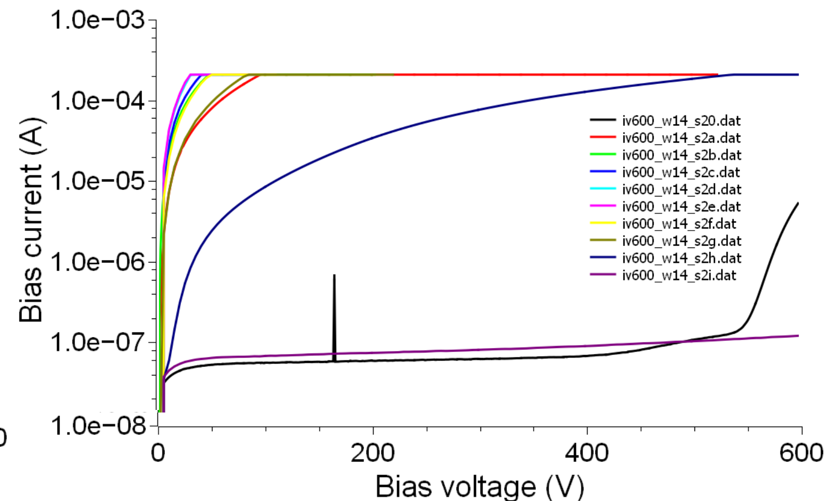
Slim-edges sensor measurements

- 200 um deep trench



- After back Al was etched, 200 um deep trenches were etched in Silicon.
- 50 nm thick Alumina deposited after trenches were done. And later removed from surface but kept inside the trenches.
- One wafer measured. Sensor current leakage is generally worse to non-etched wafers.
- No correlation between trench distances to active area and bias sensor current.
- More wafers need to be fabricated and tested.





Next steps: Slim Edges

- Cleaving test to be performed.
  - ✓ SCIPP/NRL 10 um deep trench wafer
  - ✓ CNM 200 um deep trench wafer

- Measure IV for sensors after cleaving.

- CNM will fabricate more wafers with deep trenches in order to understand high sensors current.

- Irradiations
  - Post irradiation measurements.

Conclusions

- First fabrication batch already finalized and wafers/sensors have been distributed among CNM, SCIPP and NRL.
- Technological, sensor IV, CV, PTP and Rstrip measurements performed.
- Process problem identified which reduces PTP breakdown voltage.
- CNM and SCIPP measurements show similar results.
- Punch-through protection structure has not been tested yet due to oxide breakdown.
- Fabrication and mask design changes have been implemented to solve the issues and a new batch of sensors with updated design and technology will be fabricated.
- Before next batch is fabricated, it is possible to use existing devices in wafers, such as baby sensors, to perform other measurements.

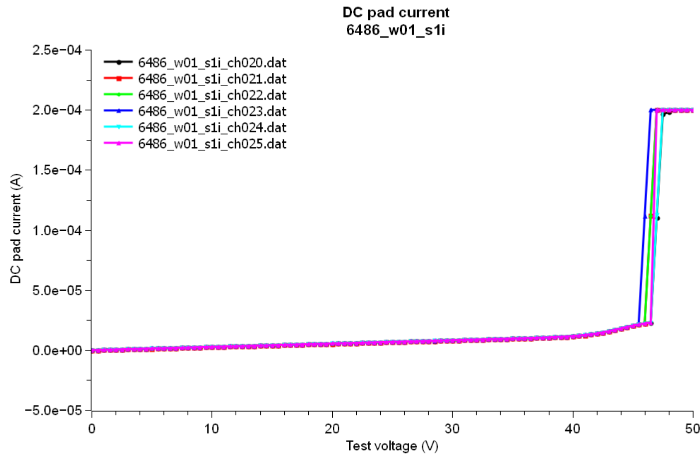
Thanks for your attention

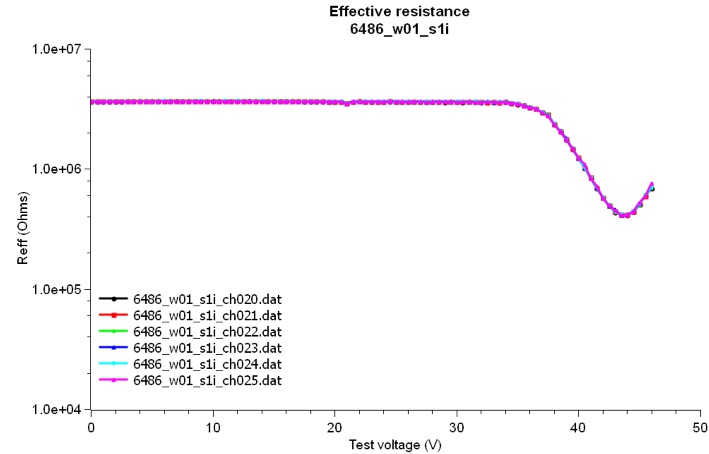
CNM 641-8A

Extra slides

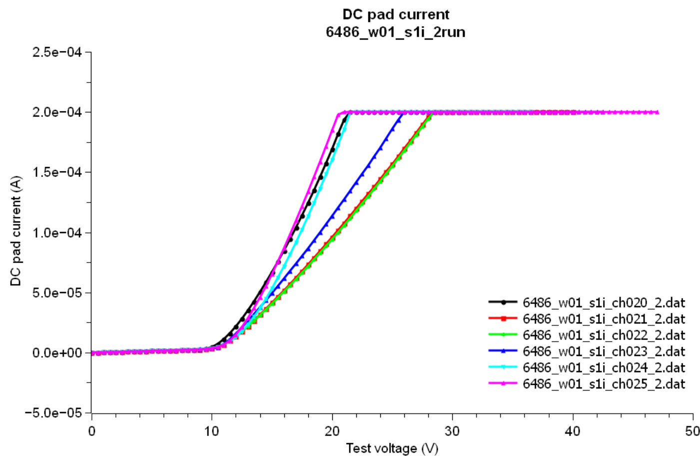
PTP measurements

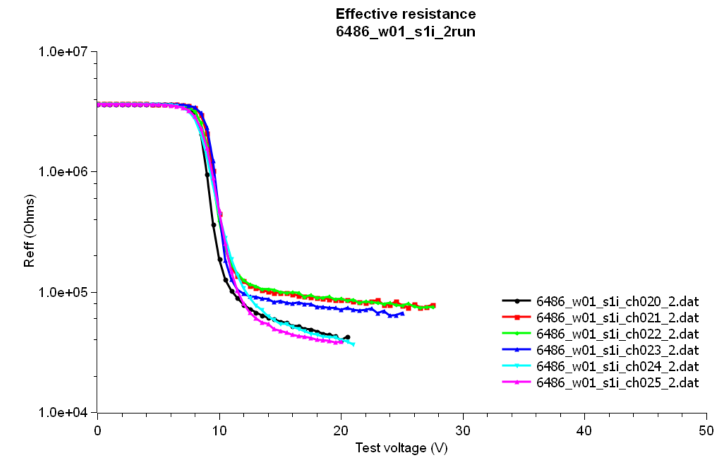
- 1 metal sensor: **d32_p08**





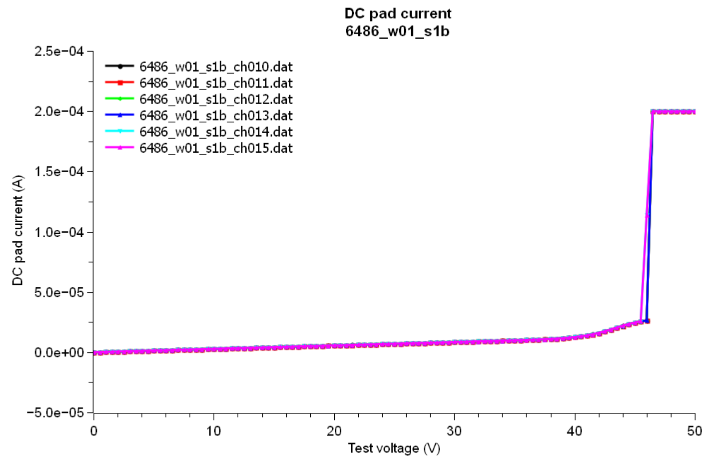
- Second measurement

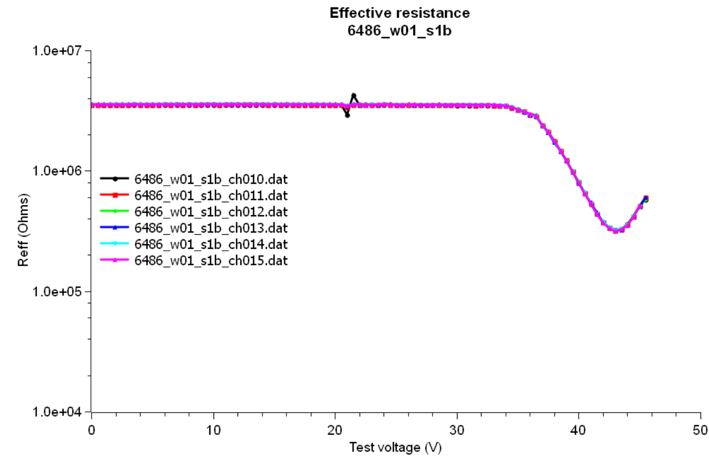




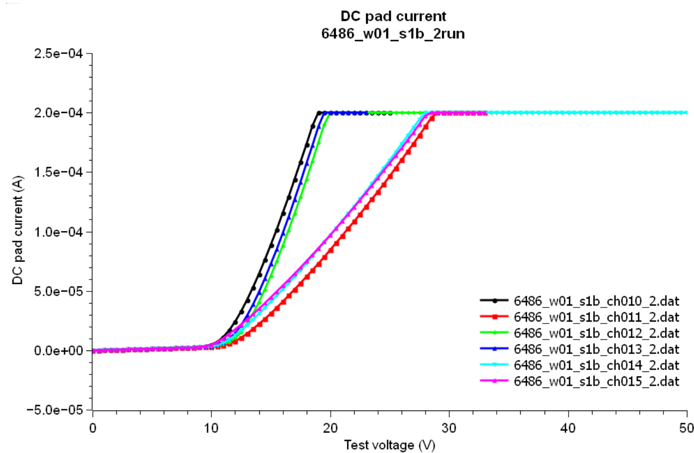
PTP measurements

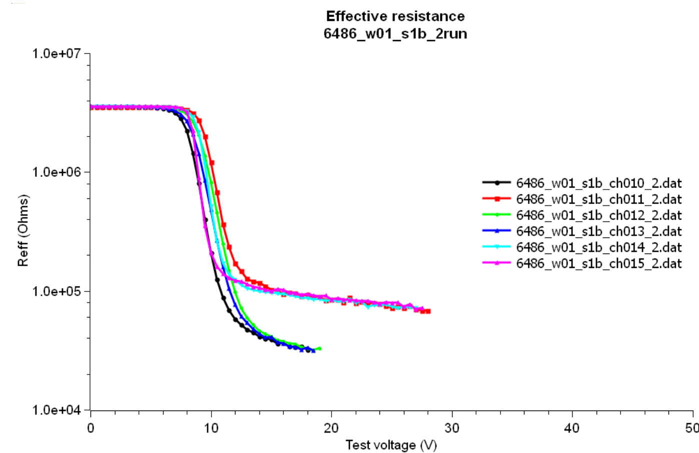
- 1 metal sensor: **d18_p06**





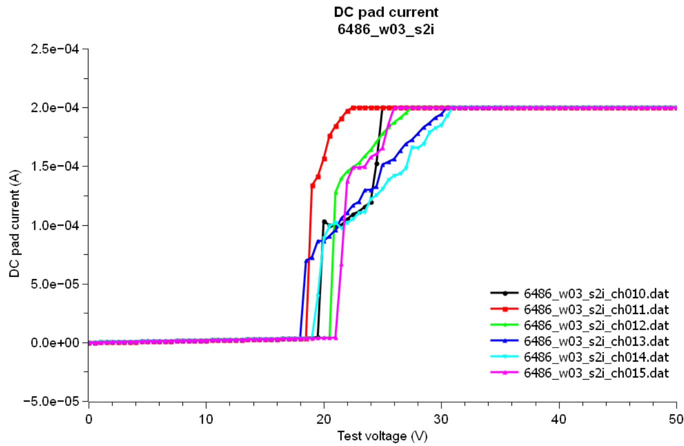
- Second measurement

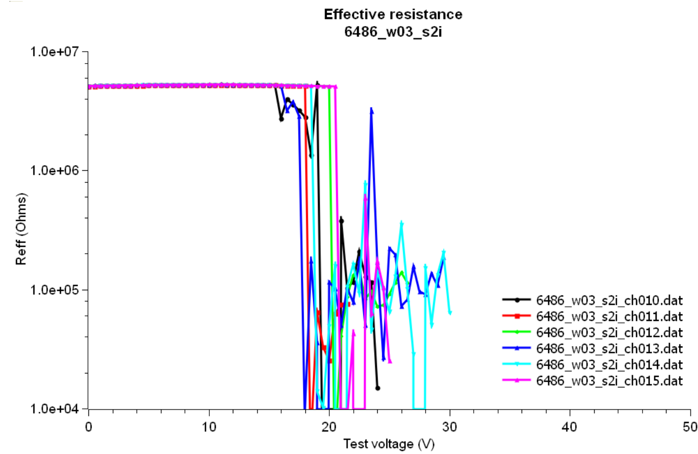




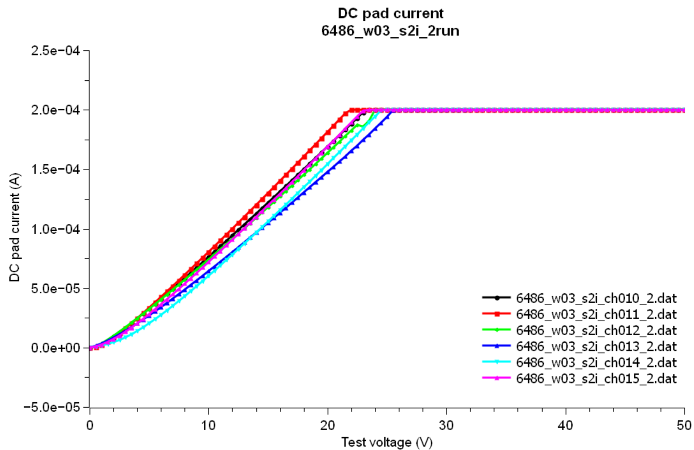
PTP measurements

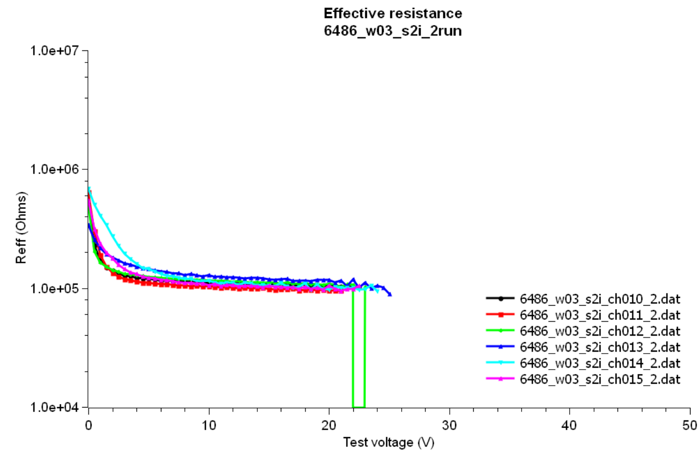
- 2 metals sensor: **d32_p08**





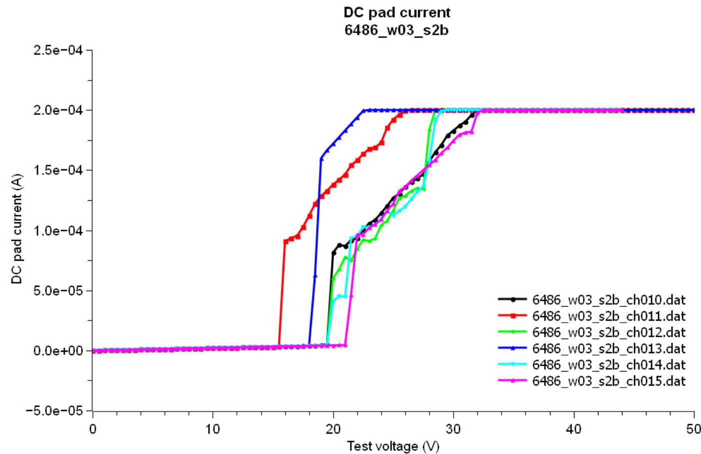
- Second measurement

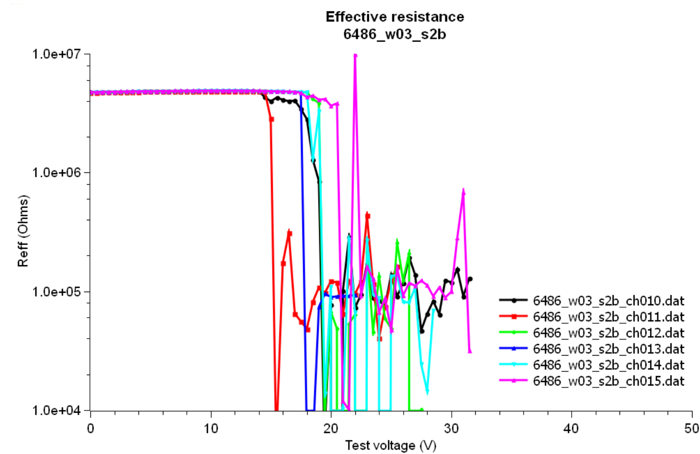




PTP measurements

- 2 metals sensor: **d18_p06**





- Second measurement