Contribution ID: **9** Type: **not specified**

TDC Design and Test Lab (Training Session)

Friday 24 May 2013 14:00 (3 hours)

The previous module will be completed by an hands-on laboratory session in which the students will design a small TDC and implement it on the provided FPGA platform. The Xilinx design environment will be utilized for this task, and the resulting configuration file will be tested on an FPGA board.

Presenters: Mr VEERAPPAN, C.; Dr REGAZZONI, Francesco

Session Classification: TDC Design and Test Lab (Training Session)