THE NEW BLM SYSTEM FOR THE INJECTOR COMPLEX

Project Team

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Introduction

**The design of the new Beam Loss Monitor System is needed to upgrade the current system on the Injectors.**

Project Objectives:

=> Build a generic, highly configurable and high performing BLM system.

=> Design the Acquisition part able to accept several detector types.

=> Use reprogrammable parts to target all injectors' requirements.

System Architecture
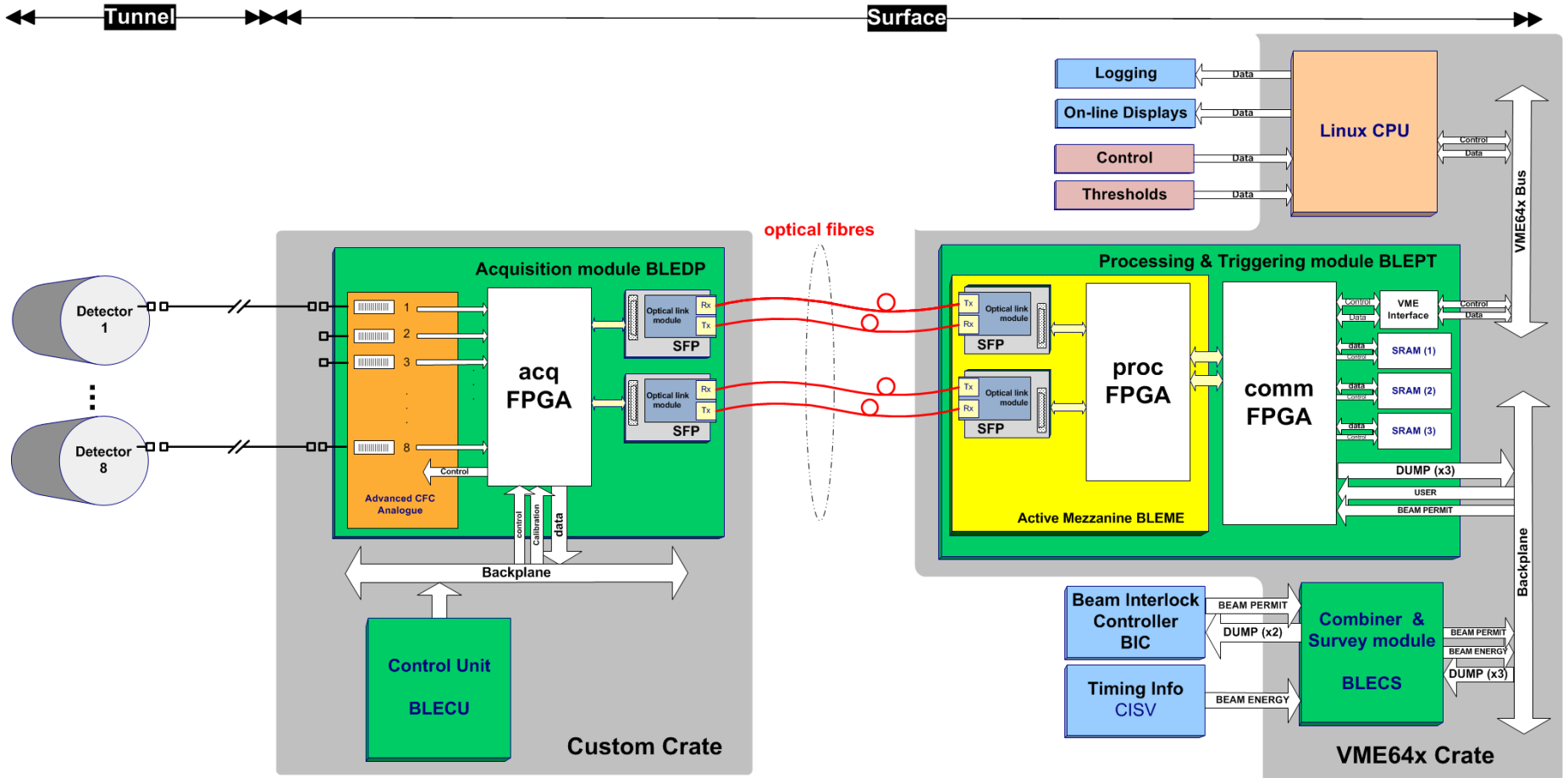
Acquisition Crate
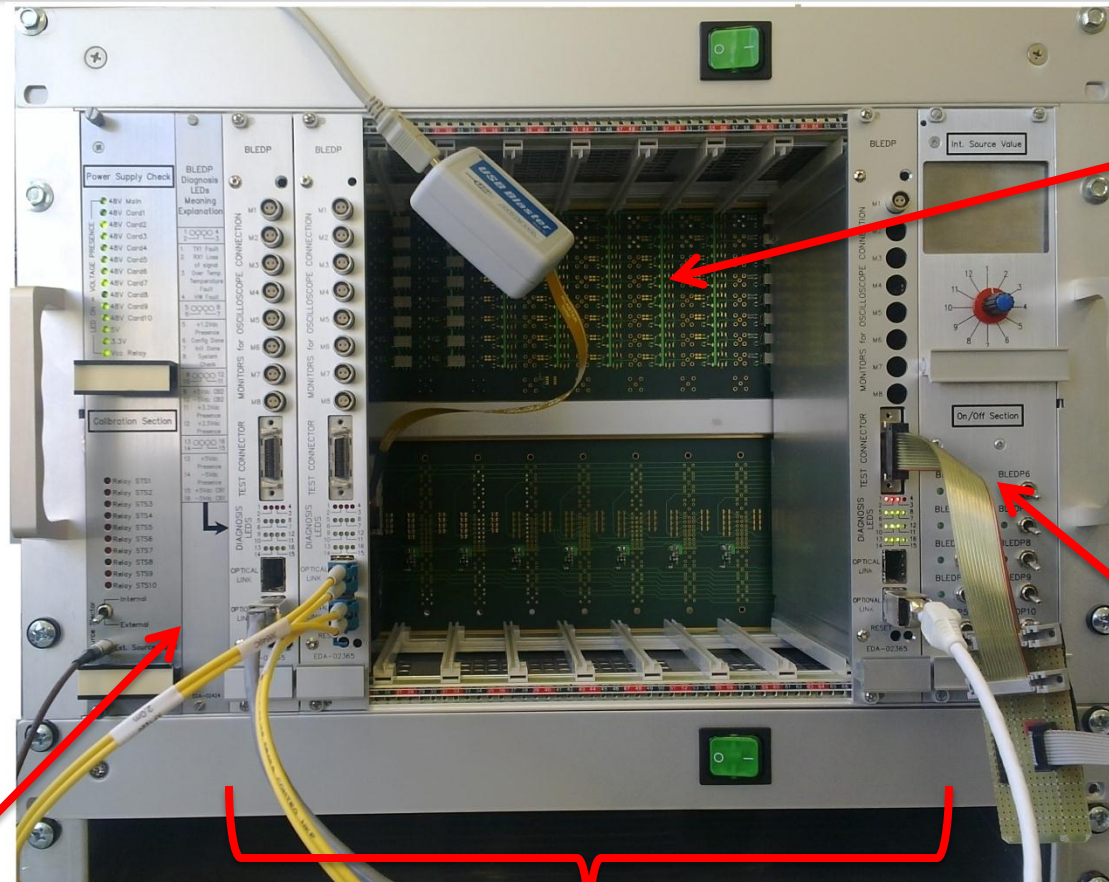
Custom Backplane
See next slide

Control Unit
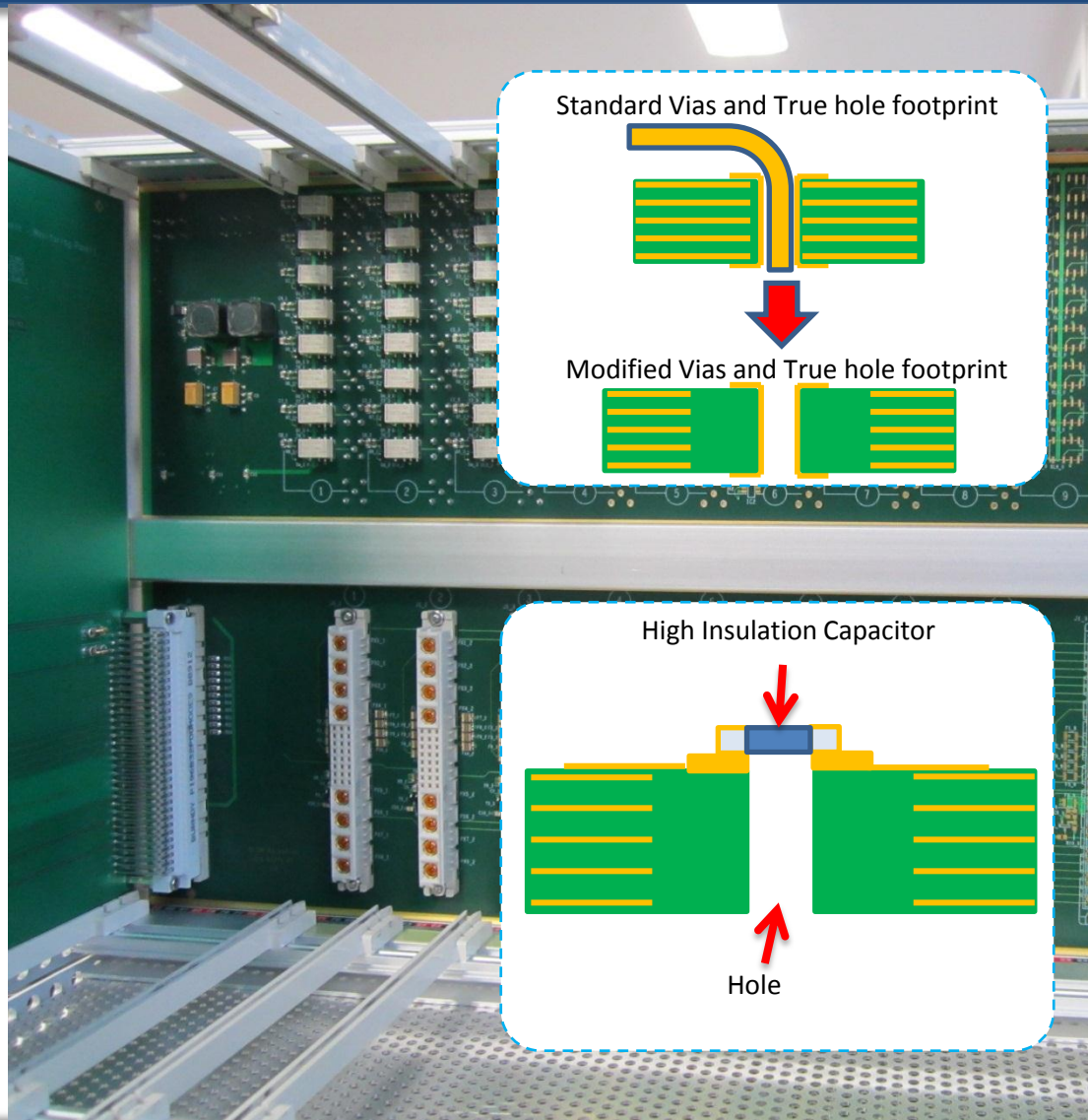Later version w/
advanced remote
functions

Main panel
• Ref. current Input
• LEDs
• Power switch

Acquisition module (BLEDP)
Up to 8 modules with
8 channel each

Backplane of the Acquisition Crate

Standard Vias and True hole footprint

Modified Vias and True hole footprint

High Insulation Capacitor

Hole

CUSTOM BACKPLANE

- Routing of 64 input cables to the 8 BLEDP cards.
- 48Vdc Power Distribution and protection by Circuit Breakers .
- Redundant Power supply single failure tolerant.
- Current Supply monitoring.
- Internal calibration current Source.
- Relays Multiplexer.
- Geographical addressing .
- Chip ID.
- Temperature and Relative Humidity measurement.
- Low Leakage design.
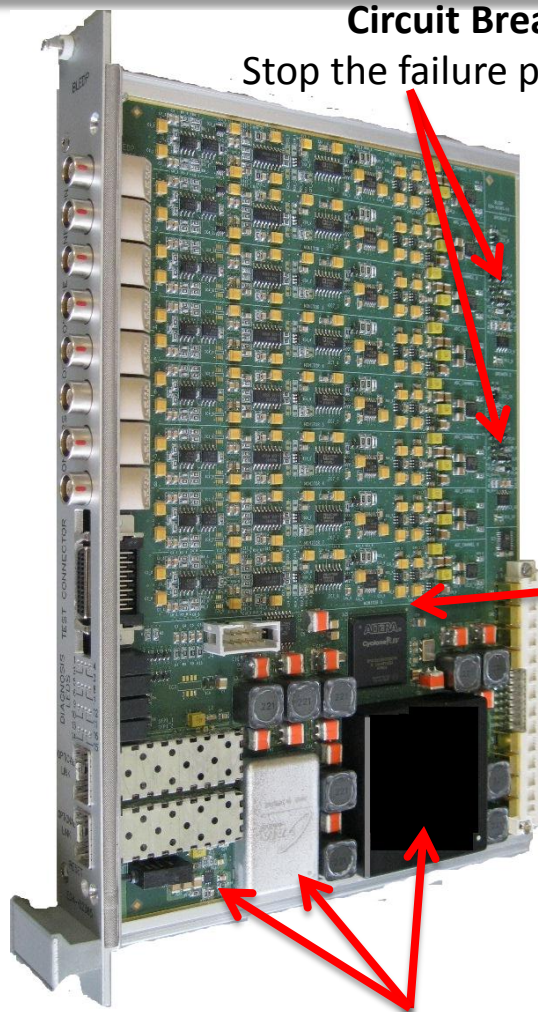
Keeping Down the Power Supply Noise
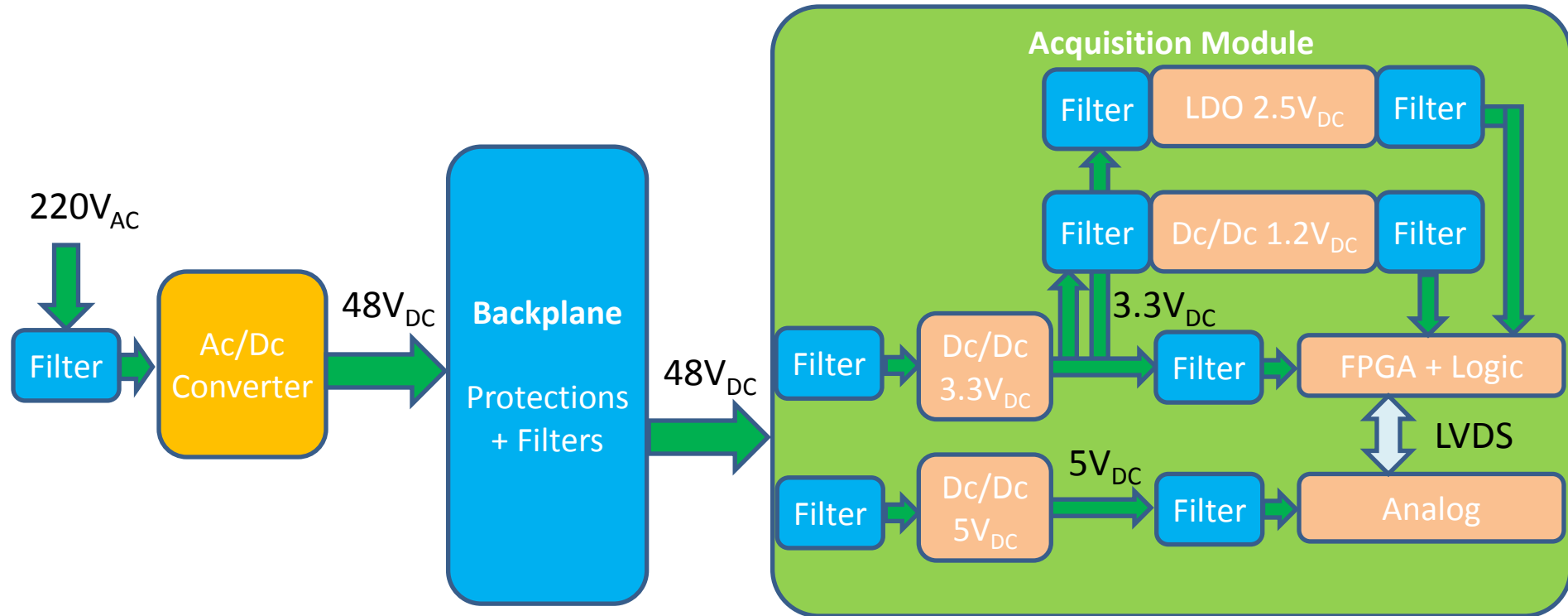
- Several PCB layers are used as ground planes.

- The star point connection is done on the Dc/Dc converters' ground.

Acquisition module (BLEDP)

Currently verifying version 2 of the printed circuit board

Circuit Breakers
Stop the failure propagation

Acquisition
digitisation of 8 channels

FPGA
Altera Cyclone IV

JTAG connection
Local programming and diagnostics

SFP connectors
Gigabit optical and/or Ethernet links

Backplane connection
Analogue inputs, power and control

Local power supplies
Separated for Digital and Analog

Acquisition principle (FDFC & DADC)

**The input channel circuit is able to measure current input from 10pA to 200mA.**

The measurement of the current input is performed by two different techniques:

1) Fully Differential Current to Frequency Converter (FDFC) used in the range **10pA to 30mA**
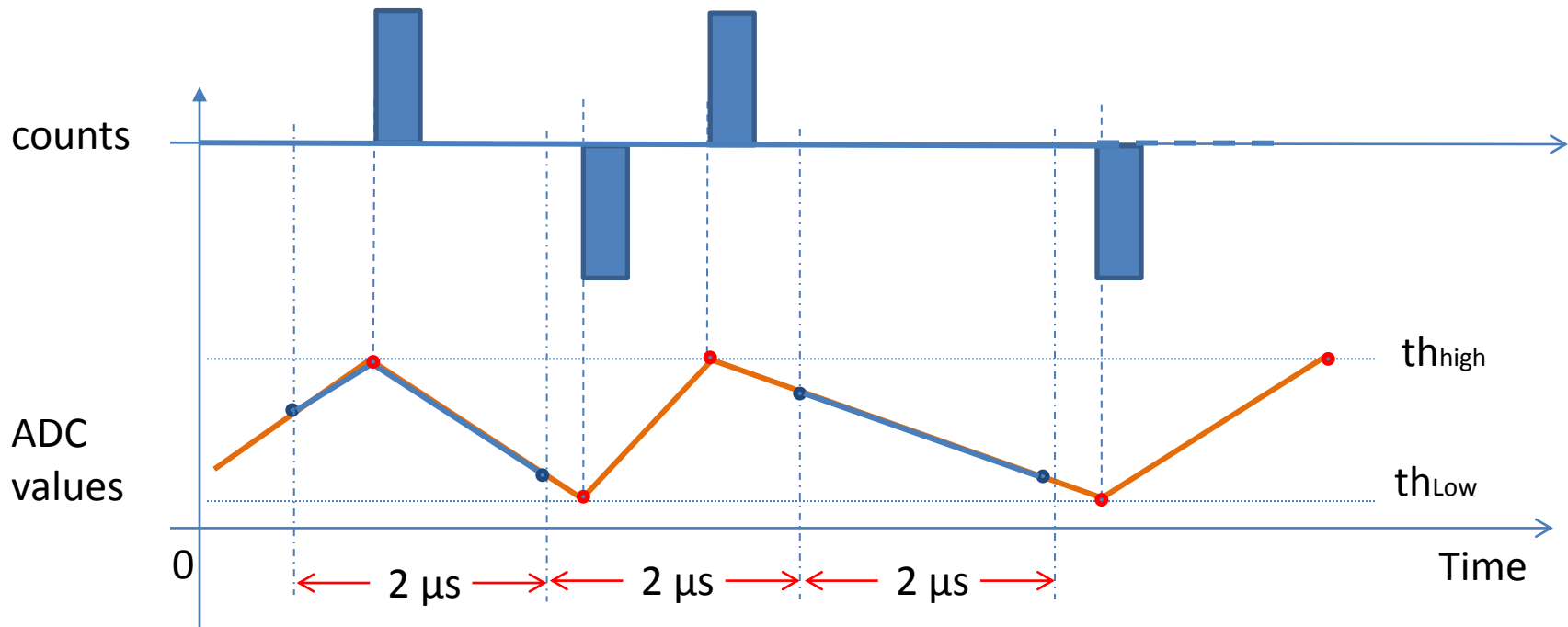2) Direct ADC acquisition (DADC) used in the range **80µA to 200mA**
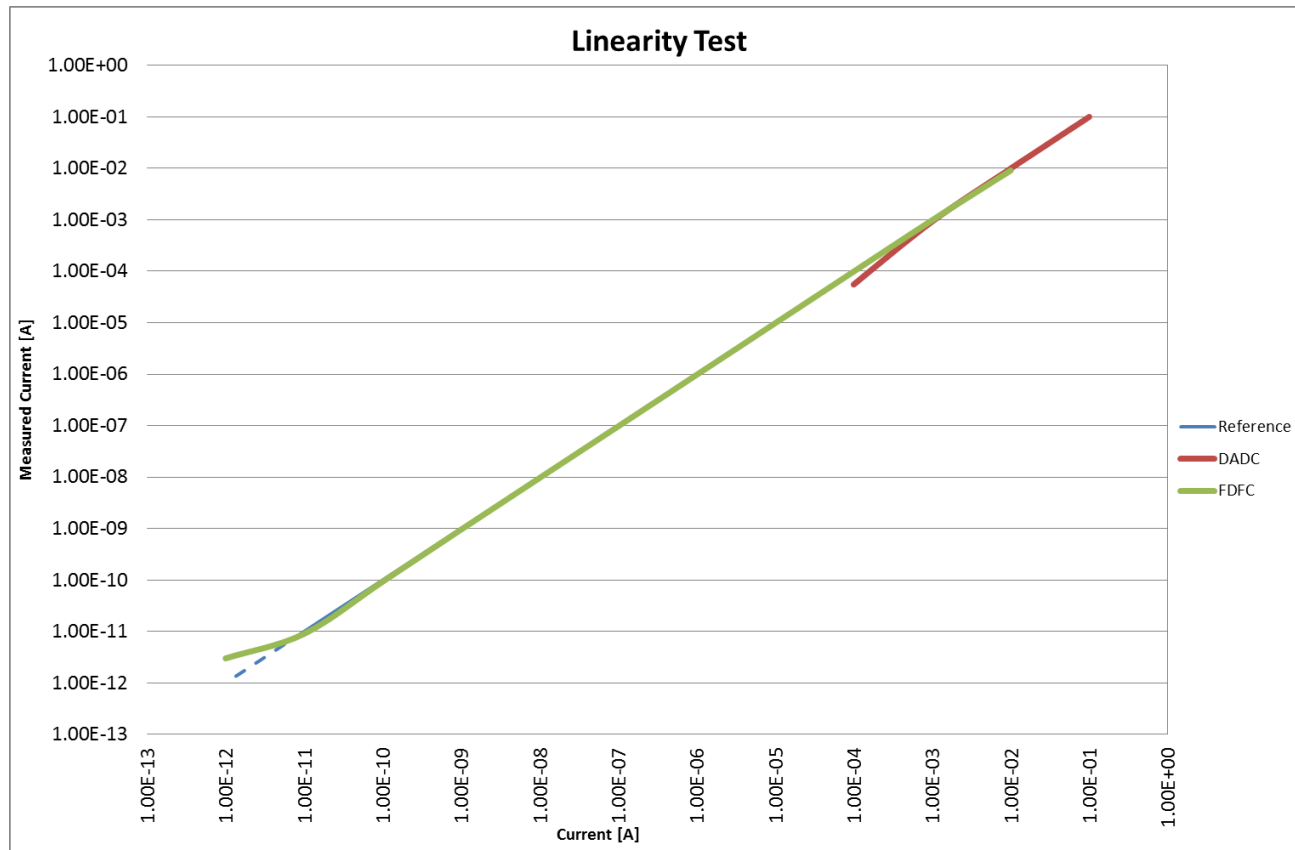
No gain change required: The switch between the 2 ranges is managed by the *FPGA*.
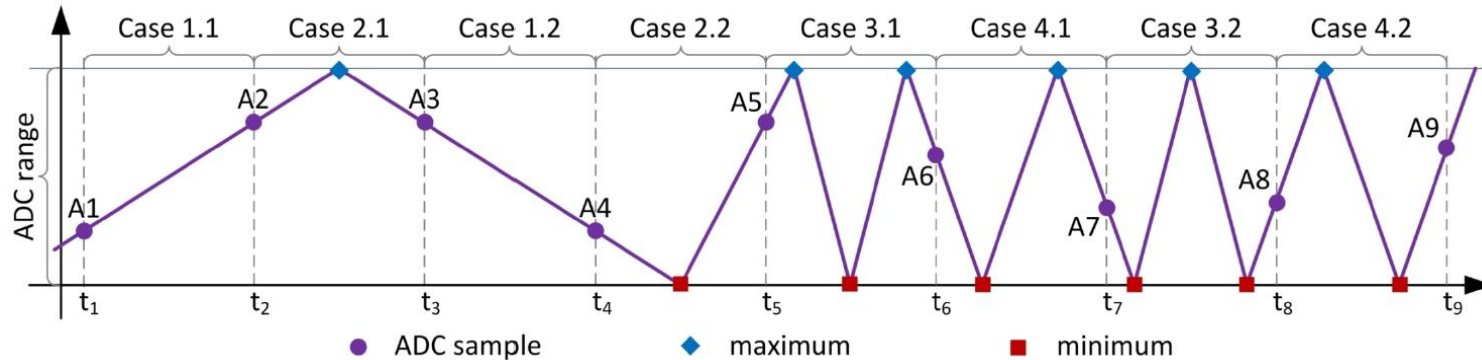
Acquisition Channel Architecture
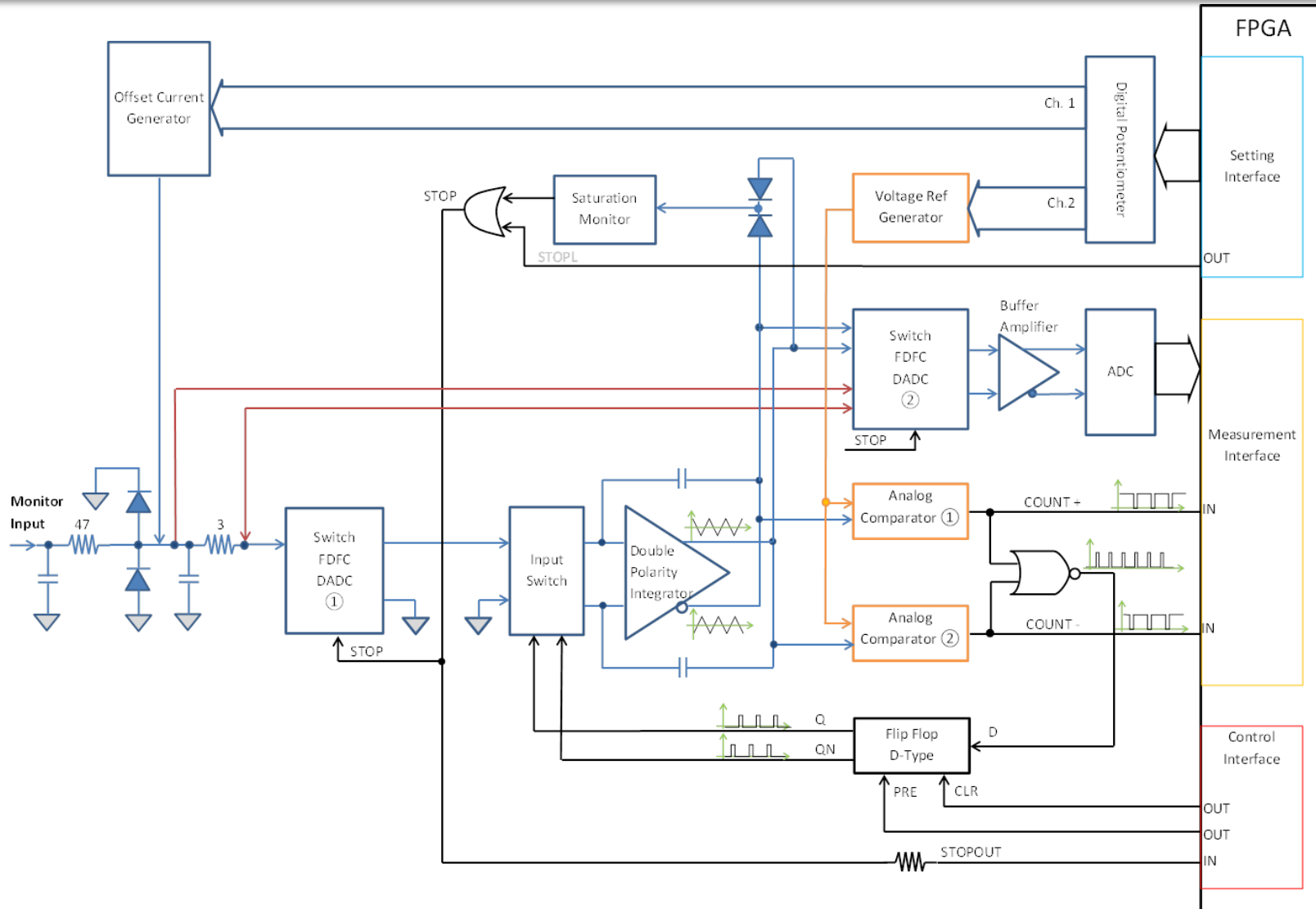
FDFC data processing

- The number of accumulated counts are combined with the ΔADC values to calculate the integrated loss over a 2 μs period.

FDFC Data Merger

| Case	Calculations
1.1	$A_{n+1} - A_n$
1.2	$A_n - A_{n+1}$
2.1	$(max - A_n) + (max - A_{n+1})$
2.2	$(A_n - min) + (A_{n+1} - min)$
3.1	$(max - A_n) + (max - A_{n+1}) + (M - 1) \cdot (max - min)$
3.2	$(A_n - min) + (A_{n+1} - min) + (M - 1) \cdot (max - min)$
4.1	$(A_n - min) + (max - A_{n+1}) + (M - 1) \cdot (max - min)$
4.2	$(max - A_n) + (A_{n+1} - min) + (M - 1) \cdot (max - min)$

Algorithms

- Two types of data acquired: Counts & ADC values.

- Algorithms have been implemented to merge those values for all possible acquisition cases.

- Next step currently under testing: implementation of further algorithms to reduce the noise.
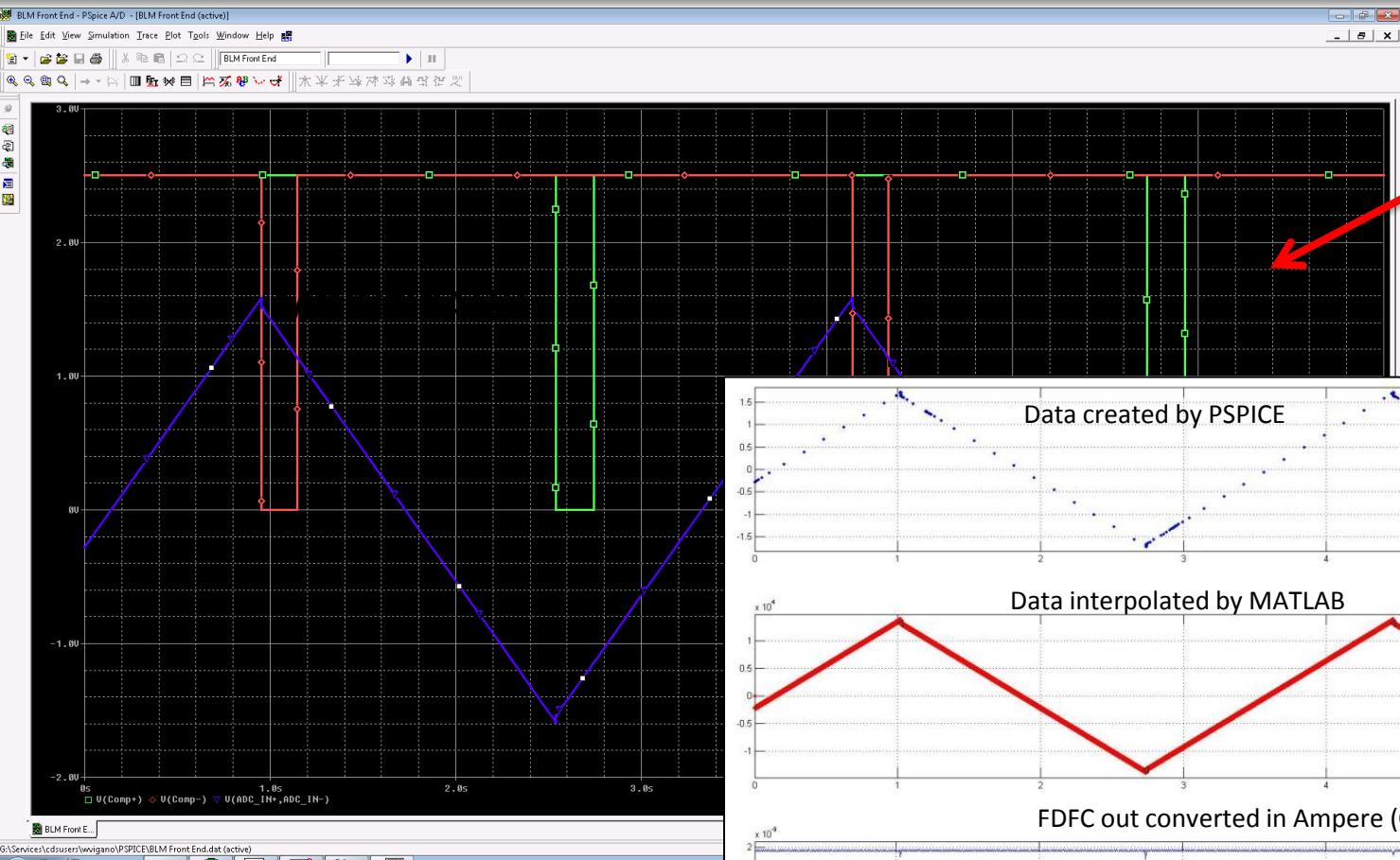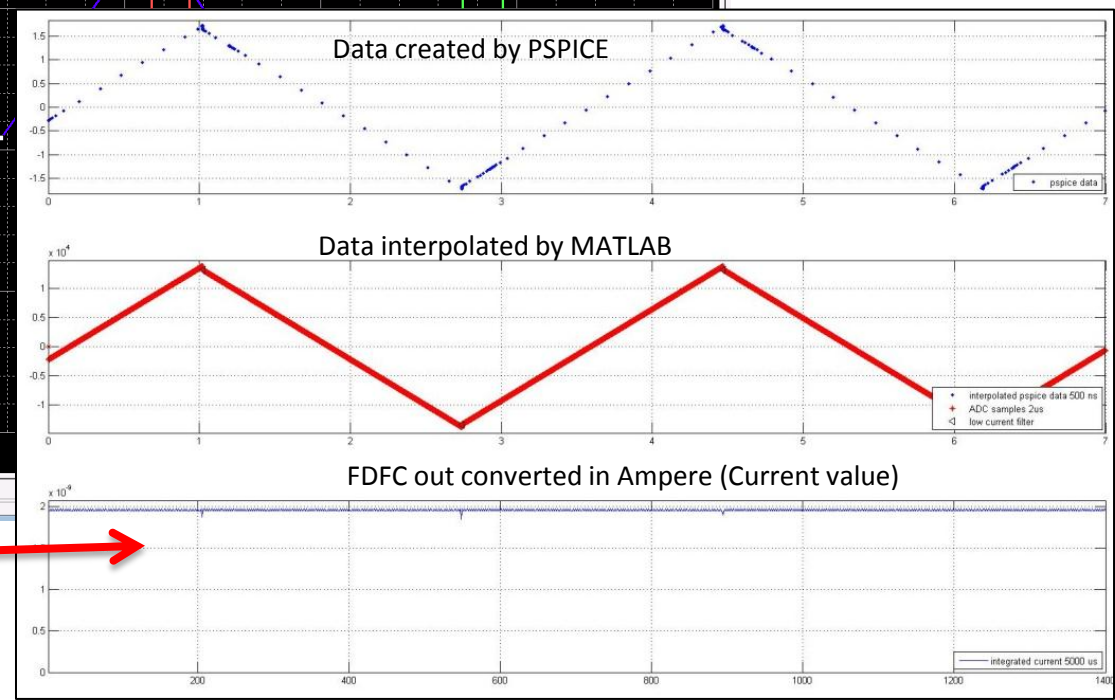
Simulation Model

PSPICE simulation model of the FDFC
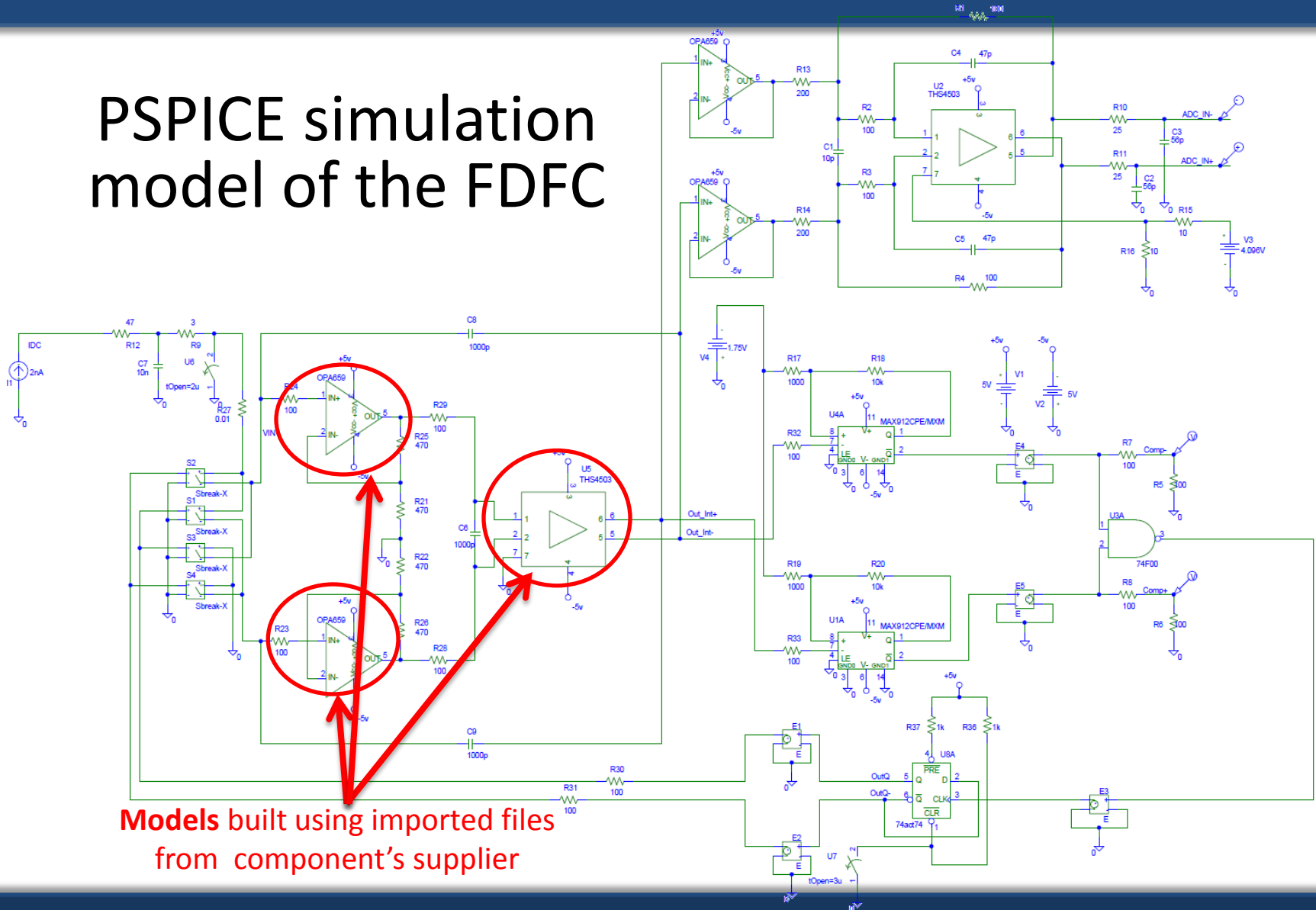
Models built using imported files from component's supplier
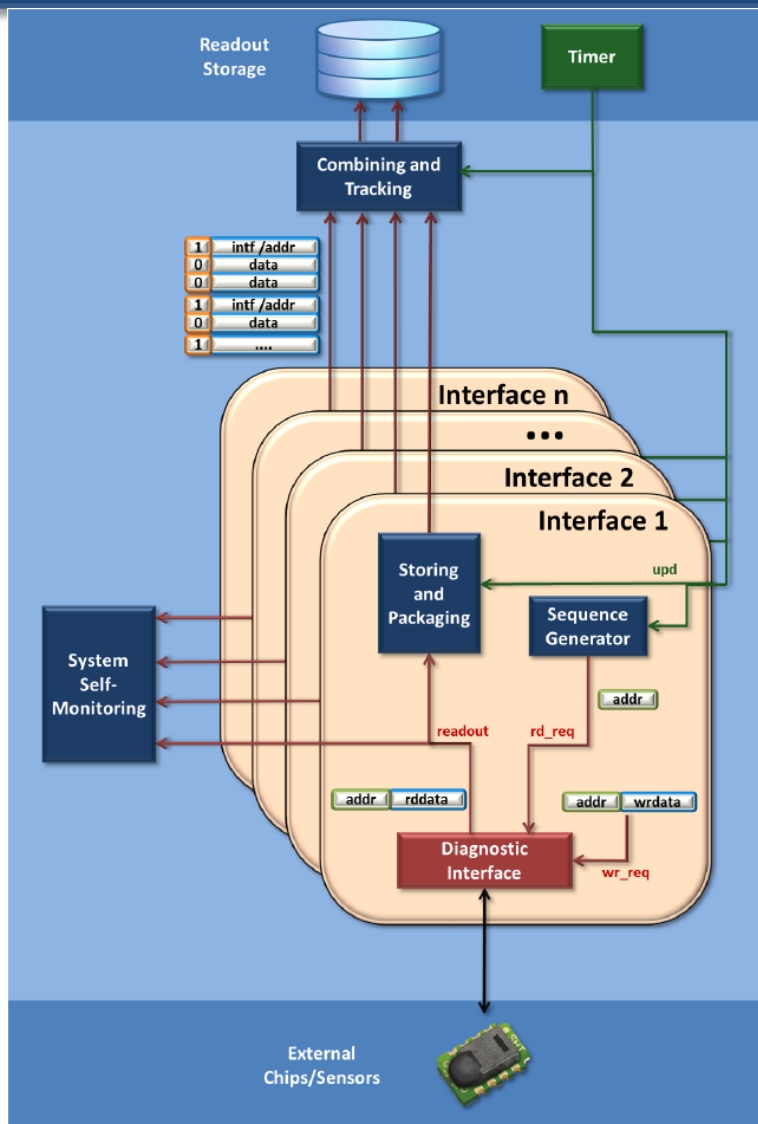
Algorithm Verification with Matlab

PSpice Output
Analog Signal + 2 Comparator Pulses

Data created by PSPICE

Data interpolated by MATLAB

FDFC out converted in Ampere (Current value)

Algorithm Verification with Matlab
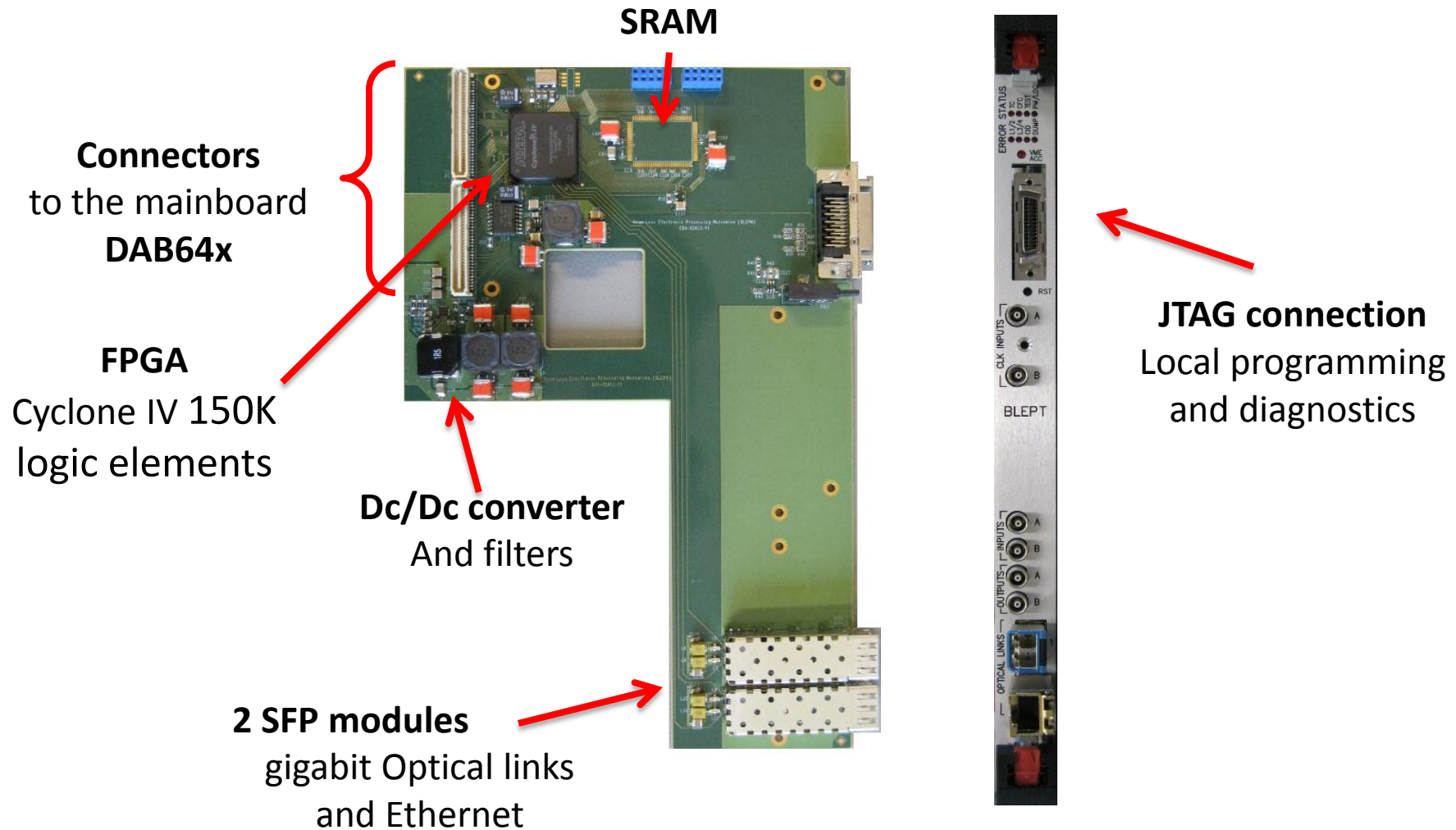Full correspondence with reality

System Survey and Diagnostic Reader


System Survey and Diagnostic Reader

- 100% of the System Functions have Diagnosis

- Read-out status and diagnostic information from connected chips or sensors with every timing event.

- All readouts are afterwards pre-stored, packaged and forwarded to logging.

- Additional interfaces can be easily added to the reader.

- All readouts can be monitored for failsafe actions.

Processing Mezzanine (BLEPM)

SRAM

Connectors
to the mainboard
DAB64x

FPGA
Cyclone IV 150K
logic elements

Dc/Dc converter
And filters

2 SFP modules
gigabit Optical links
and Ethernet

JTAG connection
Local programming
and diagnostics

Acquisition & Processing

- Different Processing per target.

- Selectable integration periods.
  E.g. : 2 µs, 400 µs, 1 ms and 1.2 s

- Threshold values unique per channel
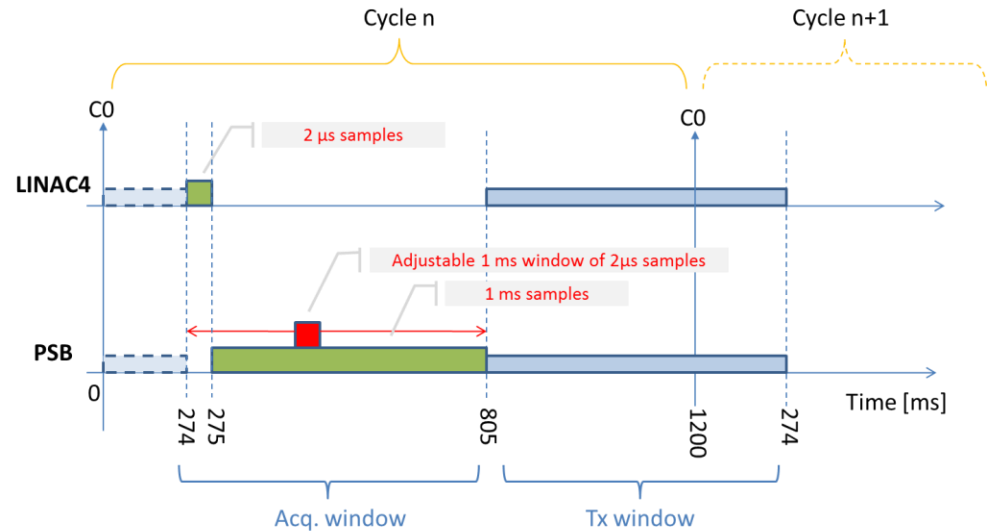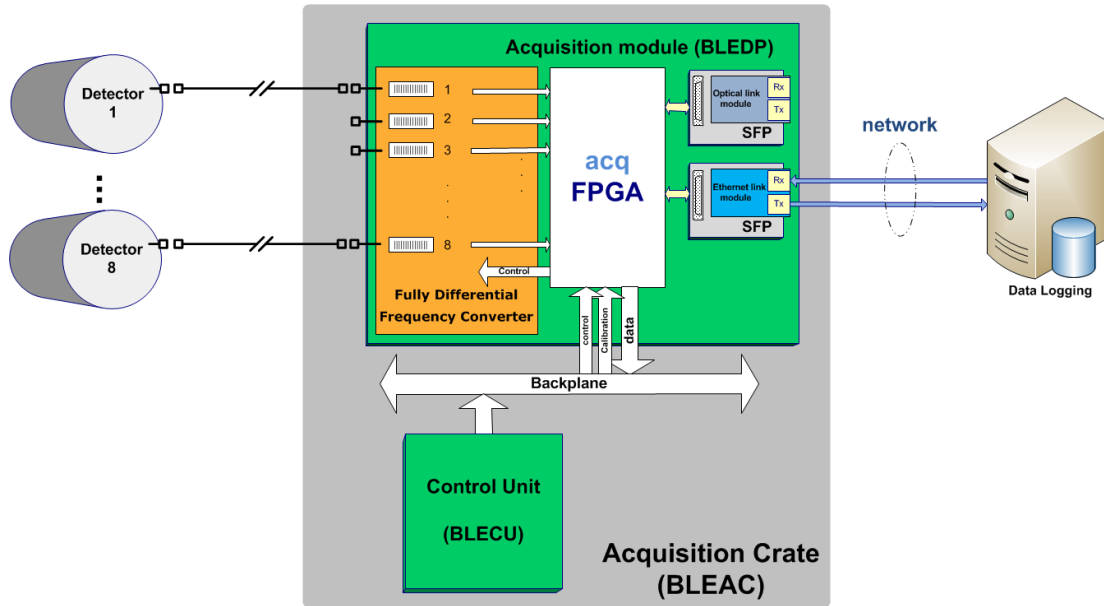

Integration	Minimum detectable current	Minimum detectable dose [Gy/s]	
		Detector: IC	Detector: LIC
2 µs	31.250 nA	5.787E-04	7.234E-03
1 ms	62.250 pA	1.153E-06	1.441E-05
400 ms	0.156 pA	2.889E-09	3.611E-08
1200 ms	0.052 pA	9.630E-10	1.204E-08
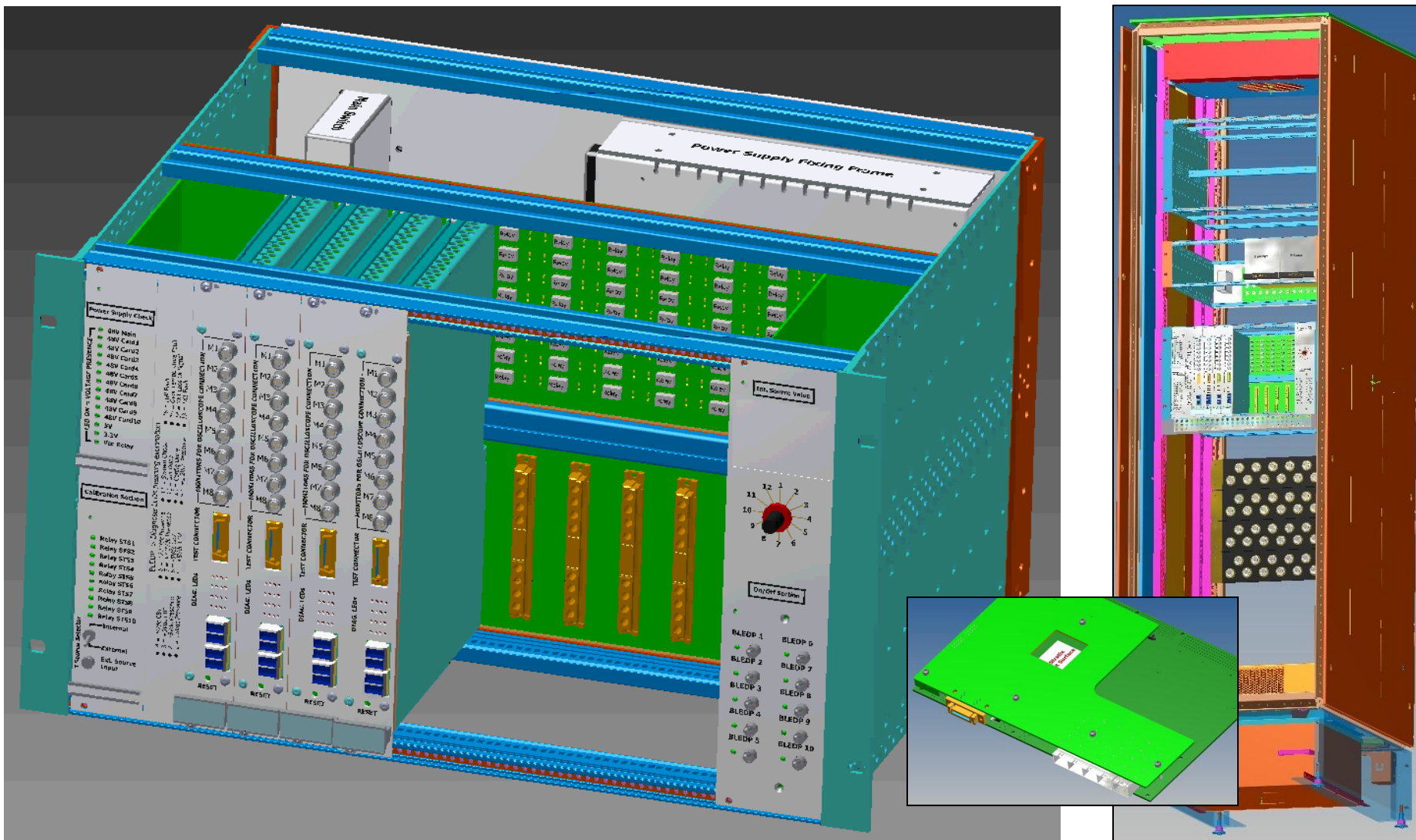
3D Models

5 type of detectors
are connected to
BLEDP cards
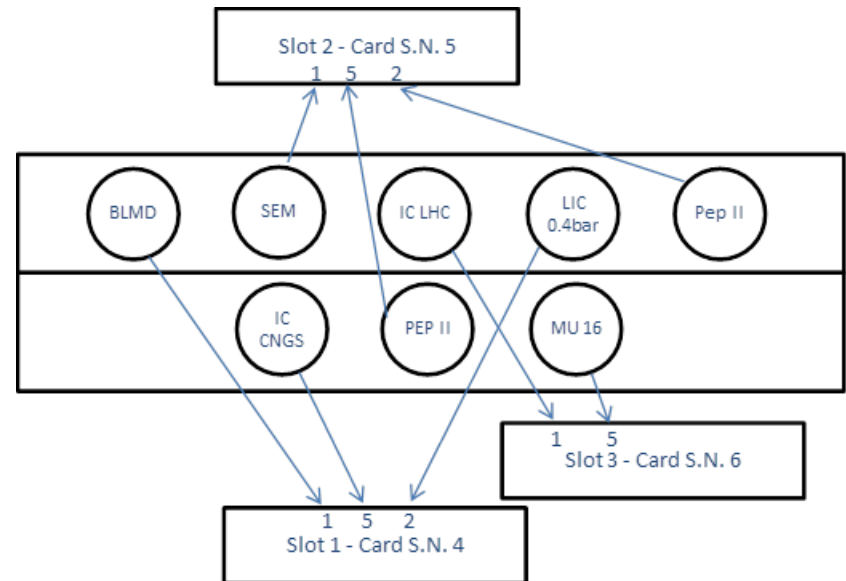
Pre-Series Manufacturing

Ethernet Hub +
JTAG Chain programmer
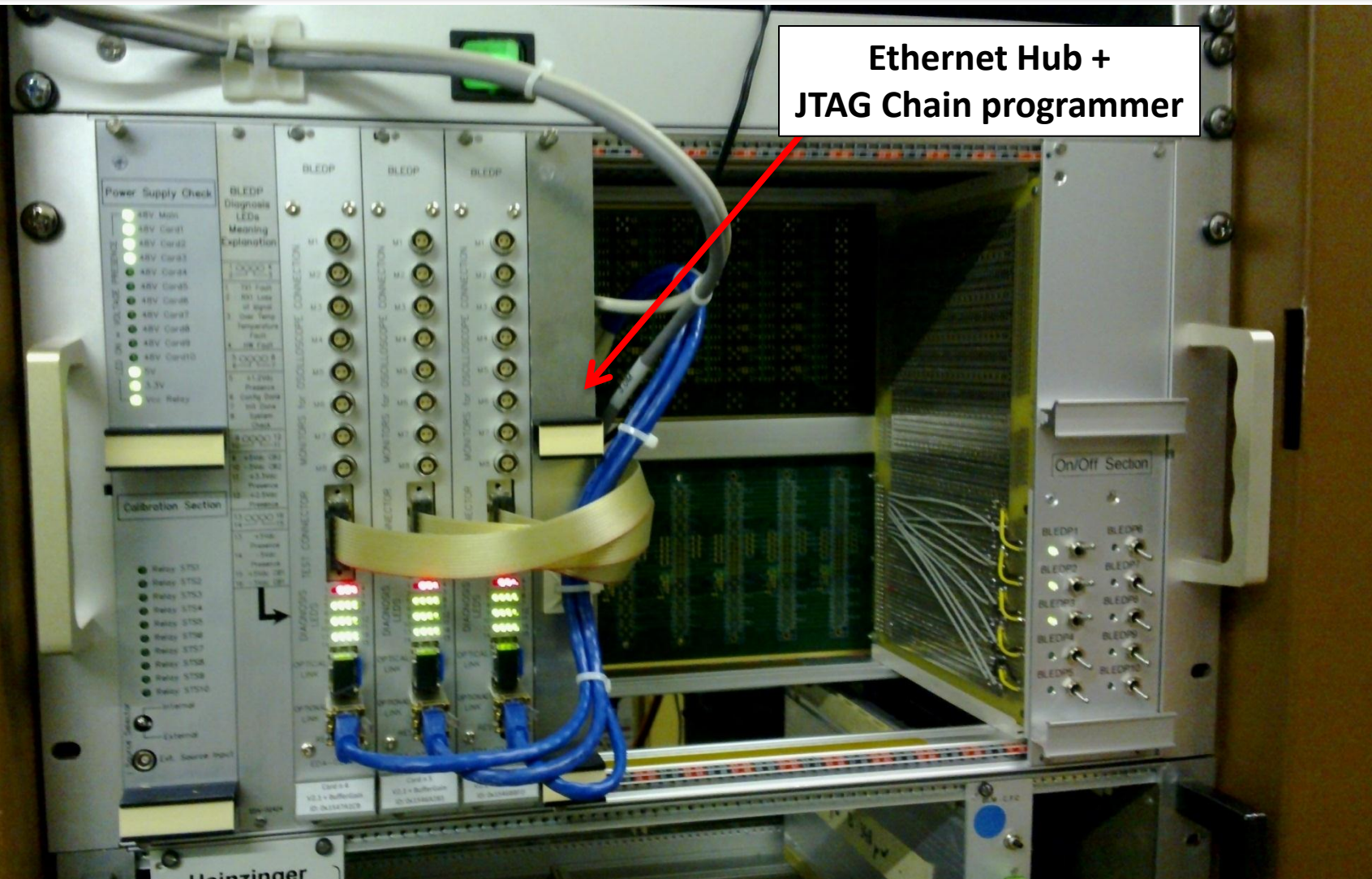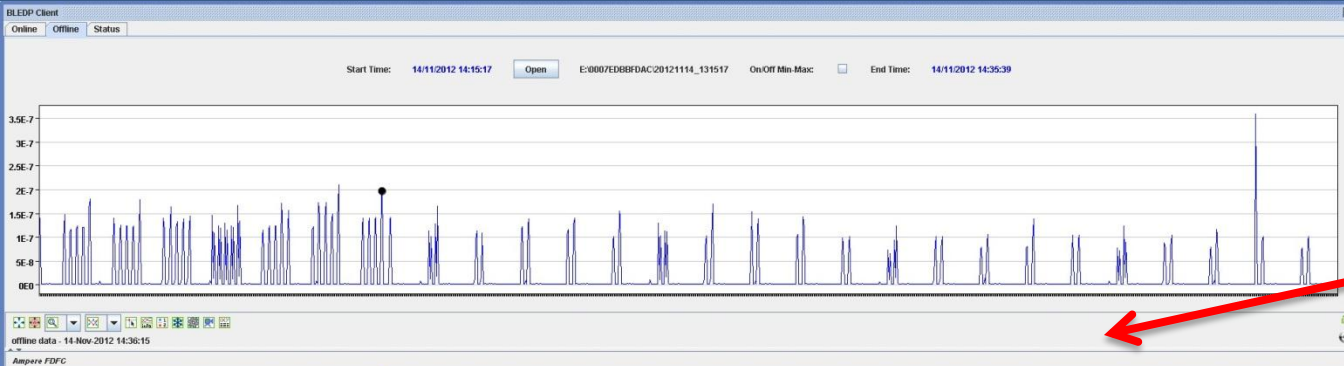
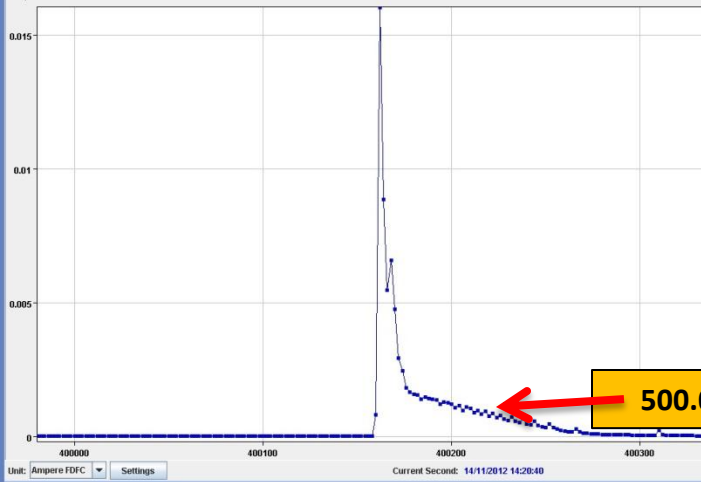# Acquisitions

Ionization Chamber

500.000 acquisition points

PEPII on MU16

THANK YOU