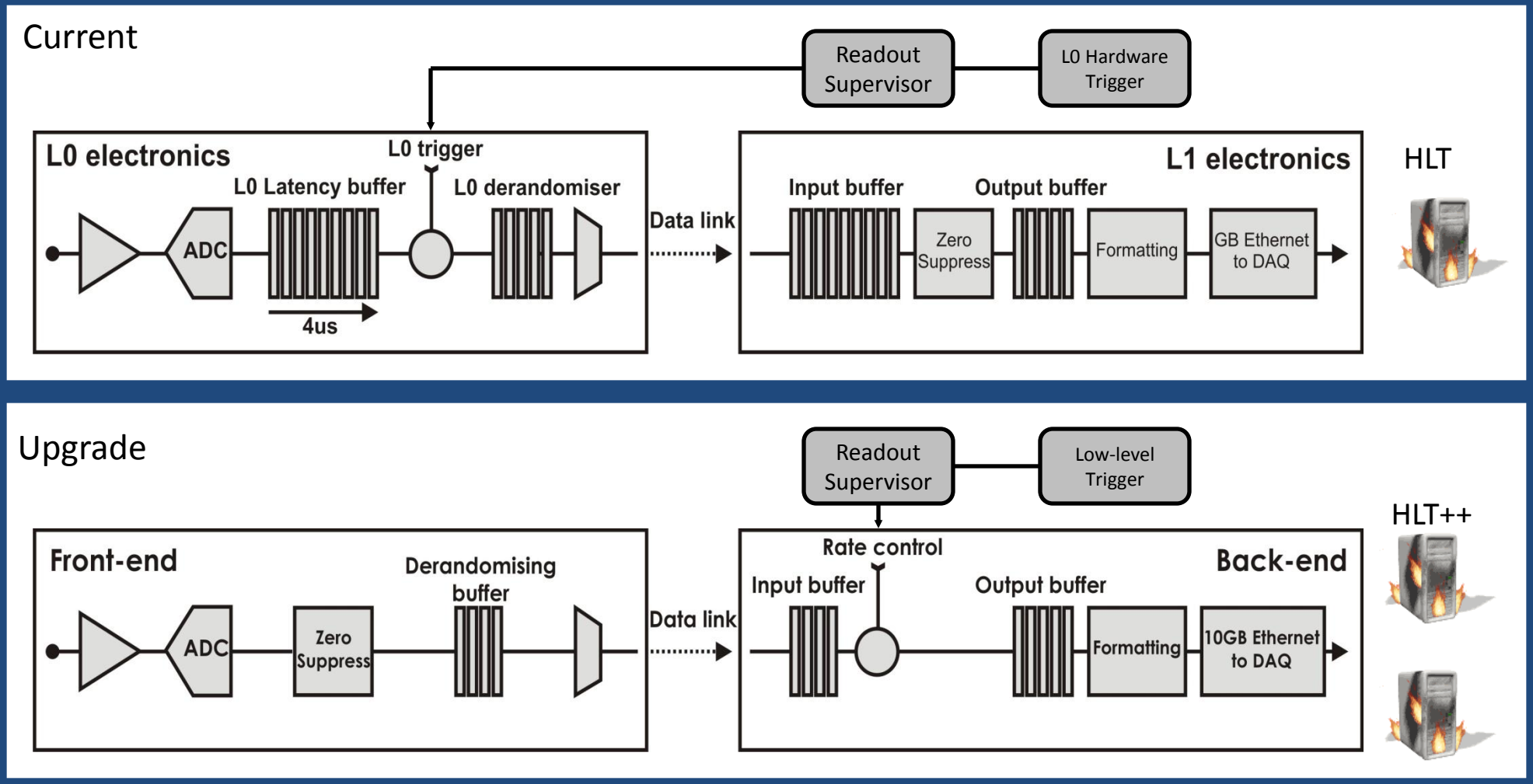
LHCb upgrade

Electronics Architecture Review

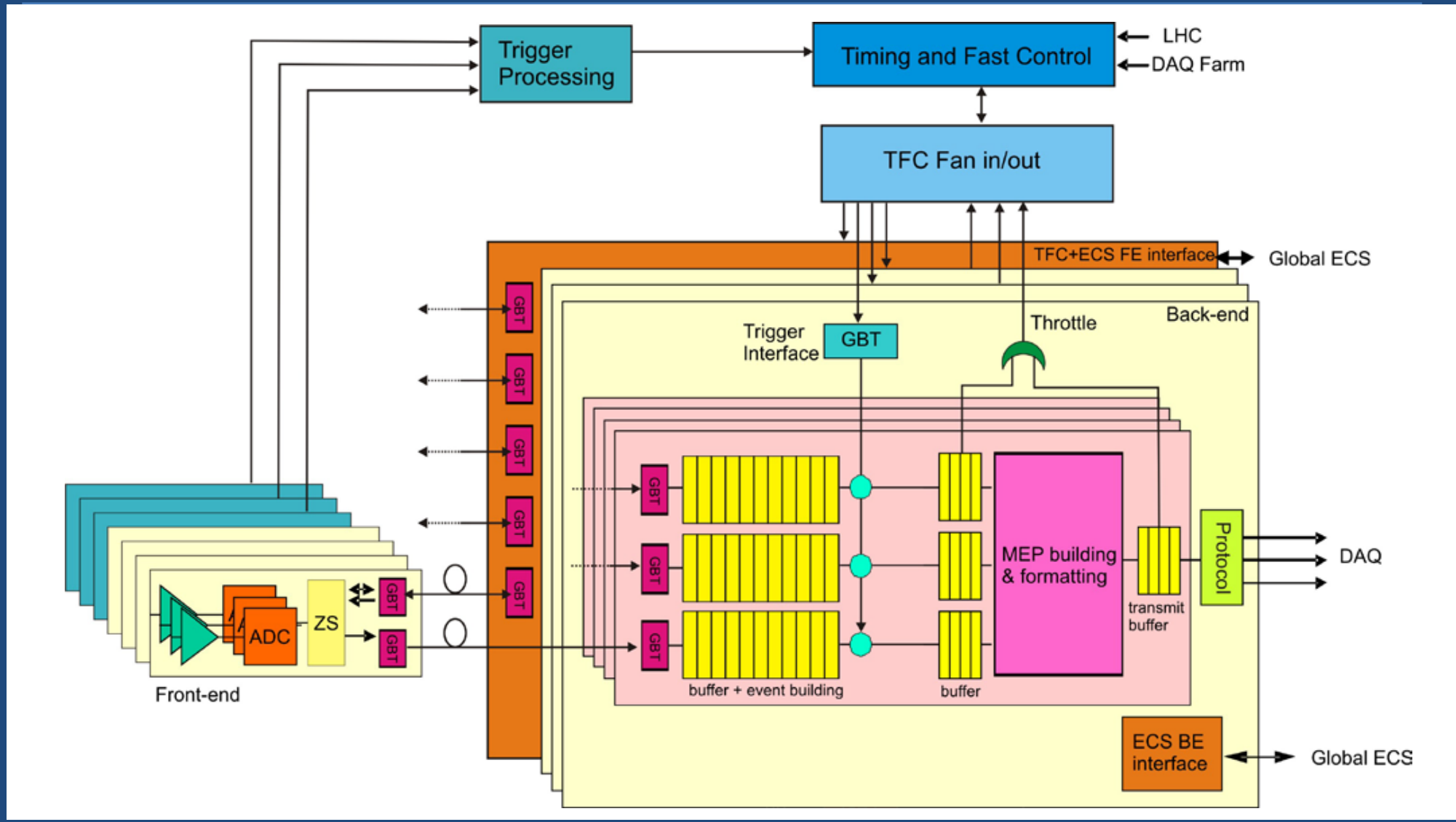
General Architecture & Front-end

Electronics architecture

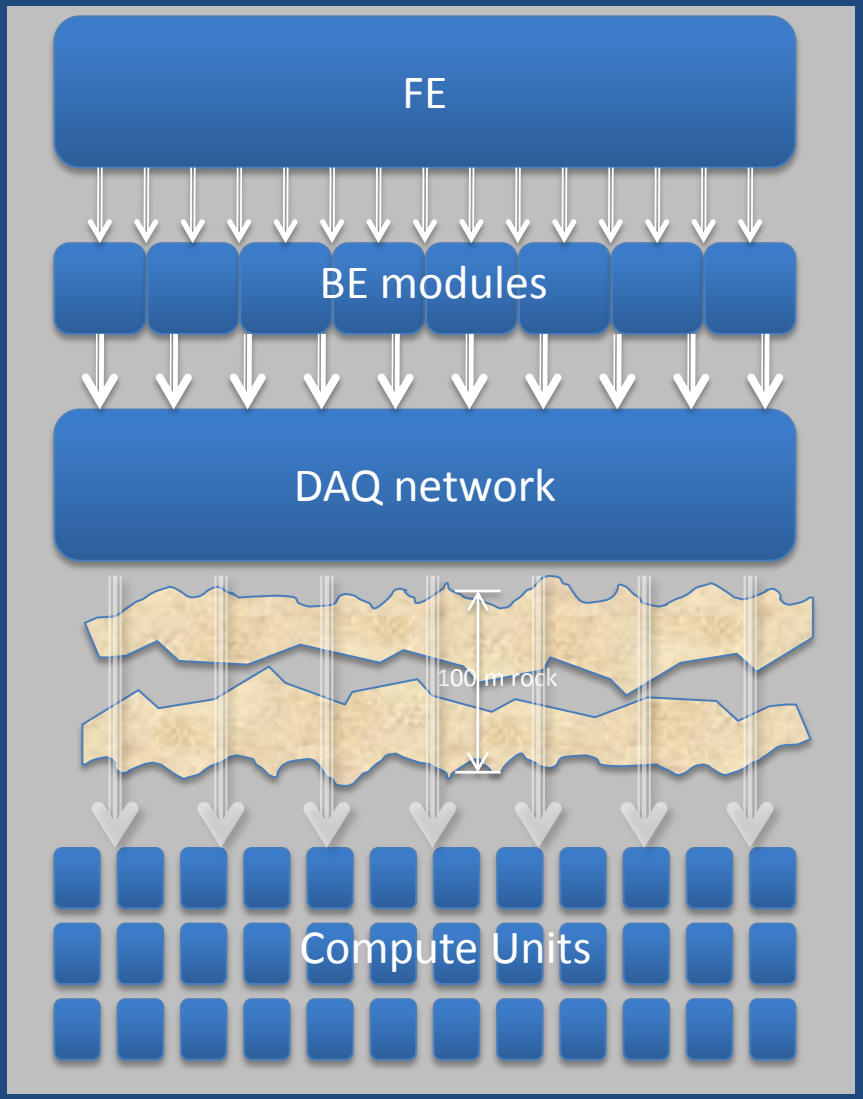
Front-end electronics: transmit data from every 25ns BX



Electronics architecture



Electronics with DAQ



'CLASSICAL' view from Niko

GBT: custom radiation- hard link over MMF, 3.2 Gbit/s (about 10000)

Input into DAQ network (10/40 Gigabit Ethernet or Infiniband)

(1000 to 4000)

Output from DAQ network into compute unit clusters (100 Gbit Ethernet / EDR IB) (200 to 400 links)

General architecture: highlights & open issues

Adopted generic link for FE

GBT chipset + Versatile Link (VL) optics

All BE hardware will be common (carrierboard + AMCs)

TELL40 for data

FE TFC/ECS interface (SOL40)

TFC

LLT interface

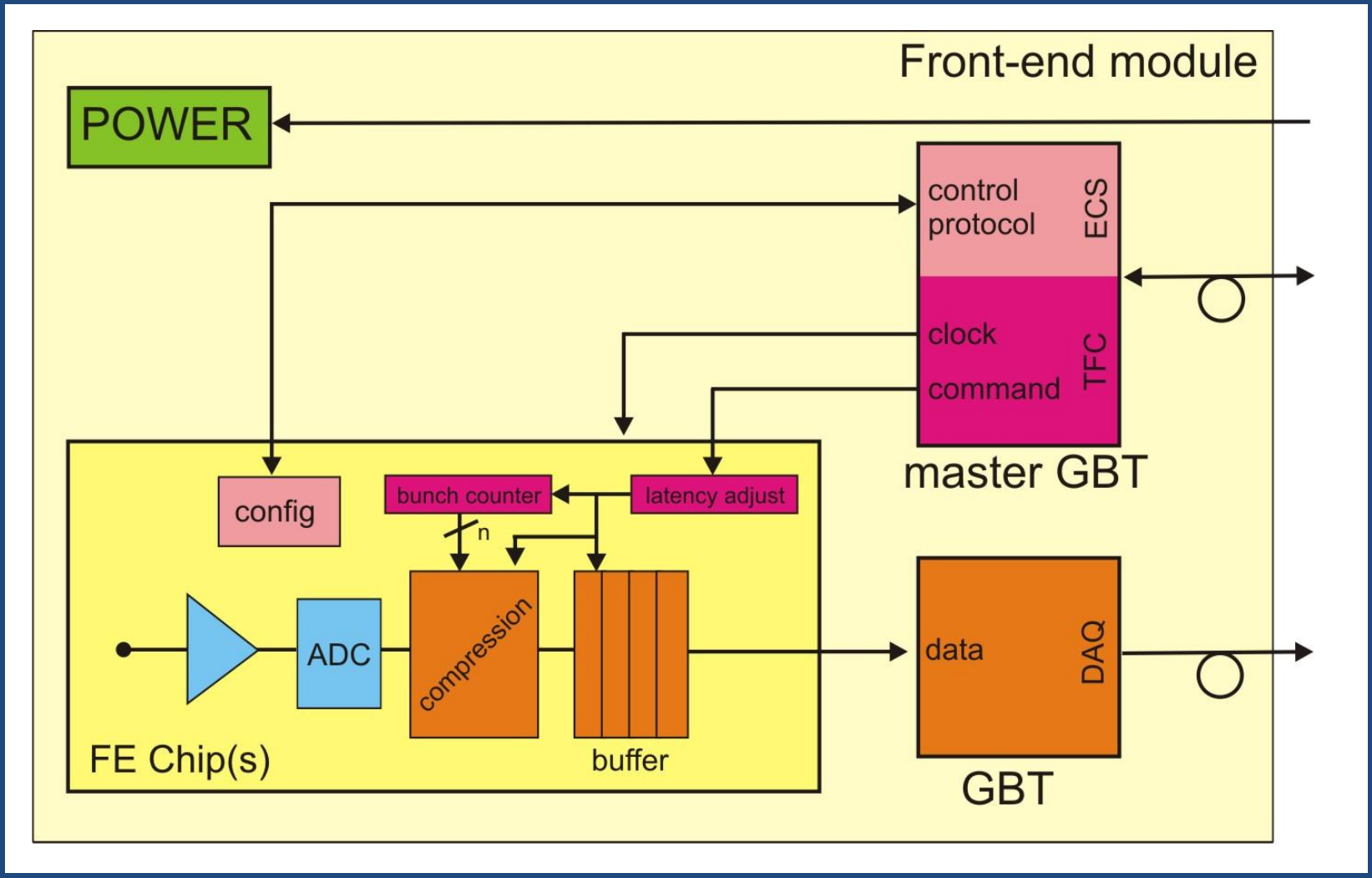
(more from Jean-Pierre)

ATCA baseline technology

Location of TELL40 + switch not yet decided (pit or surface)

Long distance transmission with VL under study

Details of FE architecture



Sub-detector specific blocks 1

Data compression

Driven by cost (minimise links)

Zero-suppression => clear advantage in low occupancy detectors

BUT some have high occupancy => no ZS, buy links

Compression recipes vary: little common overlap

FE buffer

Use link bandwidth efficiently

Riskiest part of system (eg unforeseen background fills up bandwidth)

Sub-detectors must make best estimate from simulations

- use safety factor
- make system scale-able?

If buffer overflow => truncation of payload data

Sub-detector specific blocks 2

Non-ZS data

Requested by some sub-detectors (for tuning/diagnostics)
Send as part of normal data stream (controlled by TFC)
Buffering implications to be understood

BXID

Data tagged with BXID early
BXID reset is main tool for overall synchronisation
All synch-checks, event building, LLT based on BXID
Tune-able preset of BXID counter
BXID is ALWAYS transmitted as part of header
(even during truncation)

Sub-detector specific blocks 3

Fast commands from TFC (see Federico)

Pre-delayed to match transmission latency

Resets & other special fast commands

Storing instantaneous state of FE (then read thru ECS)

Running modes

Configured by ECS (ie not on-the-fly)

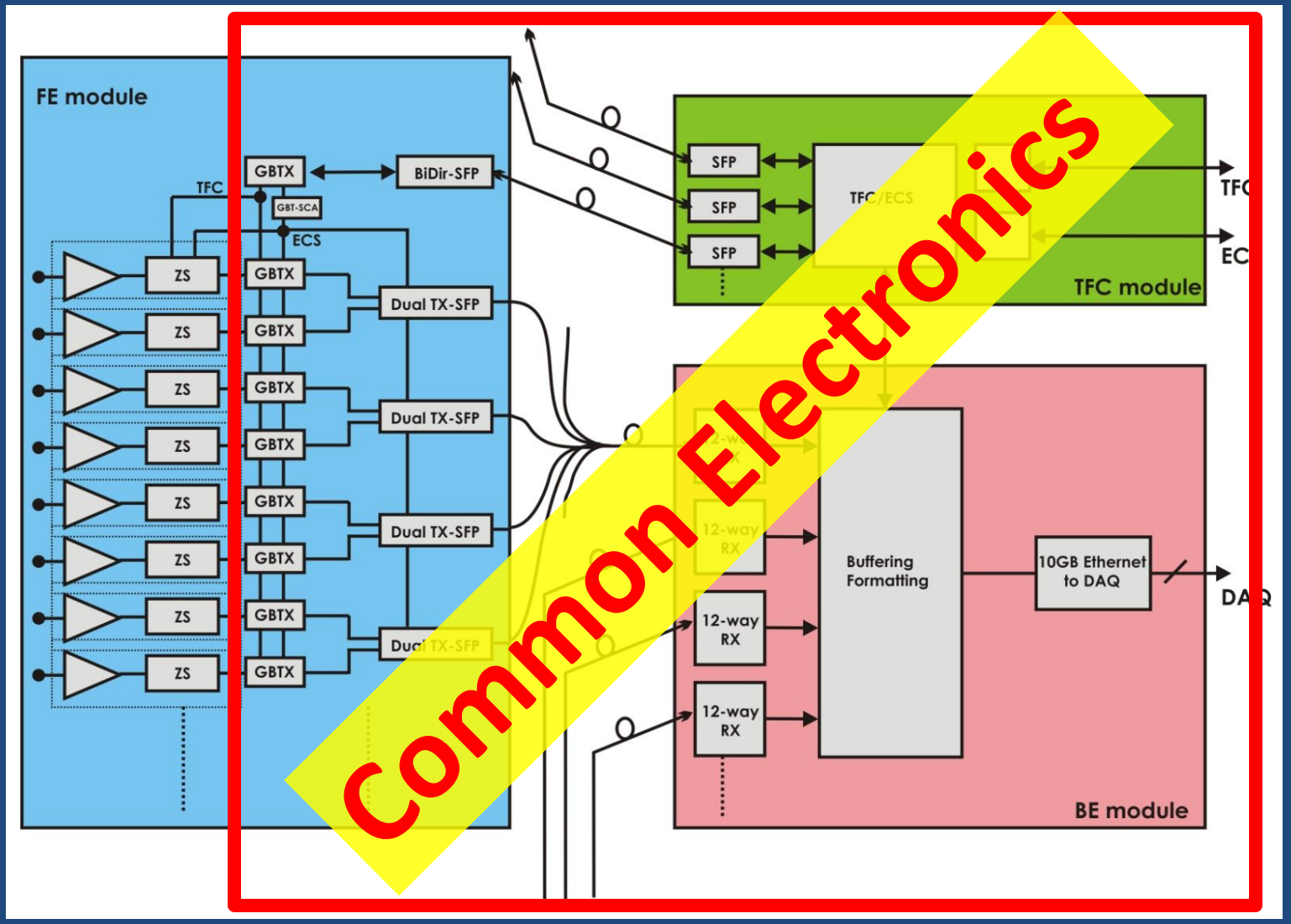
Diagnostic patterns for measuring link latencies

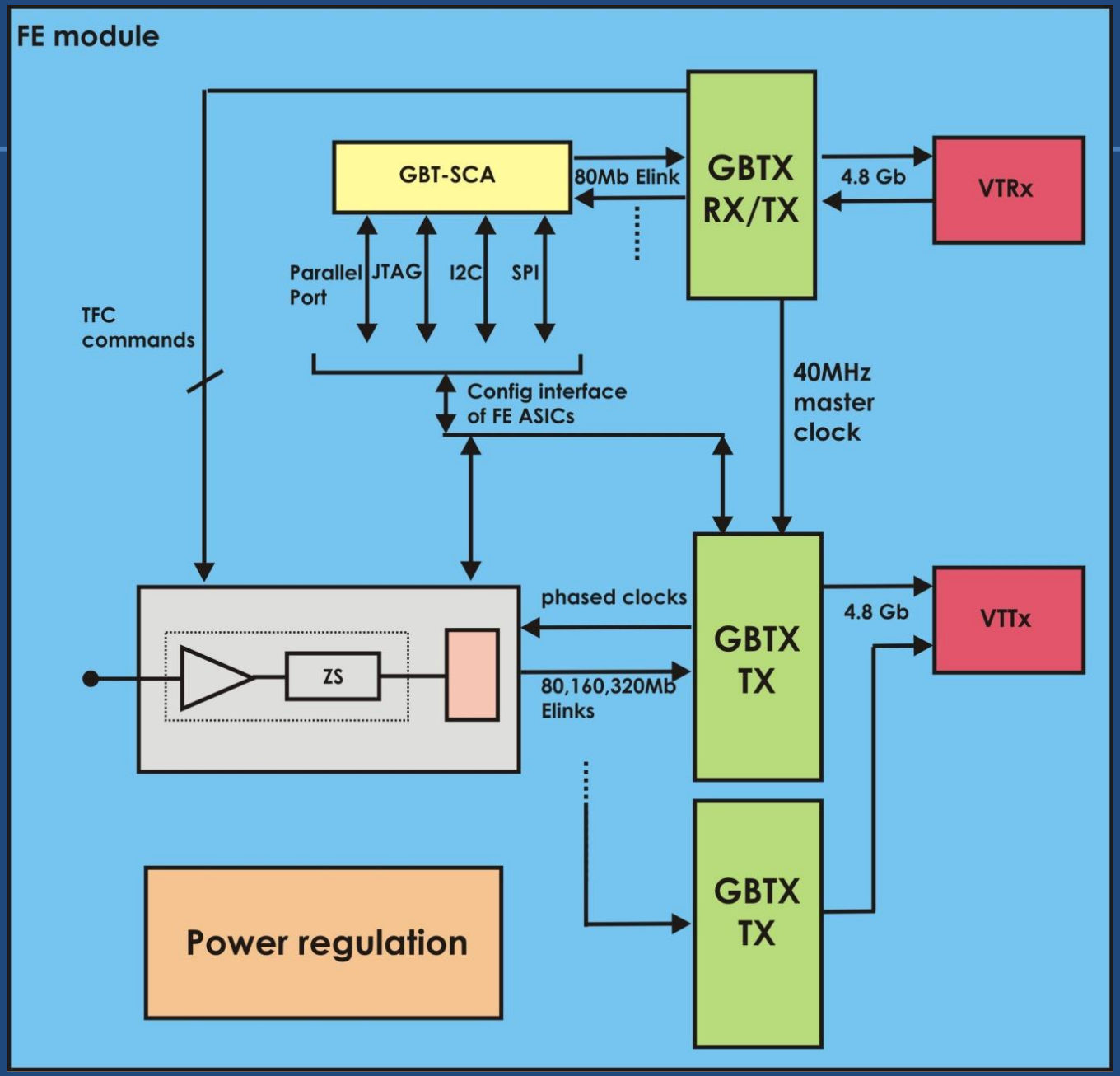
Test features

Electrical pulse, triggered light source, cosmics

Digital patterns generated by FE

Generic Sub-Detector Readout & Control





FEC format

FEC format Or wideBus

Common items 1

GBTX

Good contact with design team

But schedule is a worry

Prototypes not yet available

GBT-SCA

Schedule not clear yet: worry

Prototypes not yet available

Versatile Link

Proposed schedule OK for LHCb (2014 – 2015)

Prototypes available

Common items 2

DC-DC

Tests done with prototypes: successful

LHCb deciding on flavours & quantities

Can we start producing in 2013?

Low Voltage Power Supplies

Plan is to re-use existing systems

Estimated quantities of new purchases are small

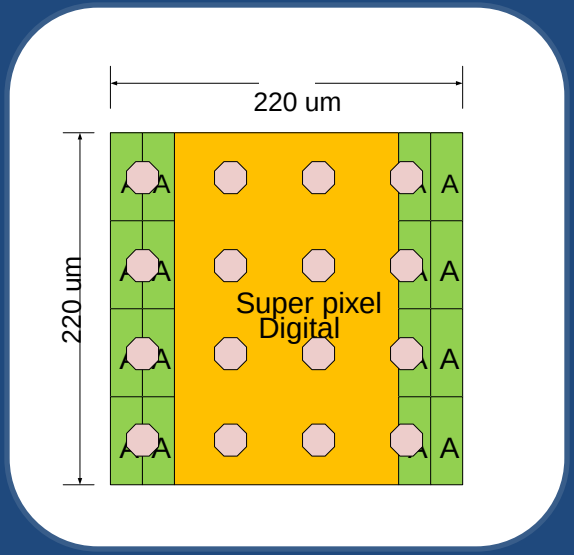
..... but obsolescence .....

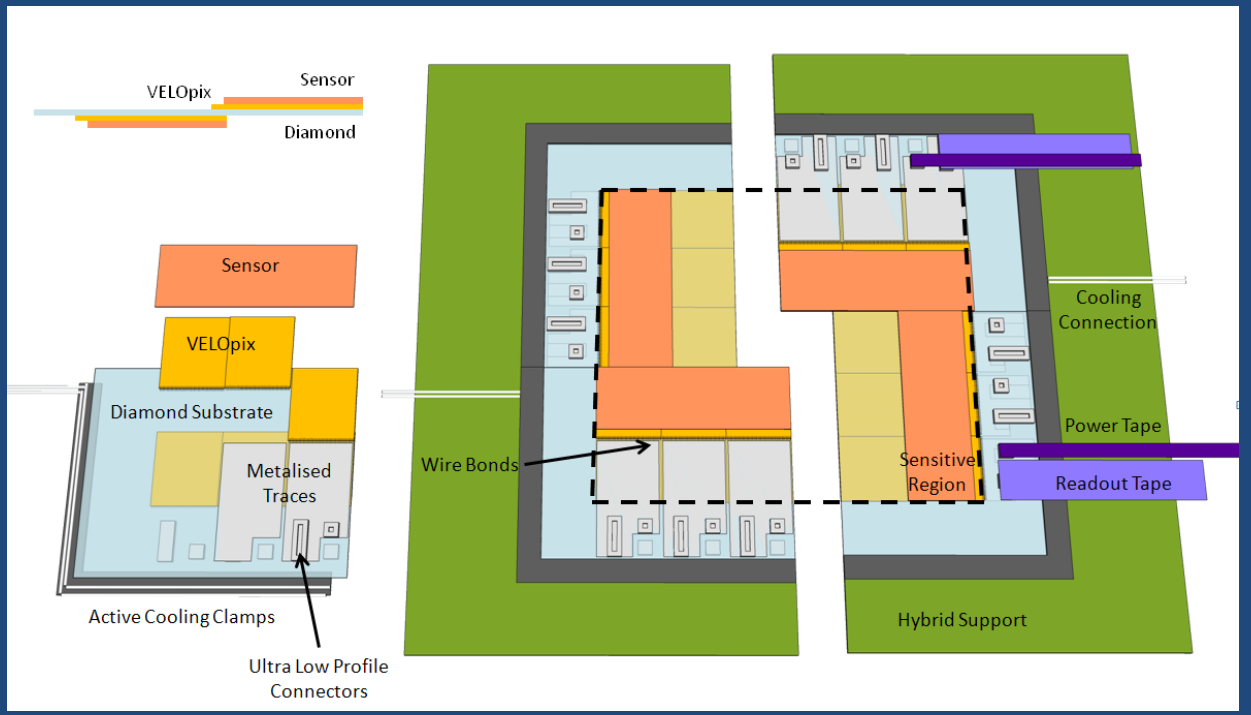
Spare slides
Sub-detector details

VELO pixel

VeloPix chip: 256 x 256 array, 55 x 55 μm pixels

- Strong overlap with TimePix3 (under design)
- 3 or 4 bits TOT
- Architecture to minimise bandwidth (hottest chip = 12 Gbit/s)
- Serial readout





Ken Wyllie, CERN

VELO strips & Silicon Tracker

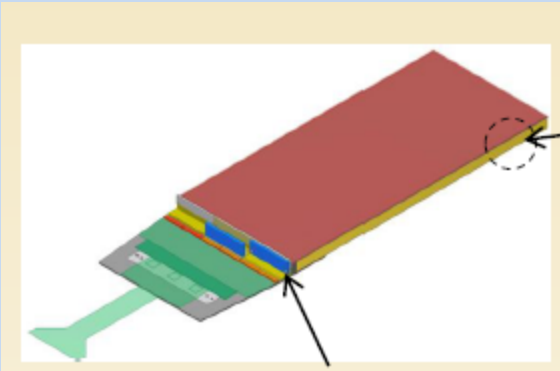
SALT ASIC under design
128-channels, each with 6-bit ADC
On-chip data compression planned
(pedestal subtraction, common-mode correction)

Tracker

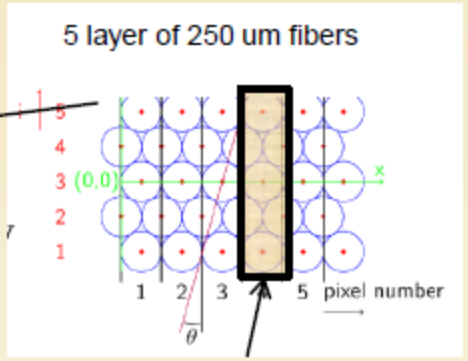
SciFi tracker

Fibres coupled to SiPM
SiPM Radiation tolerance?

ASIC design starting



SiPM array

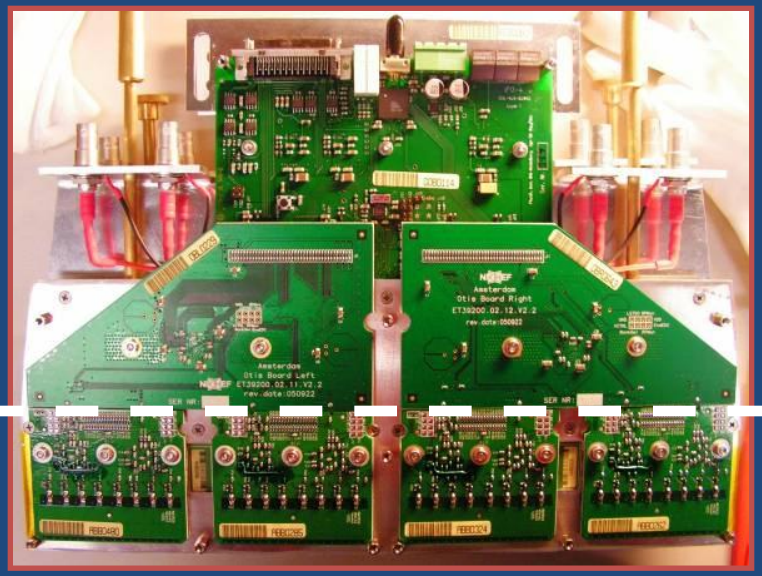


SiPM cell coverage

Outer tracker

Re-use front end

Implement TDC (1ns) in ACTEL ProASIC FPGA: prototype already working

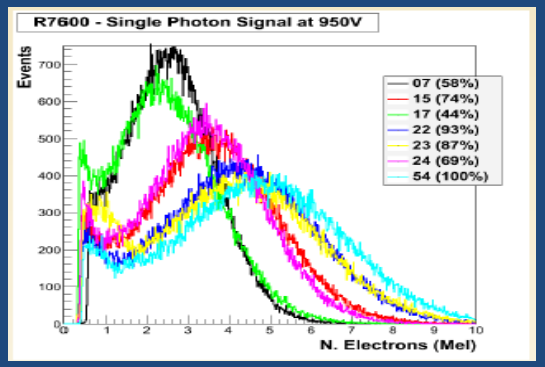


Re-use

Replace

RICH

MaPMT (baseline) option



CLARO ASIC under design:

- Gain compensation
- Binary output

Digital functions in ACTEL

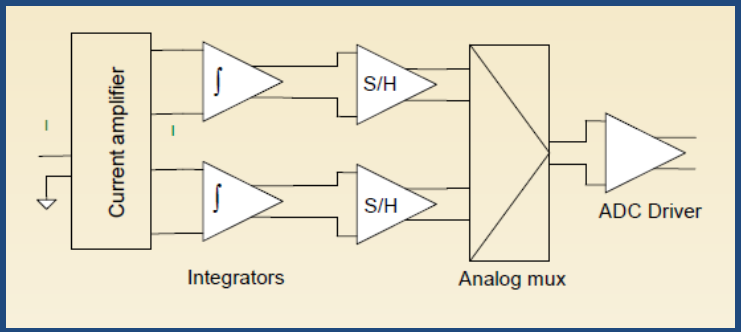
Muons

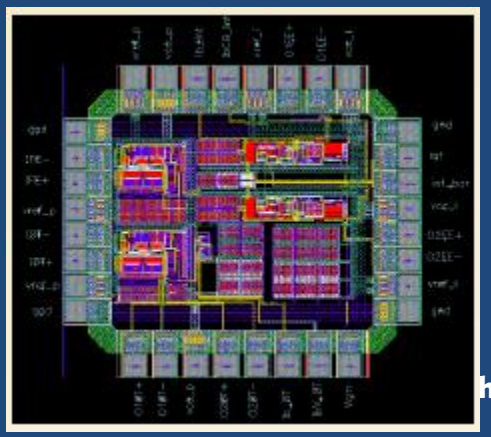
40MHz data transmission already – re-use

Calorimeter

MaPMT gain reduction
⇒Reduce electronics noise
⇒Active termination in ASIC (à la ATLAS LAr)

Interleaved integrators



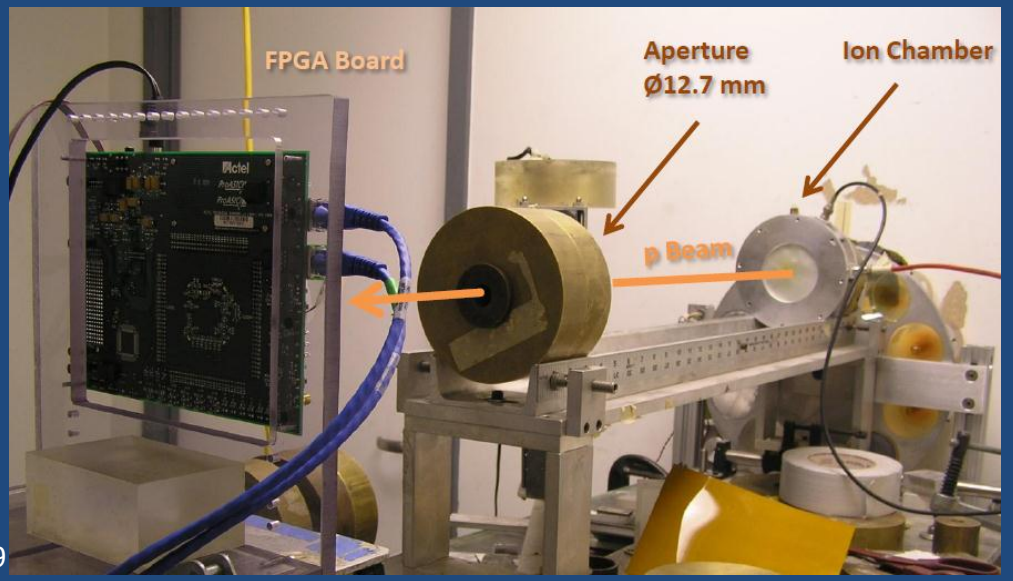


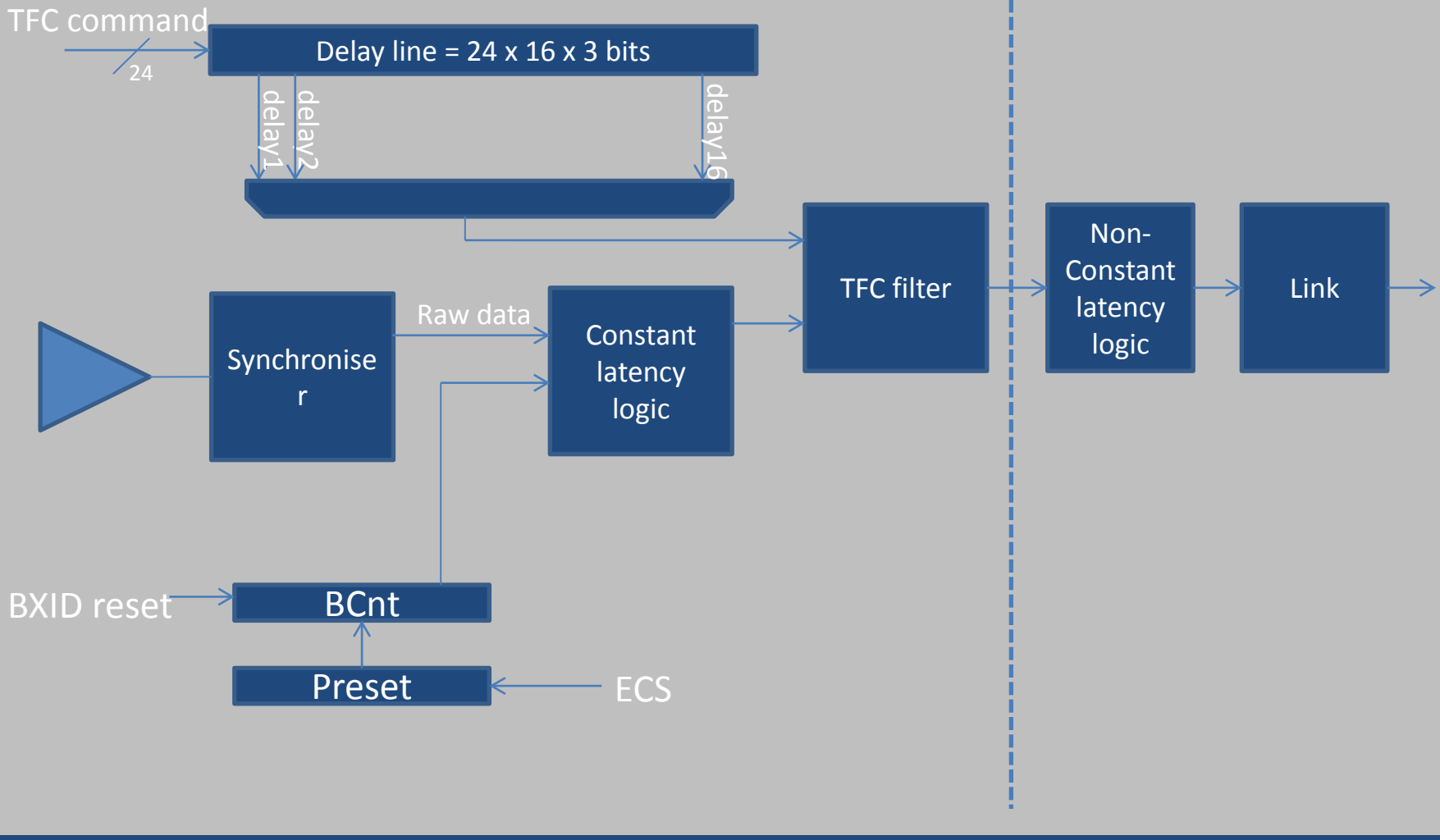
ICECAL in AMS 0.35μm SiGe

Common developments

ACTEL Flash FPGA for front-end modules

- Advantages over ASICs: re-programmable!!!
- Can they survive the radiation.....?
- Irradiation programme on-going on A3PE1500




TFC command
24
Delay line = 24 x 16 x 3 bits
delay1
delay2
delay16
TFC filter
Non-Constant latency logic
Link
Synchroniser
Raw data
Constant latency logic
BXID reset
BCnt
Preset
ECS