LHCb upgrade

Electronics Architecture Review

Introduction

LHCb upgrade plan

At L = 2 x 10^{32} $cm^{-2}s^{-1}$, beyond 5 years running, statistics don't improve

Big statistical improvement if:

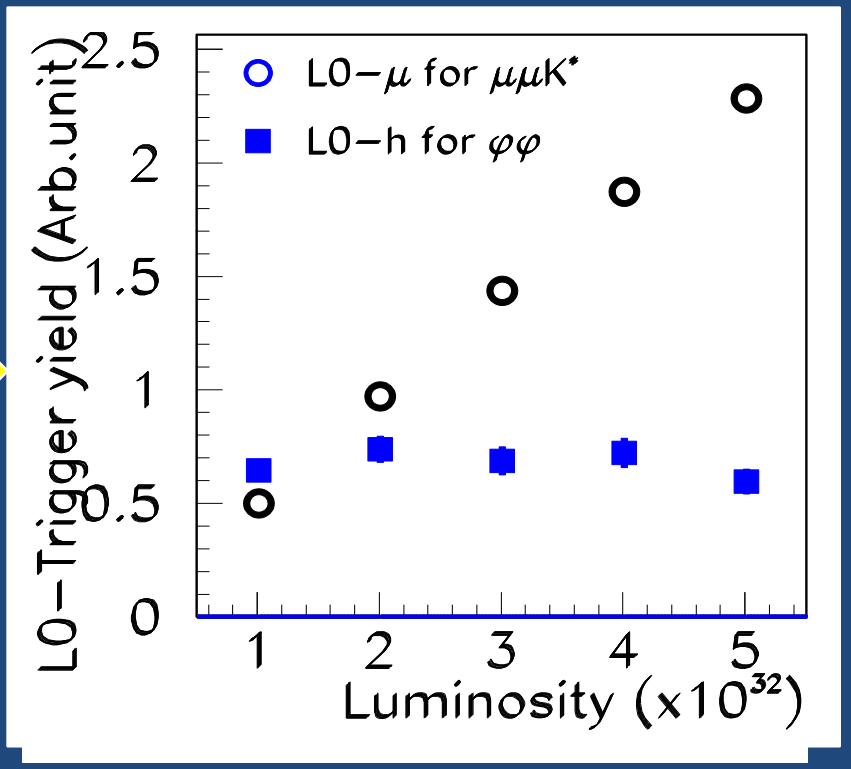
- **increase L to 1 x 10^{33}, AND**
- **improve efficiency of trigger algorithms**

BUT ..... current L0 trigger:

rate & latency limited by electronics

BUT.... efficient trigger decisions require:

- **long latencies**
- **computing power**
- **data from many (all) sub-detectors (momentum, impact parameter .....)**



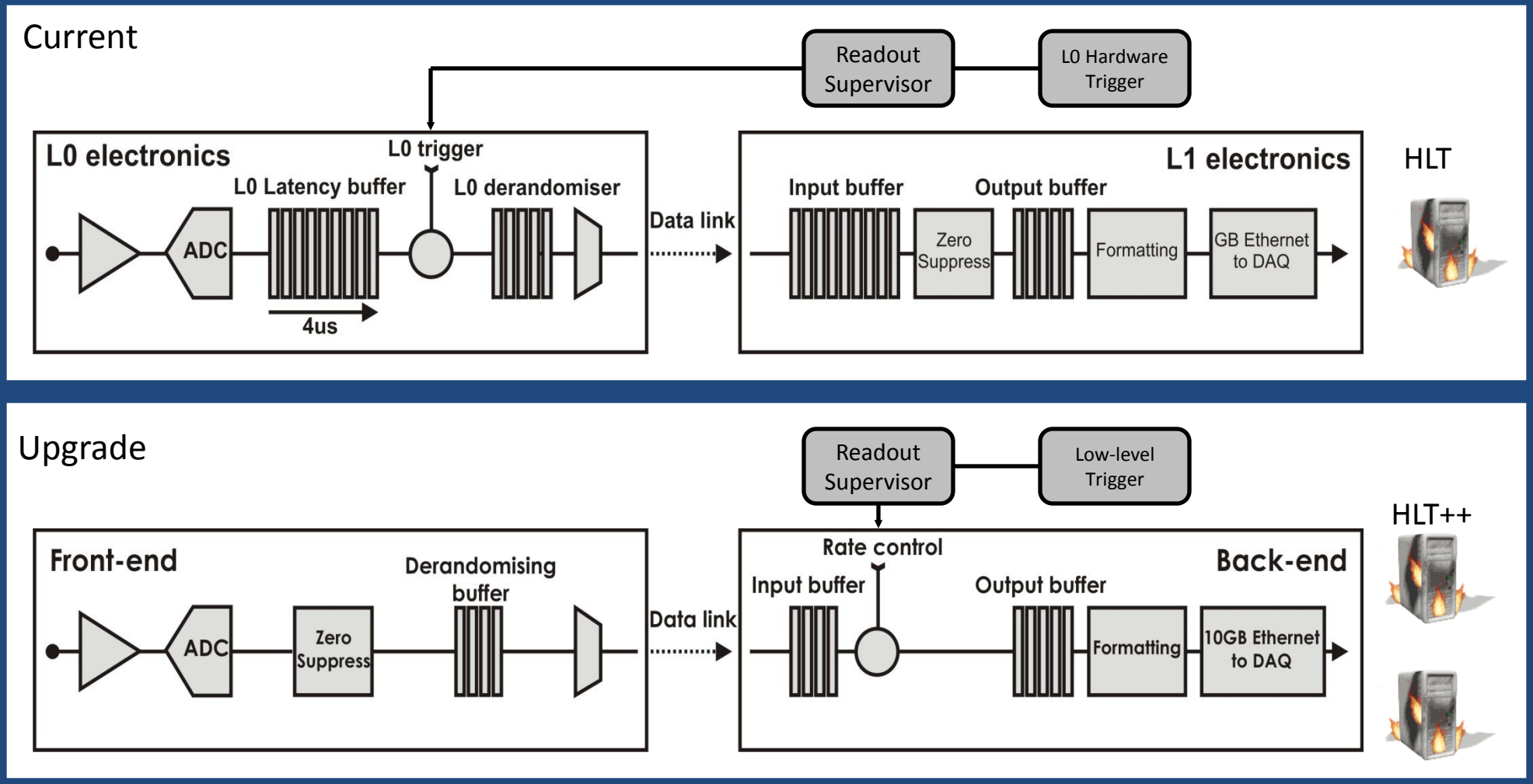
⇒ **upgrade electronics + DAQ architecture goal is 2018**

LHCC-2008-007 (EoI)

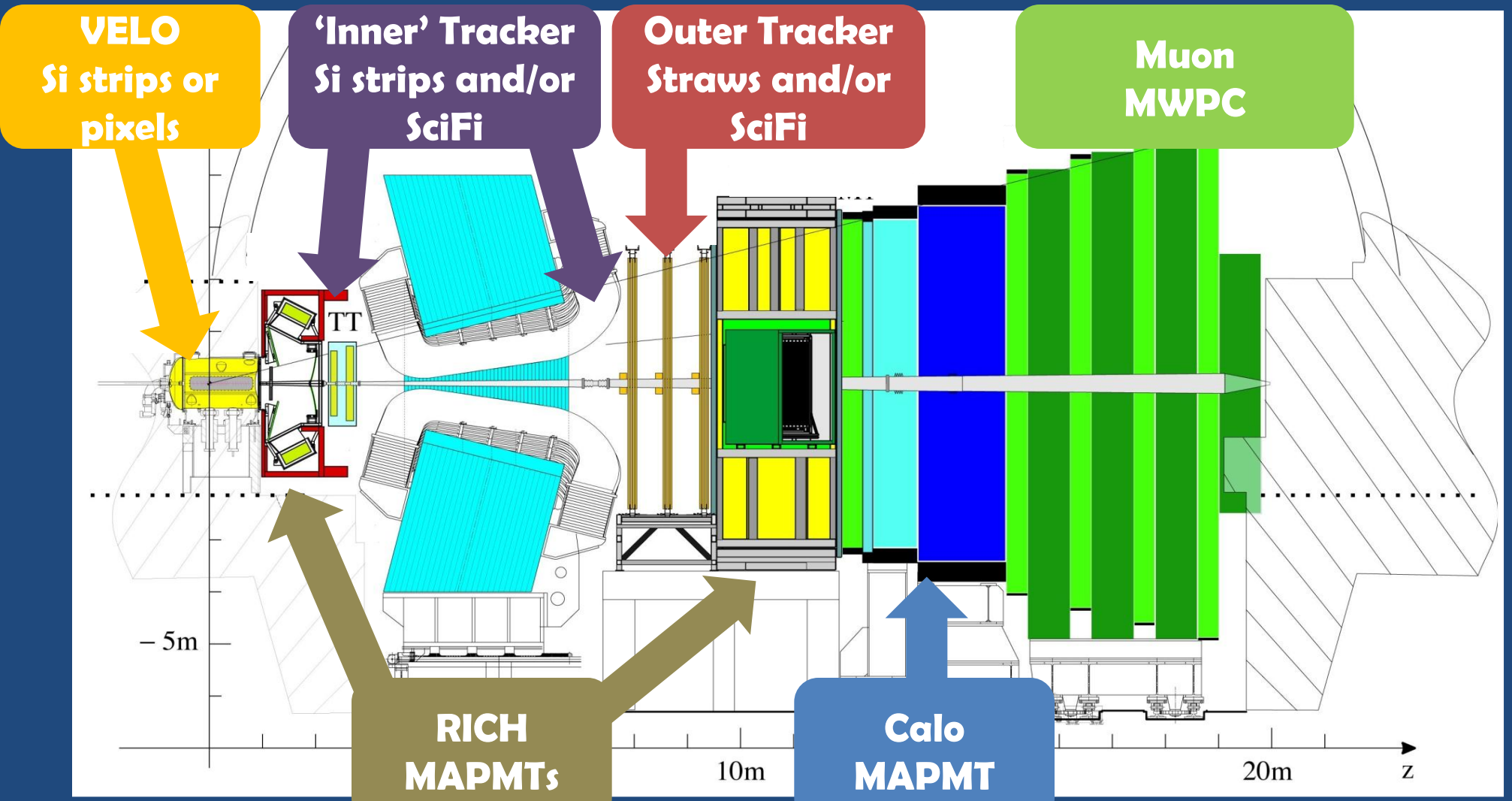
LHCC -2011-001 (LoI)

Electronics architecture

Front-end electronics: transmit data from every 25ns BX



LHCb sub-systems



Sub-Detector electronics developments

Sub-system	FE-analog	FE-digital
Velo pixel	new ASIC (VeloPix)	new ASIC (VeloPix)
Velo strip	new ASIC (SALT)	new ASIC (SALT)
RICH	new ASIC (CLARO) or MAROC	ACTEL?
Silicon Tracker	new ASIC (SALT)	new ASIC (SALT)
SciFi	new ASIC (PACIFIC)	new ASIC (PACIFIC)
OT	existing ASIC (ASDBLR)	ACTEL
Calo	new ASIC (ICECAL)	ACTEL

....and new front-end hybrids, boards modules etc for everyone !!

Implementation

Try to optimise:

- Cost
- Manpower
- Time (development, production, installation)

1. Re-use existing electronics & infrastructure as much as possible
2. Develop common solutions for use by all sub-detectors

Example: data links

Use GBT @ 4.8 Gbit/s
~ 12,000 links across all sub-detectors

Timescale

Ultimate Target is LS2:

Install new electronics at point 8 in 2018 (& new detectors)

Ready for data taking in 2019

Prepare as much as possible before (LS1 & technical stops)

- eg cabling infrastructure
- mini-system tests with BE boards & mini-network

Shorter term plans:

Complete specifications by end 2012

Sub-detectors continue implementation

Architecture reviews of sub-detector electronics through 2013

Reviewers mandate

Assess feasibility of architecture
FE, BE, TFC, LLT, ECS, DAQ interface

Recommendations (eg system robustness)

Comment on reliance on 'common' components
(eg GBT, Versatile Link, DC-DC, LVPS)

Comment on technology choices (eg Actel, ATCA)

Comment on timescale (if possible....)

Please write a short report, to be used internally in LHCb

Review structure

Front-end: Ken
Back-end: Jean-Pierre

TFC: Federico
ECS: Clara

DAQ interface: Rainer
Infrastructure: Laurent