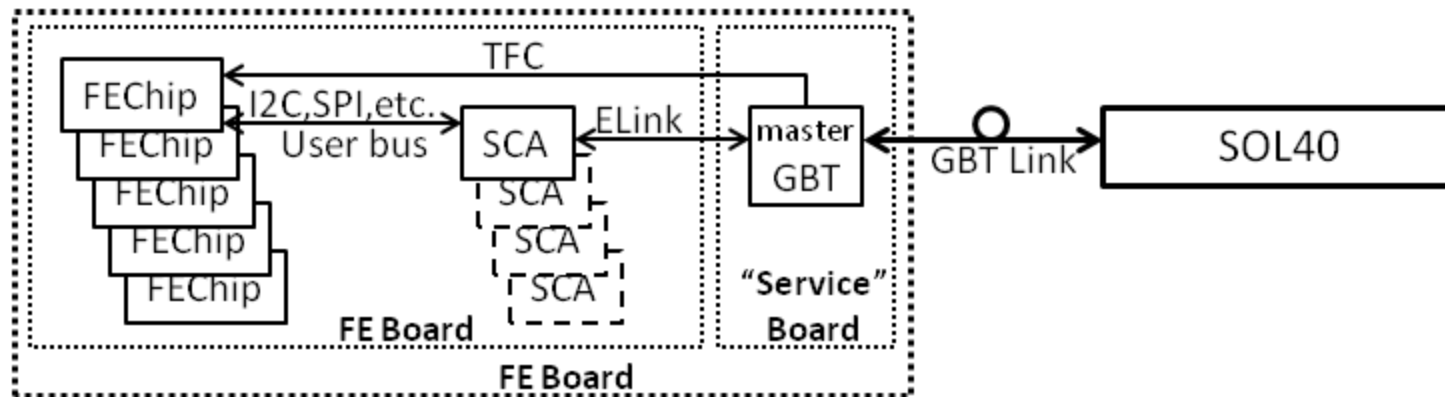


Experiment Control System & Electronics Upgrade

Clara Gaspar, December 2012

- ECS Design doesn't change (in principle)
 - Same tools:
 - | Communications: DIM
 - | Supervision: WinCC-OA (ex-PVSS II)
 - | Sequencing and Automation (FSM): SMI++
 - Same philosophy:
 - | Generic tools to describe the hardware (FwHw)
 - | Board Types -> "chips" -> registers => Boards
 - | Operation tools to Configure/Monitor boards
 - | "Recipes" for different configuration modes
 - | Stored in Configuration DB
 - New electronics will be interfaced like before

Interface to FE Electronics



Two Architectures envisaged:

- | FE electronics in one single FE board
- | FE electronics accessed via a "Service" board (masterGBT <-> SCA via "long" ELink)

■ Interface to the FE Chips

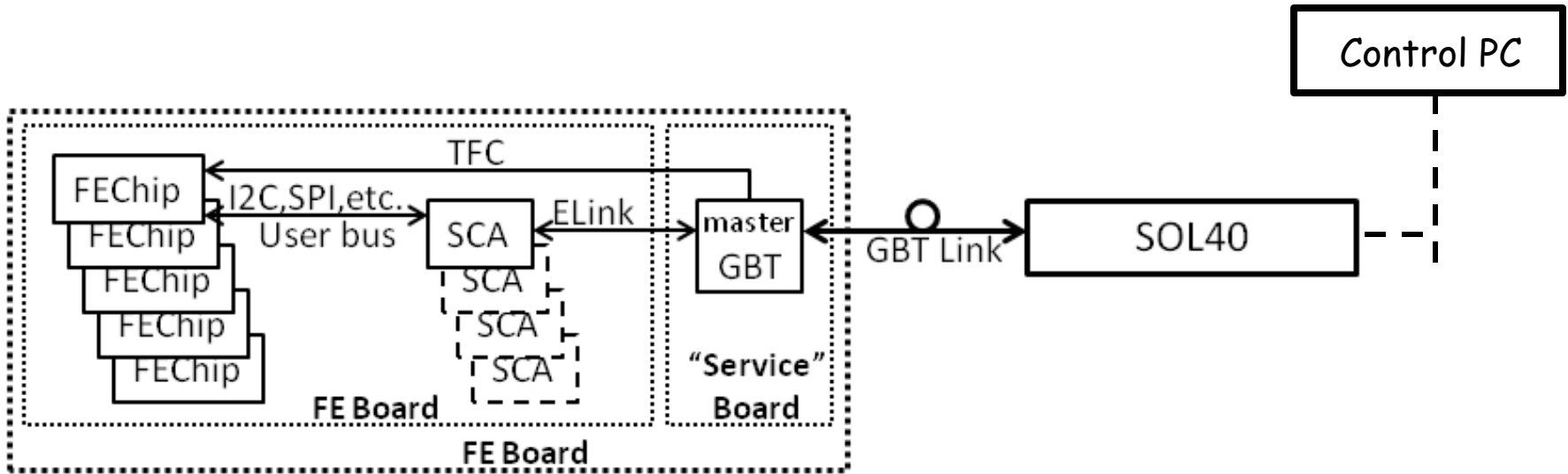
■ The GBT-SCA provides the following protocols:

- | 16 x I2C master controllers
- | 1 x JTAG master controller
- | 32 x ADC channels (multiplexed)
- | 1 x Memory bus (32 bits) controller
- | 4 x PIA (Parallel Interface Adapter) controllers
- | 1 x SPI (Serial Peripheral Interface) bus
- | 4 x DAC channels

■ Recommended protocols (for bulk transfers) are:

- | I2C
- | SPI using independent chip selects
(daisy chained SPI not allowed)

FE Addressing



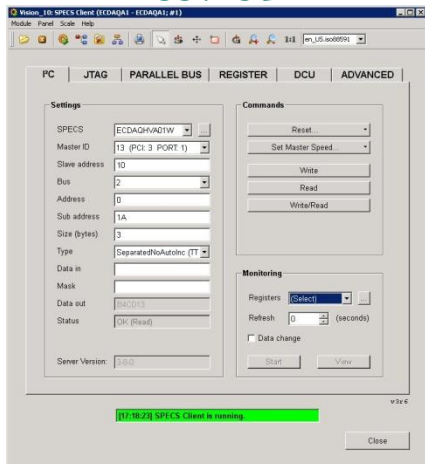
■ FE Chip Register Address:

$\langle \text{SOL-}ip \rangle \langle \text{GBT-}i \rangle \langle \text{SCA-}j \rangle \langle \text{ProtoCode} \rangle \langle \text{I2C-}k \rangle \langle \text{I2C-add} \rangle [\langle \text{I2C-s.add} \rangle]$

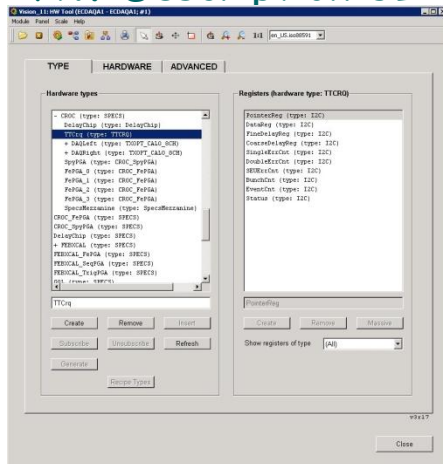
←———— fixed —————→
←———— variable —————→

ECS FE Dataflow

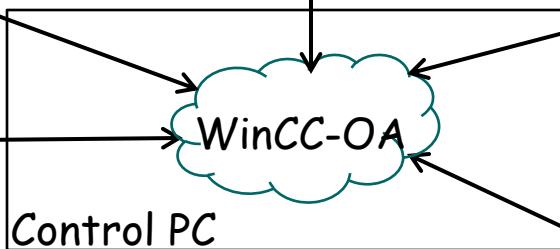
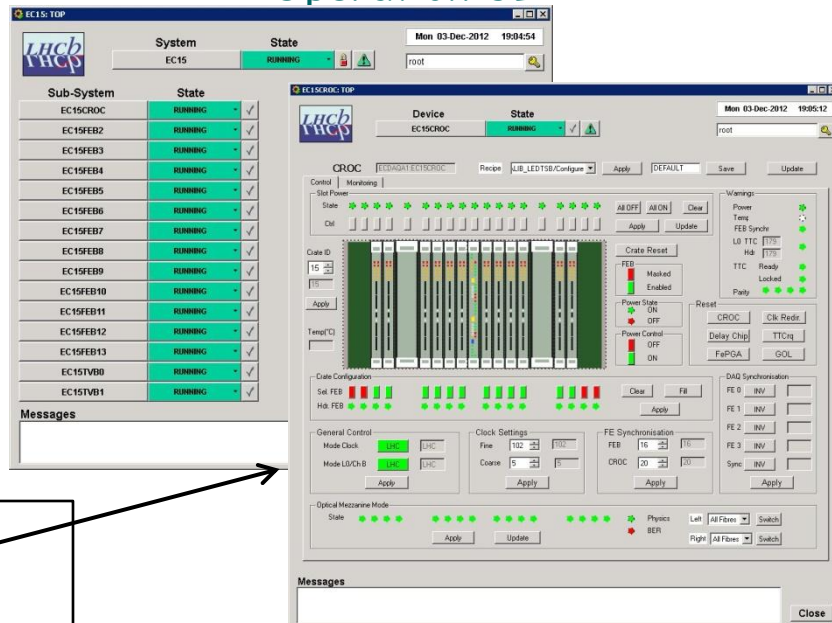
Test UI



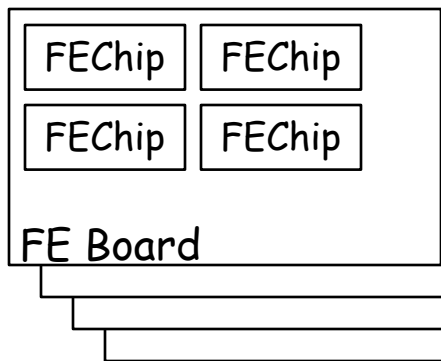
HW Description UI



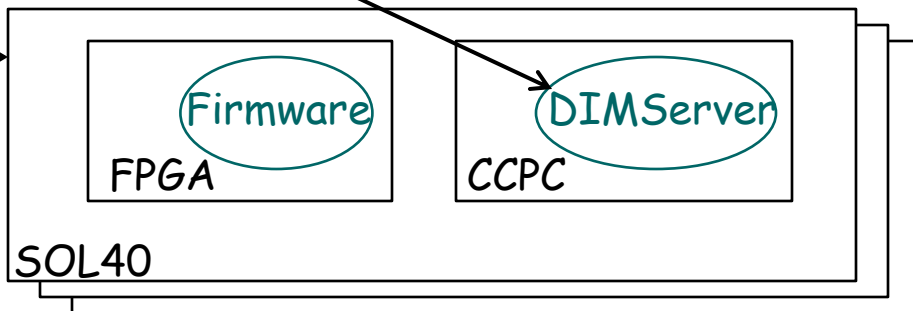
Operation UI



Control PC



GBT Link



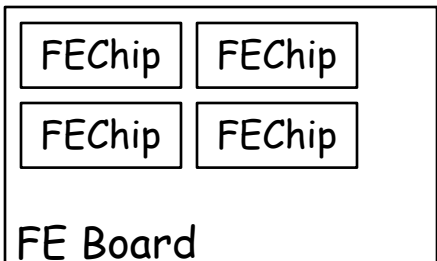
Clara Gaspar, December 2012

- Will be centrally provided:
 - The FPGA firmware for the SOL40 board
 - | Will prepare, send and receive the GBT-SCA frames for the various user protocols
 - | Should take load away from CCPC as much as possible
 - Low-level libraries and command-line tools for the CCPC in the SOL40
 - | Will allow accessing the different FE chips
 - A DIM server running on the SOL40 CCPC
 - | Will implement higher-level commands to configure and monitor the FE chips
 - A WinCC-OA component
 - | Providing the high-level description and access of all electronics components

ECS Dataflow

Test UI

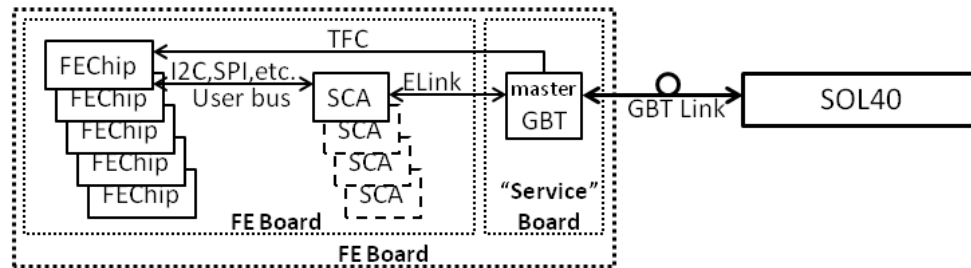
REGISTER	TYPE	DATA
ECDAQ1:EC15CROC.TTCrq.BunchCnt	I2C	7208
ECDAQ1:EC15CROC.TTCrq.CoarseDelayReg	I2C	05
ECDAQ1:EC15CROC.TTCrq.DataReg	I2C	05
ECDAQ1:EC15CROC.TTCrq.DoubleErrCnt	I2C	FF
ECDAQ1:EC15CROC.TTCrq.EventCnt	I2C	1E760D
ECDAQ1:EC15CROC.TTCrq.FineDelayReg	I2C	C8
ECDAQ1:EC15CROC.TTCrq.PointerReg	I2C	C8
ECDAQ1:EC15CROC.TTCrq.SEUErrCnt	I2C	03
ECDAQ1:EC15CROC.TTCrq.SingleErrCnt	I2C	FFFF
ECDAQ1:EC15CROC.TTCrq.Status	I2C	F0



1st Steps

- Understand the needs
- Identify bottlenecks
- Questionnaire Sent:

1. Sub-detector:
2. Number of GBT Links:
3. Number of FE Boards (/Service Boards):
4. Number of SCA chips per masterGBT:
5. Number of User buses per SCA chip:
6. Type of User buses used:
7. Number of "registers" per FE Board:
8. Data volume per FE Board for configuration:
9. Data volume per FE Board for monitoring (and how often):



■ Configuration and Monitoring speed

- Is not just data size / bandwidth

- Depends on:

- | How the data is distributed, for ex.:

- ul>- | A few large registers or many small ones

- | Are blocking operations needed, for ex.:

- ul>- | A register needs to be set and read-back before configuring the next one

- ul>- | or read-modify-write operations that need to be done by the back-end

- | Which user protocol is used and how it is used, for ex.:

- ul>- | Some I2C devices needed an extra I2C operation to write a sub-address before the block of data could be written

- ul>- | Some did not implement auto-increment so block transfer could not be used

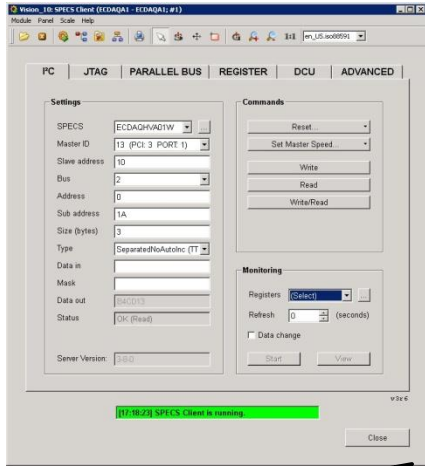
- Try to influence hw design early enough...

BE Board Interface

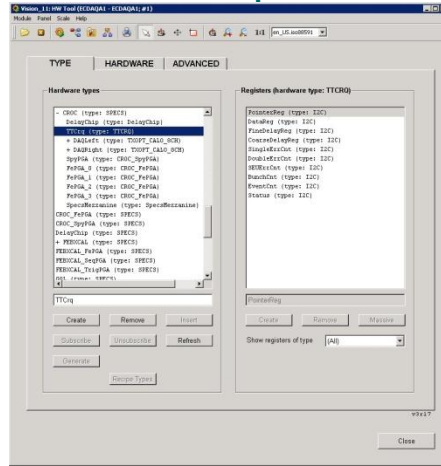
- Physically only one board type (ATCA40/AMC40):
TELL40, S-ODIN, TRIG40, SOL40
 - But logically different types (different "registers")
- Similar Tools will be provided centrally:
 - Low-level libraries and command-line tools for the CCPC in the board
 - Will allow accessing the different registers (PCIexpress)
 - A DIM server running on the CCPC
 - Will implement higher-level commands to configure and monitor the board components
 - A WinCC-OA component
 - Providing the high-level description and access of all electronics components

ECS BE Dataflow

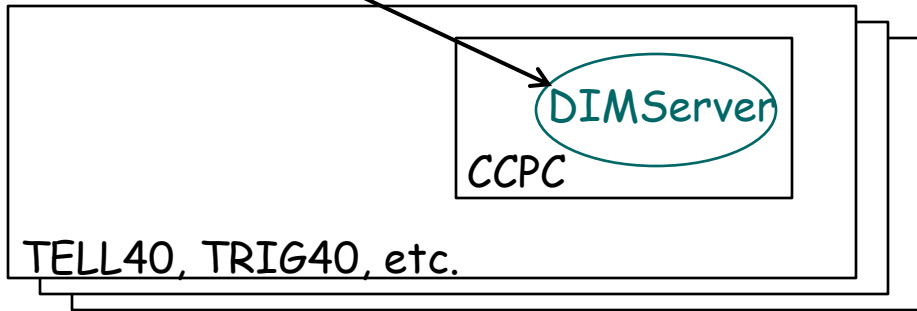
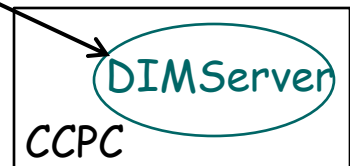
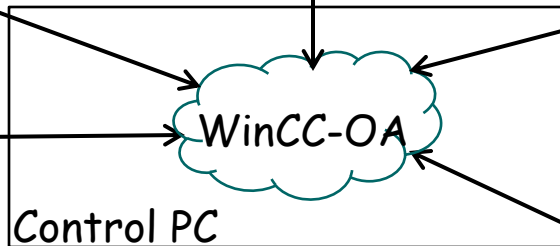
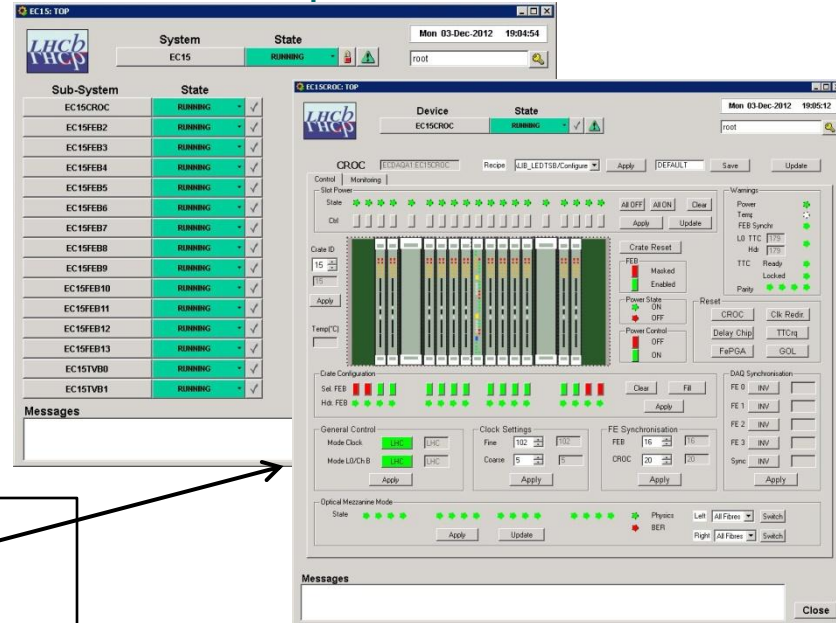
Test UI



HW Description UI



Operation UI



Infrastructure Control

- The control & monitoring of the crates (& boards) will also be provided centrally
 - ATCA provides a standard for the control and monitoring of power, voltages, temperatures etc.:
-> IPMI
 - A WinCC-OA component will be provided.