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1

DATACENTER IMPERATIVES IN THE NEW ERA

HERBERT CORNELIUS
TECHNICAL DIRECTOR ADVANCED COMPUTING, EMEA

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IT
WOVEN INTO THE
FABRIC OF SCIENCE & BUSINESS

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DATACENTER EVOLUTION

AND NOW....

DATACENTER
1990 - 2000
"DIVERSITY OF SYSTEMS"

DATACENTER
2000 - 2010
"VIRTUALIZED RESOURCE POOLS"

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DATACENTER AS A SYSTEM

FACILITIES NETWORKING HARDWARE SOFTWARE OPERATIONS

ENABLING *"IT as a SERVICE"*
seamlessly integrated system architecture operating as one resource

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IMPERATIVES

Competitiveness
Performance, Efficiency & Agility

Convergence
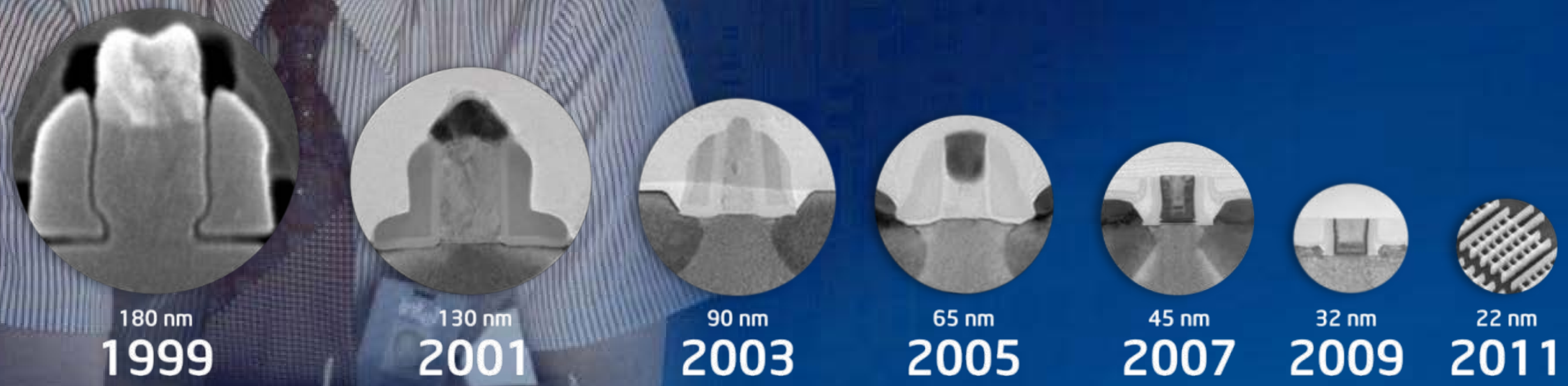Between Compute, Storage, Networking

Capabilities
To Unlock Insights of Big Data

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TRANSFORMING THE ECONOMICS OF HPC

Predictable Silicon Track Record
Executing to Moore's Law
Enabling new devices with higher performance and functionality while controlling power, cost, and size
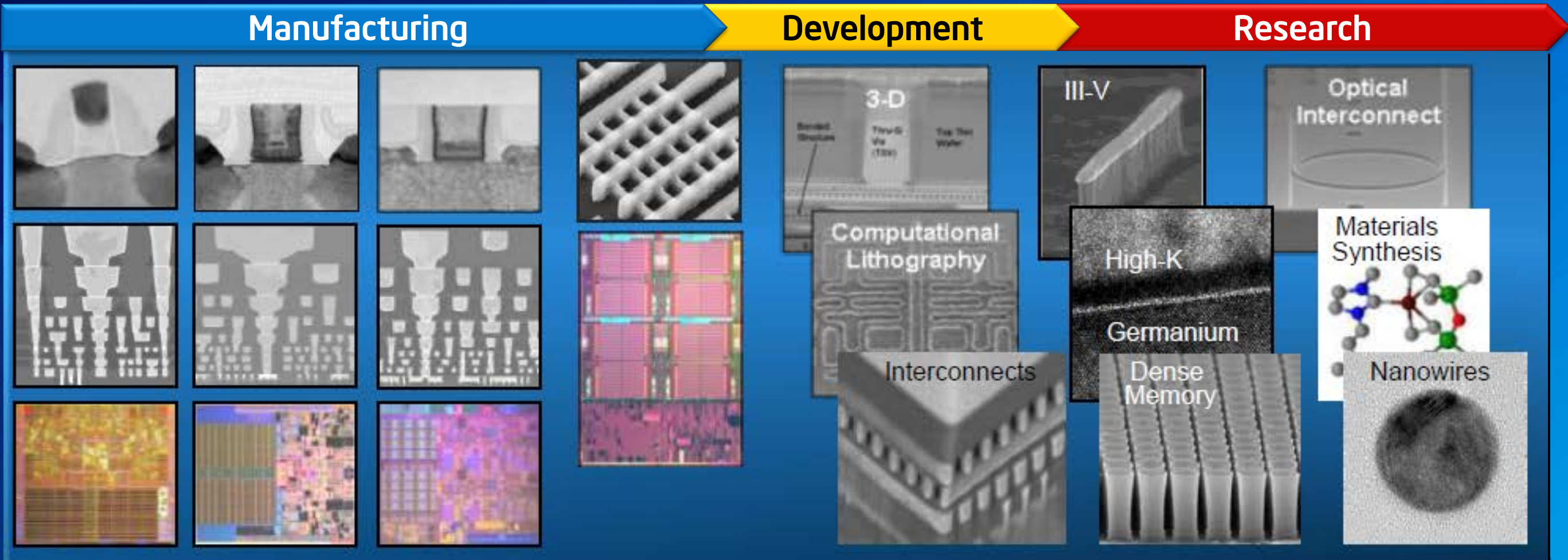

| 180 nm | 130 nm | 90 nm | 65 nm | 45 nm | 32 nm | 22 nm | On Track 14nm |
| 1999 | 2001 | 2003 | 2005 | 2007 | 2009 | 2011 | |

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PROCESS TECHNOLOGY RESEARCH @ INTEL

| 65nm 2005 | 45nm 2007 | 32nm 2009 | 22nm 2011 | 14nm 2013** | 10nm 2015** | 7nm 2017** | Beyond 2019+ |

Manufacturing → **Development** → **Research**

**projected

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INTEGRATION

Example: Intel® Architecture
More Performance and New Capabilities

integrated
Integer ALU

+ integrated
Floating-Point
+ integrated
Cache

+ integrated
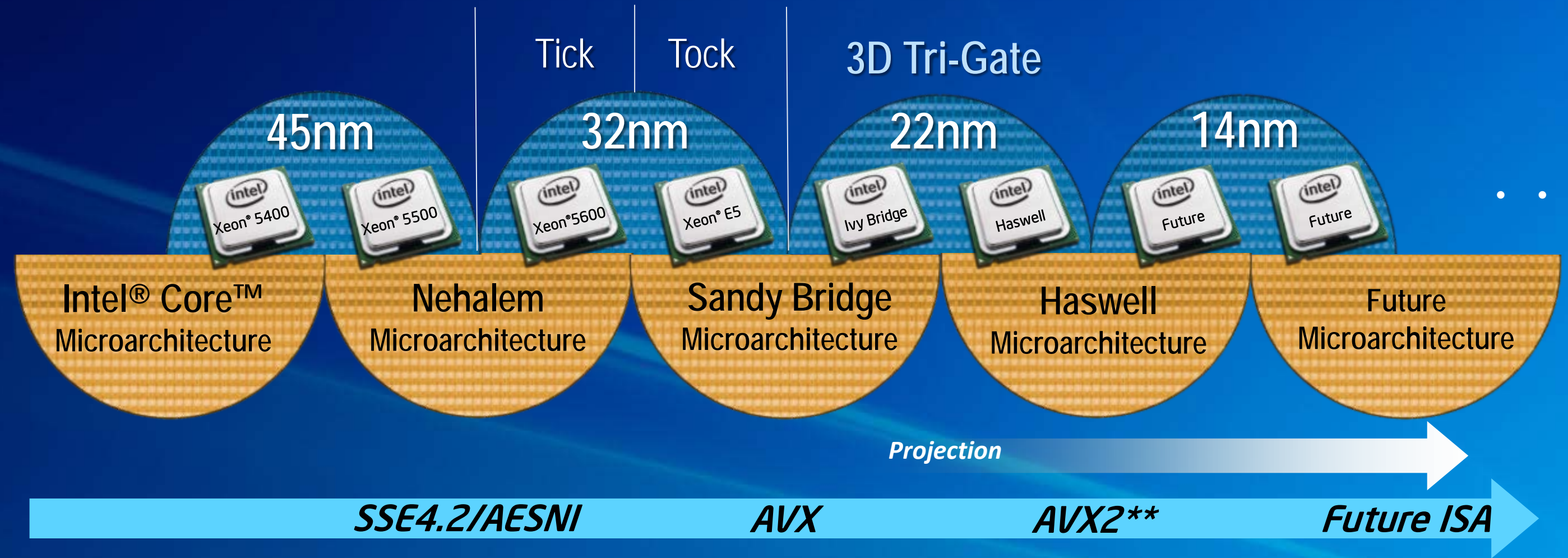SIMD
+ Multi-Core

+ integrated
Memory
Controller

+ integrated
Graphics
+ integrated
I/O

⭐ New Instructions

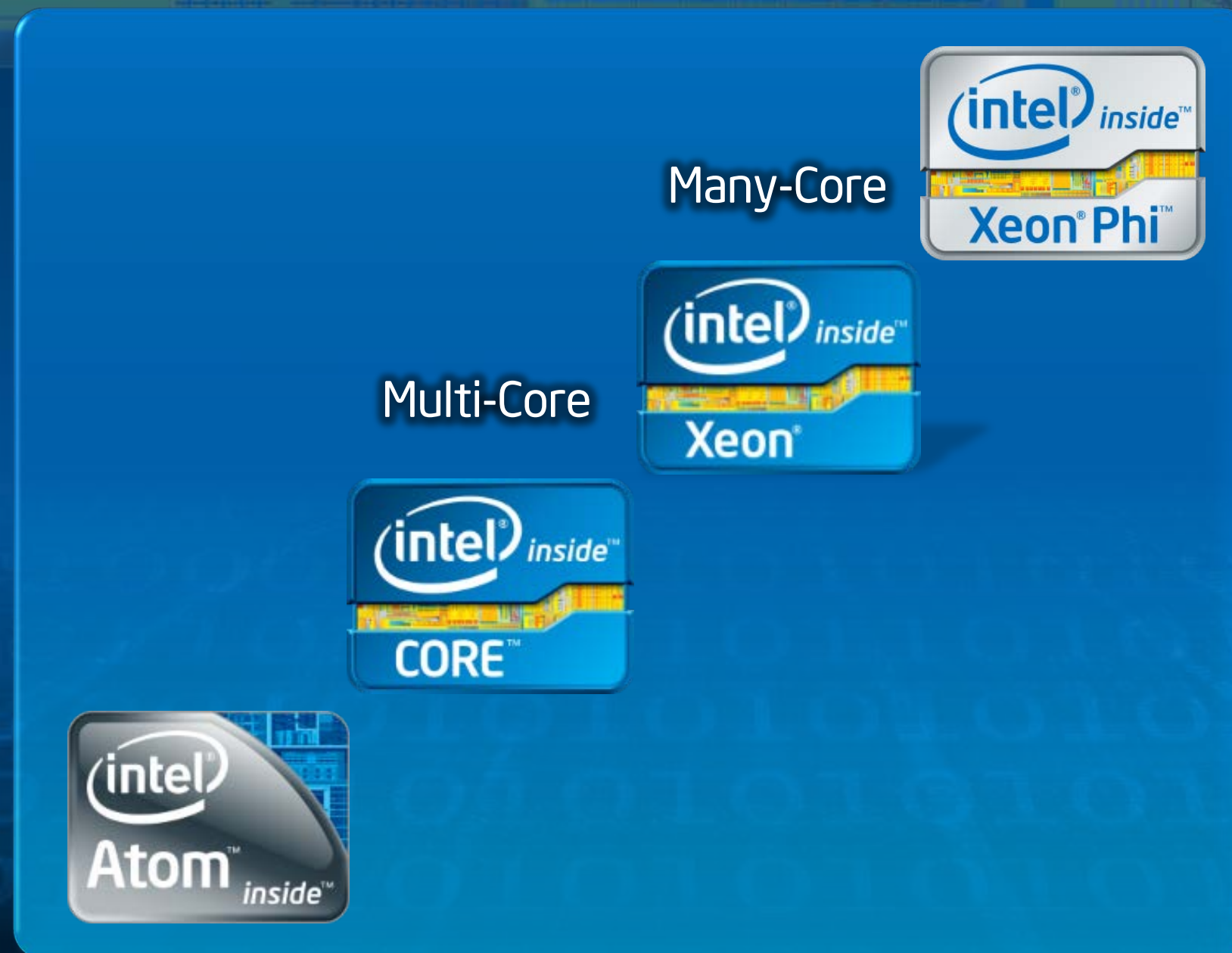IT requirements for the next generation research infrastructures workshop, CERN, 01-February-2013.

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TICK-TOCK DEVELOPMENT CYCLES
Integrate. Innovate.

Tick   Tock   3D Tri-Gate

45nm   32nm   22nm   14nm

Xeon® 5400   Xeon® 5500   Xeon® 5600   Xeon® E5   Ivy Bridge   Haswell   Future   Future

Intel® Core™ Microarchitecture   Nehalem Microarchitecture   Sandy Bridge Microarchitecture   Haswell Microarchitecture   Future Microarchitecture

Projection

SSE4.2/AESNI   *AVX*   *AVX2***   *Future ISA*

**Intel® Architecture Instruction Set Extensions Programming Reference, #319433-012A, FEBRUARY 2012

Potential future options, subject to change without notice.

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FROM TERAFLOPS TO MILLIWATTS

iA

Many-Core

intel inside™
Xeon Phi™

Multi-Core

intel® inside™
Xeon®

intel® inside™
CORE™

intel
Atom™ inside™

Energy
Efficient

INTEL

EFFICIENCY EXAMPLE AT SCALE

SUPERCOMPUTING

Top 500*
(1997 – 2012)

1500X
Performance

4X
Power Increase

100X
Reduction
In cost per
FLOP

Driven by Moore's Law & Architecture Innovation

Source: Intel Analysis / Top500

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WORLD RECORD!
"Beacon" at NICS

Intel® Xeon® + Intel Xeon Phi™ Cluster
Most Power Efficient on the
TOP500 List Nov'2012:

2.449 GFLOPS / Watt
70.1% Efficiency

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INTEL TERASCLAE RESEARCH

MANY-CORE COMPUTING

3D STACKED MEMORY

SILICON PHOTONICS

Teraflops
of computing power
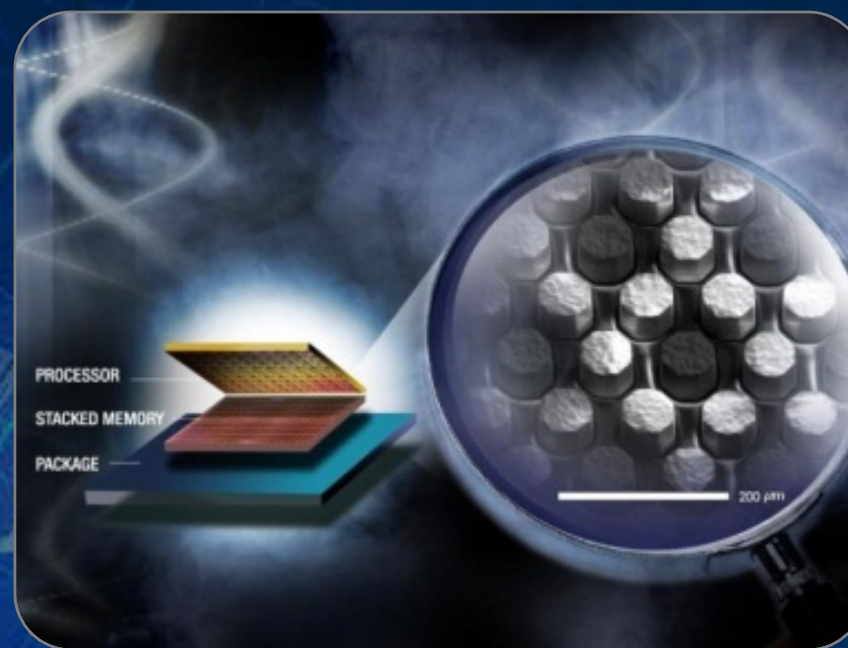
Terabytes
of memory bandwidth
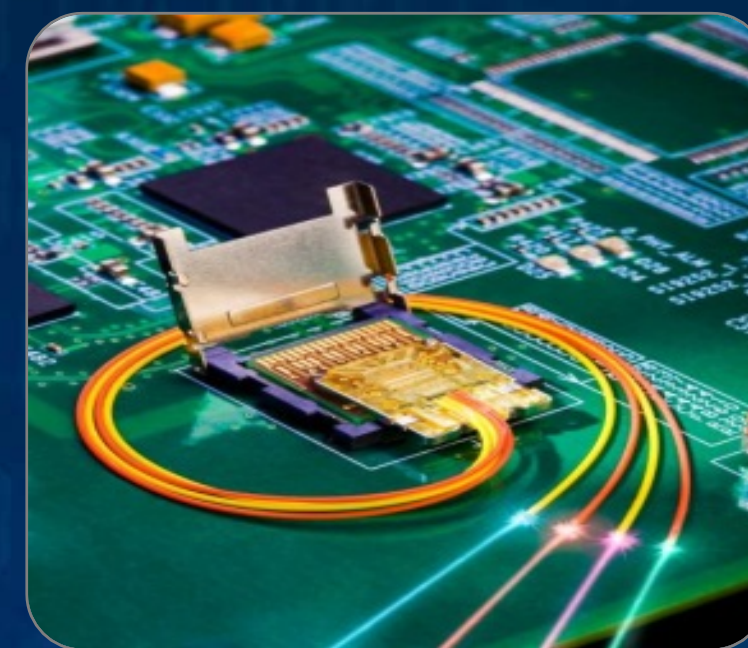
Terabits
of I/O throughput

Future vision, does not represent real products.

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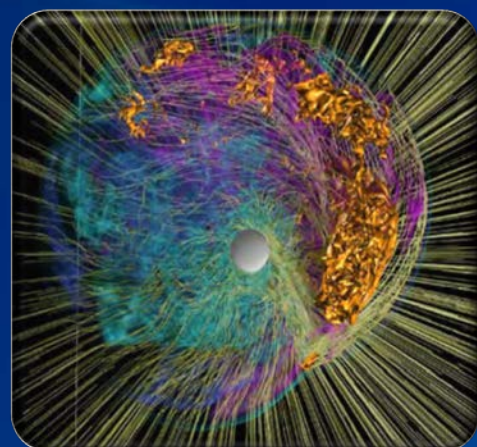# ASSUMING EXASCALE COMPUTING AT 20MW ... BY 2020
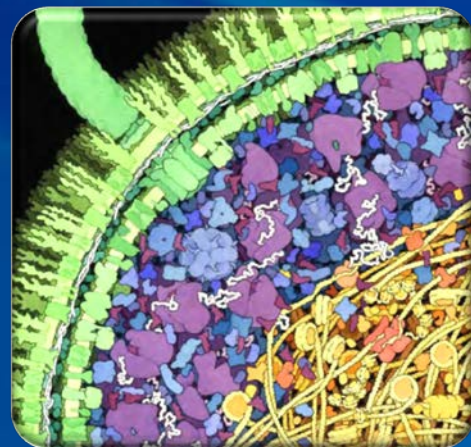
New Forms of Energy
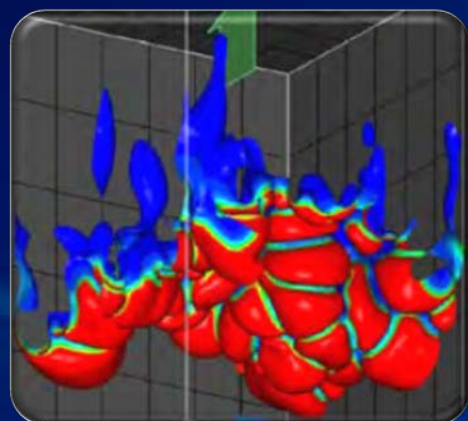
Ecological Sustainability

Space Exploration

Medical Innovation

And many others....

Data Center Sized <u>Exascale</u> System
Lower Volume
Higher Cost
20MW

Rack Sized <u>Petascale</u> System
"Mainstream"
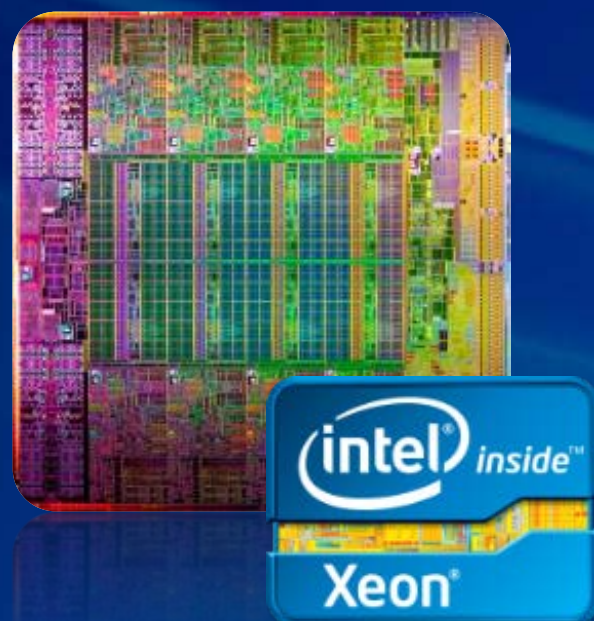**20KW**

Embedded <u>Terascale</u> System
Higher Volume
Lower Cost
20W

For illustration and concept only.

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HPC:
THE PATH TO EXASCALE

Processors
Intel® Xeon® Processor

Co-Processor
Intel® Many Integrated Core
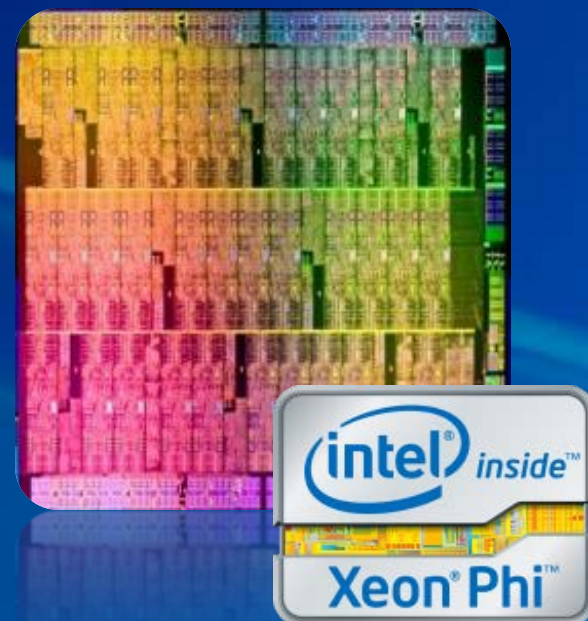
Fabrics

Software

Scalability

Parallelism

HPC:
THE PATH TO EXASCALE (CONT.)

Memory & Storage

Networking

Reliability & Resiliency

Power Management
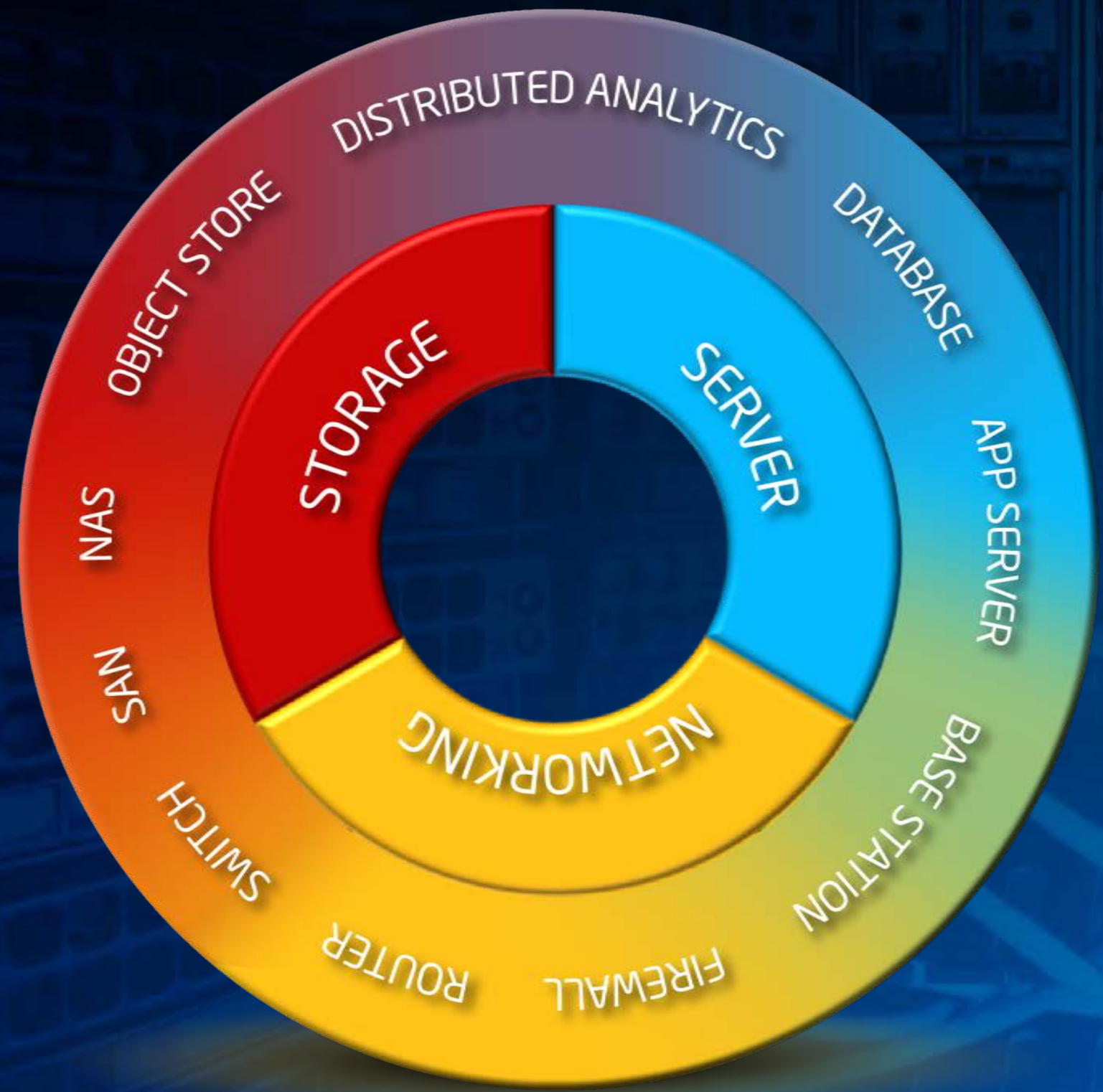
Energy Efficiency

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HOLISTIC OPTIMIZATION

TCO

AGILITY

Facilities

Network

Rack

Server

Silicon

Application

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The Server, Network, Storage
LINES ARE BLURRING

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NEW STORAGE OPTIMIZATIONS

DRIVEN BY
COMPUTATION
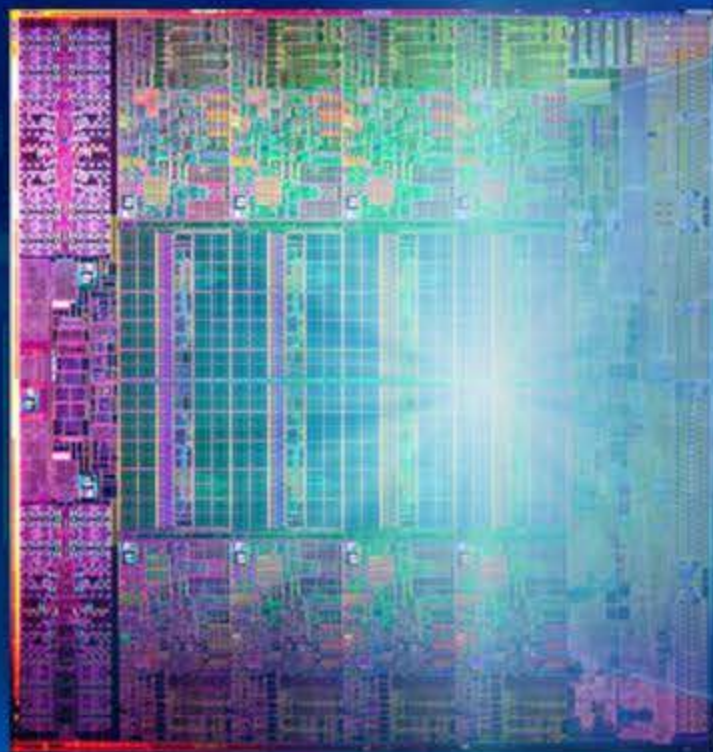
Intelligent Tiering

Real Time Compression

Thin Provisioning

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NON VOLATILE MEMORY

Changing The Game In Datacenter Storage

4X More IOPs vs. HDD

90% LOWER POWER CONSUMPTION

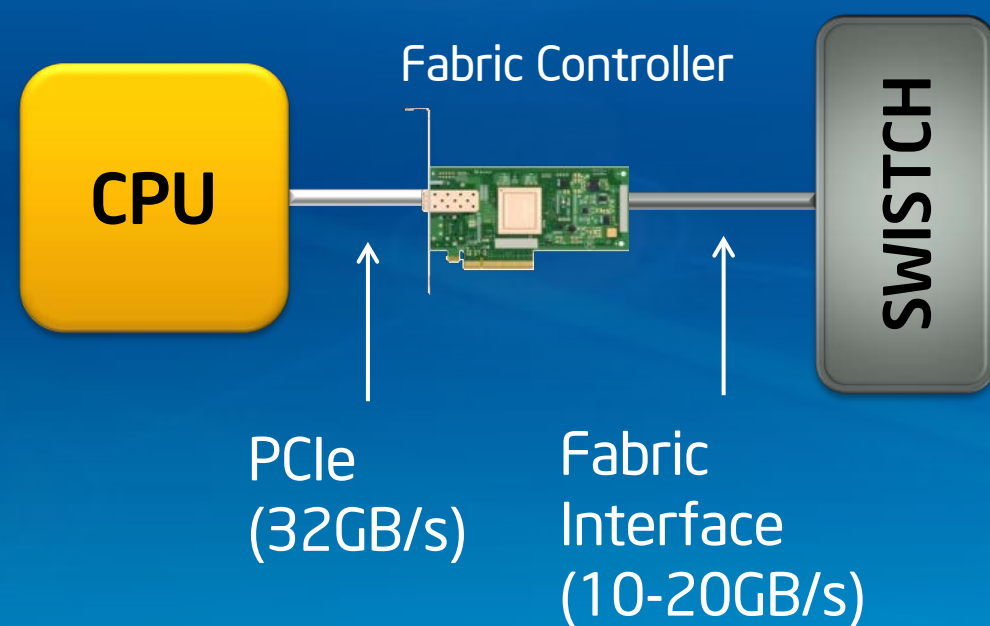## Ideal For Accelerating I/O & Throughput-bound Applications

Source: SNIA, 2011

intel

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NETWORK BANDWIDTH

10GbE is required to make the transition to scale - evolving

to 40GbE to 100GbE

... and beyond

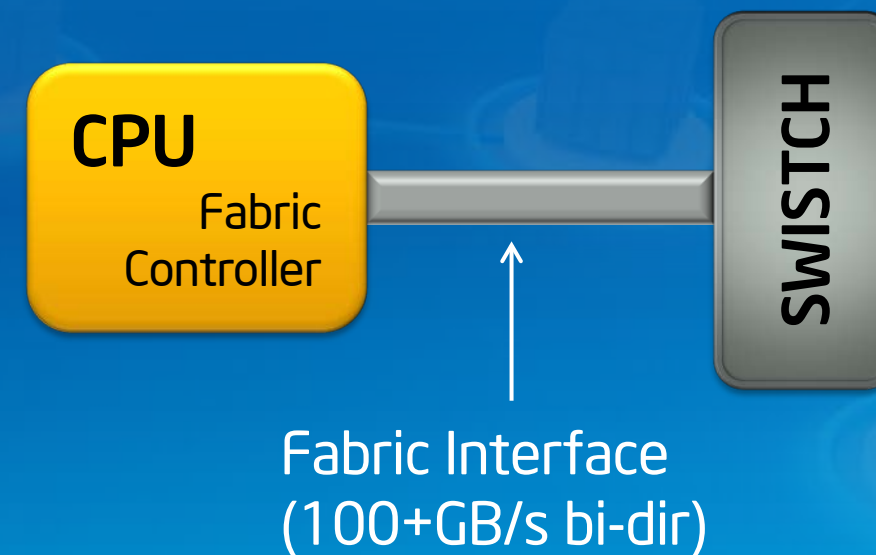Vision concept, potential future options, subject to change without notice.

10GBASE-LR

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FABRICS INTEGRATION

TODAY

CPU

Fabric Controller

SWISTCH

PCIe
(32GB/s)

Fabric
Interface
(10-20GB/s)

FUTURE

CPU
Fabric
Controller

SWISTCH

Fabric Interface
(100+GB/s bi-dir)

Benefits: *Performance . Scalability . Efficiency . Power . Space . Costs*

Vision concept, potential future options, subject to change without notice.

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SOFTWARE DEFINED NETWORKS

Agility And Scale for Next Gen Networks

Network Intelligence

API

Switch

API

Switch

API

Switch

Network Intelligence

Switch

Physical Switch

Virtual Switch

DISCRETE FIXED FUNCTION

VIRTUALIZED SW DEFINED

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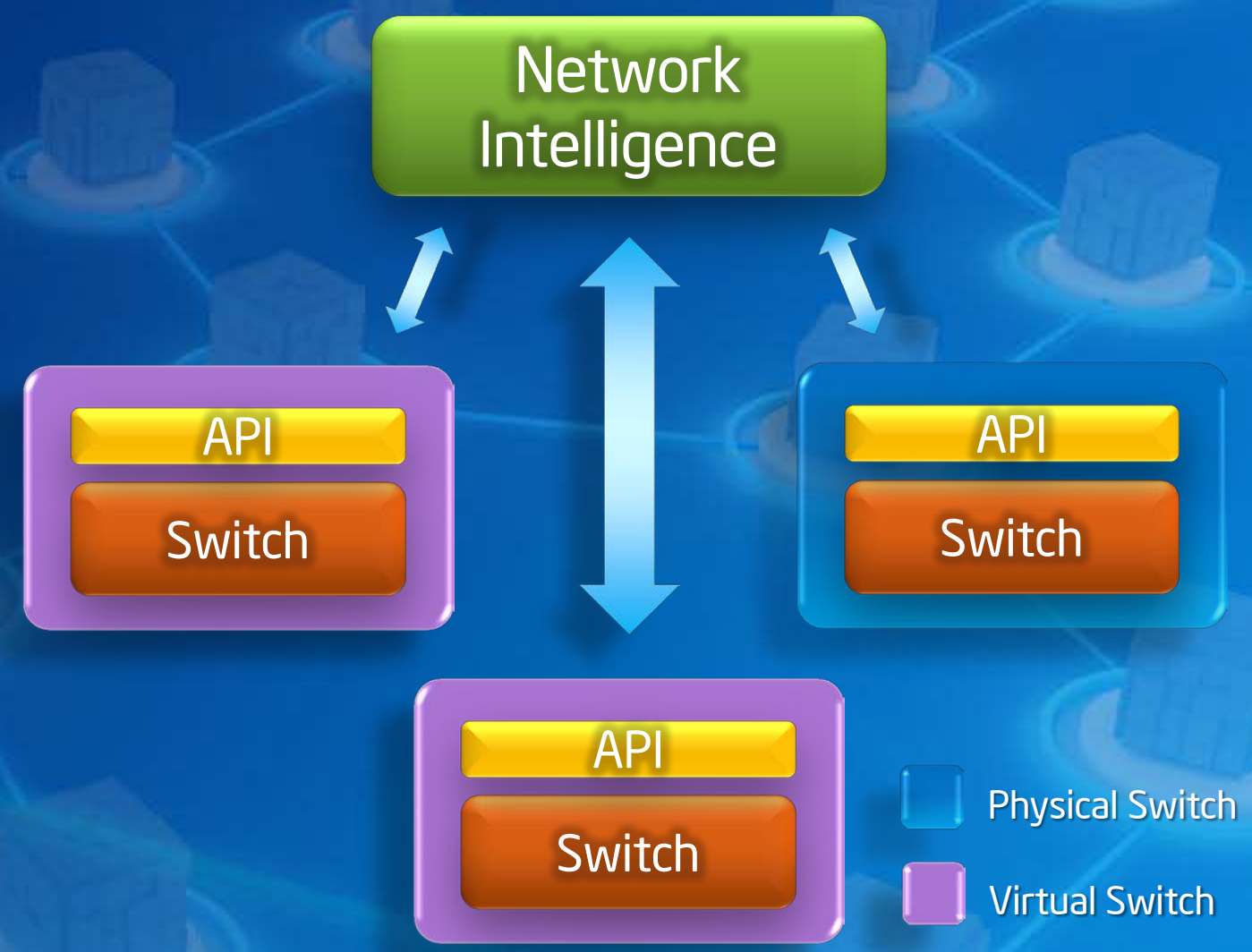
DATA CENTER RACK DESIGN EVOLUTION

- Distributed Switches
- Optical Interconnects
- Storage Appliances
- Shared I/O

Step 1: Physical
Sheet Metal Reduction
Consolidated Power Supply

Step 2: Distributed IO
Switching and Storage
Disaggregation

Step 3: Subsystem
Compute, Memory & I/O
Disaggregation

BIG DATA
Challenges and Opportunities

MACHINE & SENSOR GENERATED

HUMAN GENERATED

BUSINESS GENERATED

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IT IS TRANSFORMING

Convergence For

Performance, Efficiency & Agility

Datacenter Is The System

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INNOVATION & LEADERSHIP
FOR THE ROAD AHEAD

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Thank You.