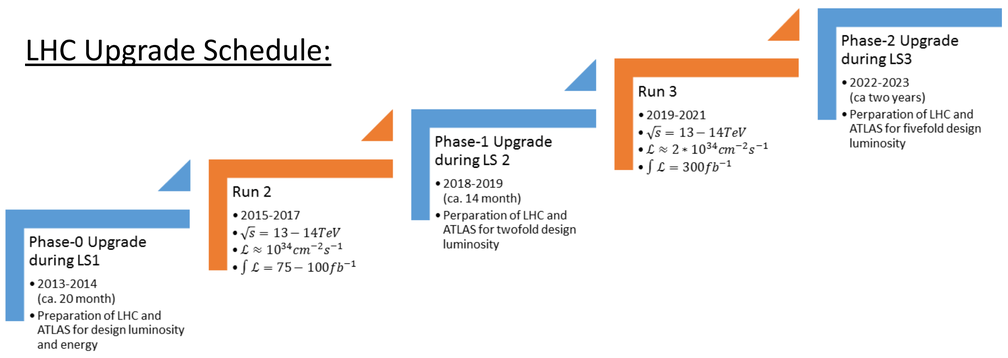
FPGA-based 10-Gbit Ethernet Data Acquisition Interface for the Upgraded Electronics of the ATLAS Liquid Argon Calorimeters

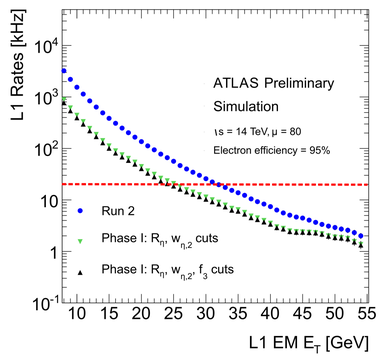
J. Philipp Grohs on behalf of the ATLAS Liquid Argon Calorimeter group • philipp.grohs@tu-dresden.de

Motivation

LHC Upgrade Schedule:

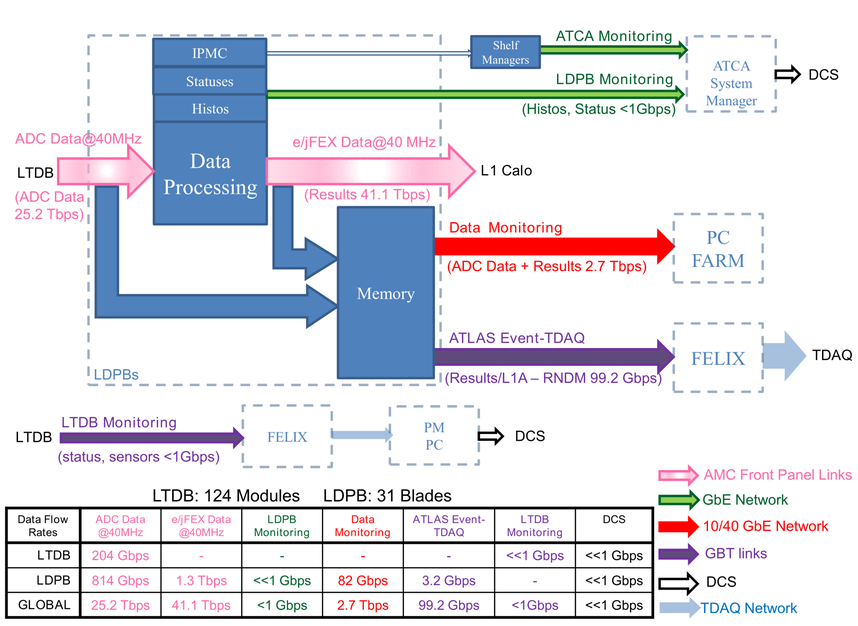


A stepwise upgrade of the LHC is foreseen starting now until the year 2023 to increase the instantaneous luminosity up to the fivefold of its design value. This implies a challenge for the ATLAS detector to cope with increased particle densities, especially for the Level-1 calorimeter trigger system. In order to keep the trigger rates within the limited bandwidth new algorithms (Figure right) have to be applied which in turn requires an upgrade of the ATLAS Liquid Argon calorimeter trigger readout electronics [1]. Towards this upgrade, the ATLAS LAr Calorimeter group develops a high-speed data acquisition interface in ATCA standard.



ATLAS Liquid Argon Calorimeter Electronics Upgrade

Due to the expected increased instantaneous luminosity of the LHC after 2018 an upgrade of the ATLAS Liquid Argon (LAr) Calorimeter trigger readout electronics is required. The front end electronics (FE) on the detector is going to be extended such that the current trigger towers (TT), which are the analog sums of 60 calorimeter cells, are split into 10 Super Cells whose output signal will be digitized with 40 MSPS with at least 12 bit precision within the FE while keeping the current TTs as legacy system. The digital Super Cell data are transmitted via optical fibers to the LAr back end electronics (BE) offside the detector where the energy and time reconstruction is performed by FPGAs.

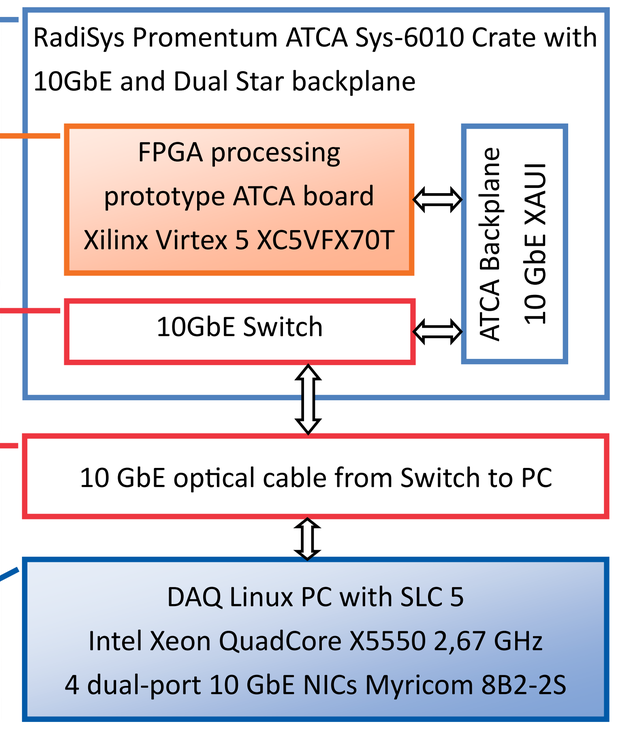


LTDB: 124 Modules LDPB: 31 Blades

Data Flow Rates	ADC Data @40MHz	e/jFEX Data @40MHz	LDPB Monitoring	Data Monitoring	ATLAS Event-TDAQ	LTDB Monitoring	DCS
LTDB	204 Gbps	-	-	-	-	<<1 Gbps	<<1 Gbps
LDPB	814 Gbps	1.3 Tbps	<<1 Gbps	82 Gbps	3.2 Gbps	-	<<1 Gbps
GLOBAL	25.2 Tbps	41.1 Tbps	<1 Gbps	2.7 Tbps	99.2 Gbps	<1Gbps	<<1 Gbps

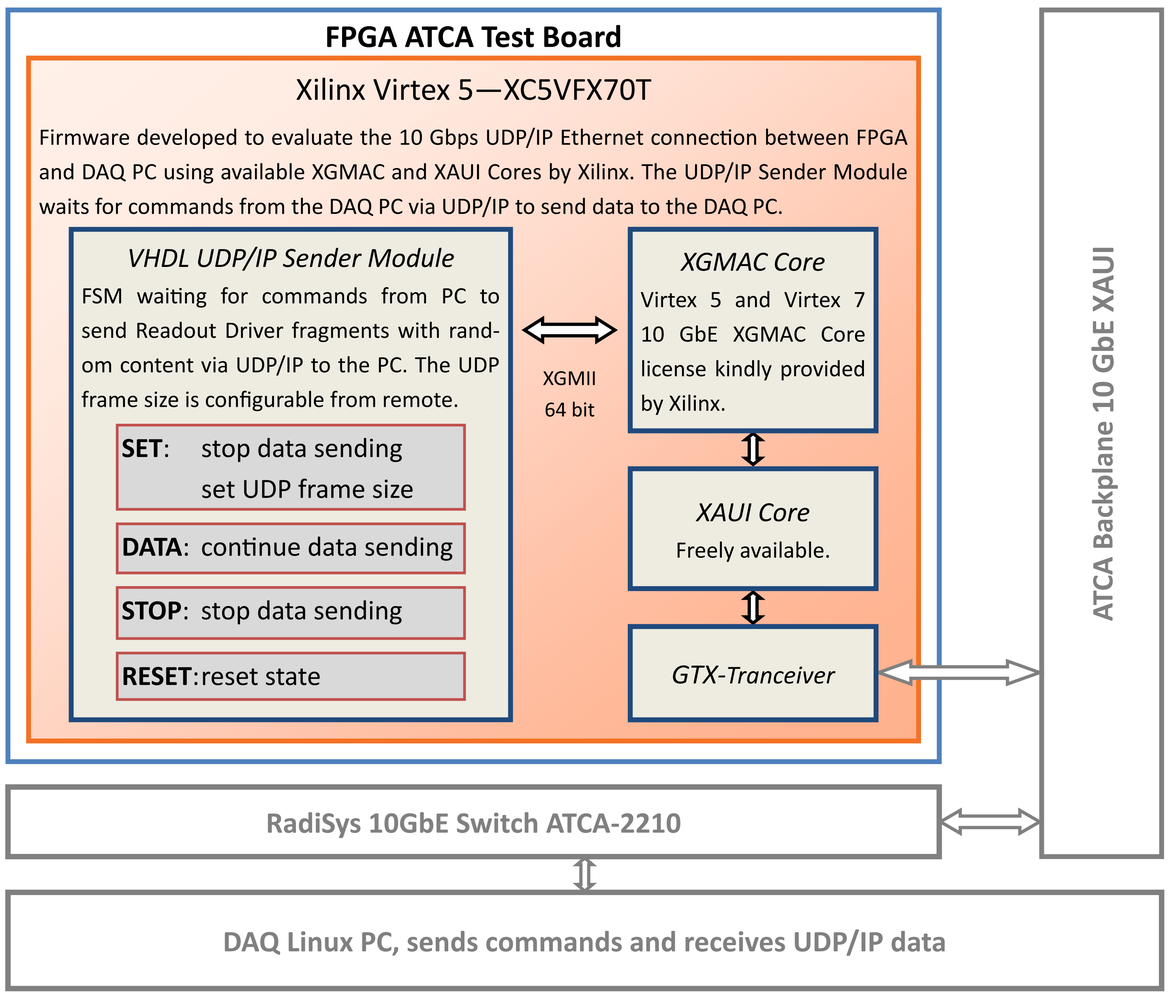
The BE will be housed in ATCA crates and is going to send data to the Level-1 Trigger as well as to a PC farm for DAQ and monitoring purpose [1]. The fast and reliable data transfer to this PC farm is the objective of the development efforts.

Test Setup Overview



The depicted test setup contains all components to evaluate the 10 Gbps Ethernet connections between the BE and the consecutive PC farm. An ATCA crate houses a FPGA test board to run energy and time reconstruction algorithms and to send data over the ATCA backplane to an ATCA switch and further to the readout PC. The goal is to demonstrate a highly reliable data transmission directly from an FPGA to a PC with a 10 Gbps standard protocol and almost only commercial hardware.

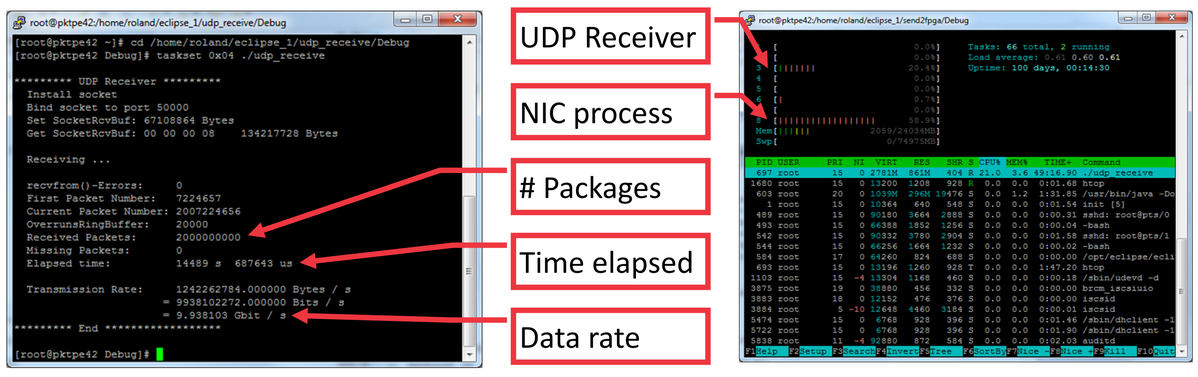
Back-End Readout FPGA Firmware



DAQ PC Software

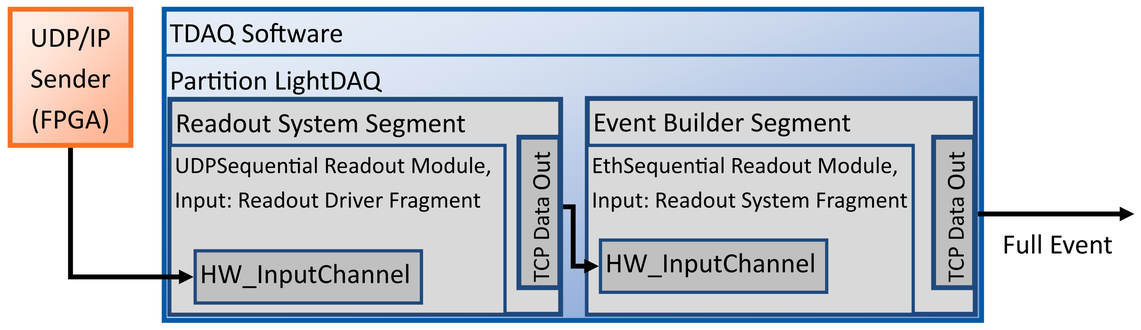
Data Transmission Performance Tests:

Continuous UDP/IP data stream from FPGA received by PC. Two billion UDP 9000 byte frames transferred within four hours without any loss of frames. The resulting data rate is **9.983 Gbps**. NIC and UDP receiver process were bound to specific CPUs.



ATLAS TDAQ Software Integration:

Installation of the ATLAS TDAQ software on PC done, adaption ongoing.



TECHNISCHE UNIVERSITÄT DRESDEN

References:
[1] ATLAS Collaboration, *LAr Phase-1 Upgrade TDR*, 2013, to be published
[2] ATLAS Collaboration, *Letter of Intent Phase-I Upgrade*, CERN-LHCC-2011-012, 2011

Supported by:
PHYSICS AT THE TERA SCALE Helmholtz Alliance
Bundesministerium für Bildung und Forschung