



Contribution ID: 78

Type: **Oral presentation to parallel session**

Many-core applications to online track reconstruction in HEP experiments

Thursday, 17 October 2013 14:10 (20 minutes)

One of the most important issues facing particle physics experiments at hadron colliders is real-time selection of interesting events for offline storage. Collision frequencies do not allow all events to be written to tape for offline analysis, and in most cases, only a small fraction can be saved. Typical trigger systems use commercial computers in the final stage of processing. Much of the effort is focused on understanding the latency for trigger systems. In this talk we describe updates to a previous study of latencies in GPU for potential trigger applications, where we measured the latency to transfer data to/from the GPU, exploring the timing of different I/O technologies on different GPU models. Those studies, where a simplified track fitting algorithm was parallelized and run on a GPU, show that latencies of few tens of microseconds can be achieved to transfer and process packets of 4 kB of data, combining the modern Infiniband data transfer technology with direct access to GPU memory allowed by NVIDIA GPUDirect utilities. We now have expanded our latency studies to include other multi-core systems (Intel Xeon Phi and AMD GPUs, in addition to NVIDIA GPUs) and other software environments (OpenCL, in addition to NVIDIA CUDA). We also discuss the implementation of a scaled-up version of the algorithm used at CDF for online track reconstruction - the SVT algorithm - as a realistic test-case for low-latency trigger systems using new computing architectures for LHC experiments.

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Session Classification: Data Acquisition, Trigger and Controls

Track Classification: Data acquisition, trigger and controls