# Measurements of the LHCb software stack on the ARM architecture

# Marco Clemencic, Ben Couturier, Niko Neufeld, Vijay Kartik Subbiah

Physics Department CERN CH-1211 Geneva 23, Switzerland

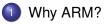
Computing in High Energy and Nuclear Physics, 2013



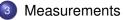
LHCb software stack on ARM

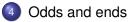
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# **Overview**









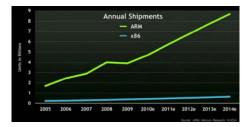


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LHCb software stack on ARM

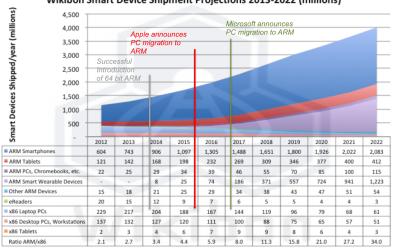
# The Market

- Most tablets and smart-phones powered by ARM processors
- 2013 will see more shipments of tablets than laptops
- Server market has virtually no growth, desktops declining





# Nightmare in Santa Clara



Wikibon Smart Device Shipment Projections 2013-2022 (millions)

Year

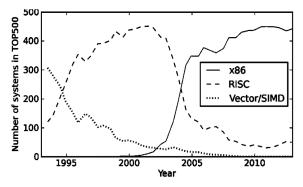
Source: Wikibon 2013, IDC & Garnter 2012 shipments & Wikibon 2013-2022 projections. Assumption: Apple & Microsoft migrate to successful 64-bit ARM.



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Why ARM?

# So you believe that Vax, Alpha, MIPS, *your favourite architecture here*, are eternal?



- μ-processors weren't faster
- They were much cheaper and "greener"
- Mobile processors are not faster
- They are much cheaper and greener

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In practice

# The computer-farm of the future



In practice

# The computer-farm of the future



# **Micro-servers**

- ARM-based SoCs are widely available now
- Lots of interest in micro-servers (cloud, web-shops)
- Still glue-logic is needed (no fast PCIe/SATA on current SoCs)
- Dense packaging of multiple SoCs
- Example (and used in these tests) Boston Viridis (based on Calxeda)



- 48 SoC, 4 cores 4 GB RAM
- ARM A9 Cortex 1.4 GHz (v7 architecture 32-bit)
- 80 Gb Ethernet switch (10 GigE external)
- Total 192 cores / 192 GB RAM /300 Watt

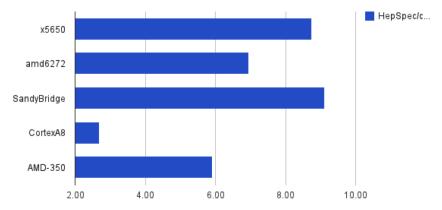
• redundant power, etc...



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# First look: HEPSpec



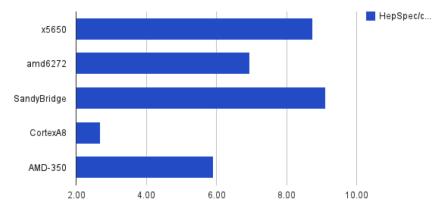


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# First look: HEPSpec





### So we need many

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LHCb software stack on ARM

# HEP spec is not enough - do the real test

# HepSPEC is not necessarily a good test for Online usage

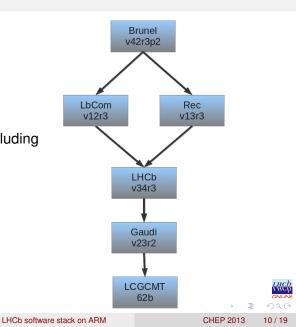
- Online we (currently) run *n* instances of the same application in parallel, where *n* is ≥ number of cores/hyperthreads
- In such a scenario hyperthreading typically adds overproportionally (up to 40% of total machine performance) compared to mixed work-loads
- Need to benchmark a real LHCb work-load: Brunel (the reconstruction program)

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### Measurements

# The task

- 3.6 MLOC of code (excluding LCG\_CMT)
- ROOT v5.34.05
- gcc 4.7.2, Boost 1.51



### Measurements

# The platform

- Remote test
  - CPU = Calxeda EnergyCore (SoC), ARM Cortex-A9 CPU, 4 cores,  $\approx$  1.1 GHz, 4GB RAM
  - Linux cloud12 3.6.10-8.fc18.armv7hl.highbank 1 SMP Tue Jan 29 14:01:38 EST 2013 armv7l armv7l armv7l GNU/Linux
- Local development, CARMA
  - CPU = NVIDIA Tegra 3, a Quad-core ARM Cortex-A9 CPU  $\approx$  1.3 GHz
  - Ubuntu 11.04
  - Linux carma-devkit 3.1.10-carma 2 SMP PREEMPT Fri Aug 31 15:28:42 PDT 2012 armv71 armv71 armv71 GNU/Linux
  - Not a hard-float kernel (not good)

(B) (A) (B) (A)

# Single core performance

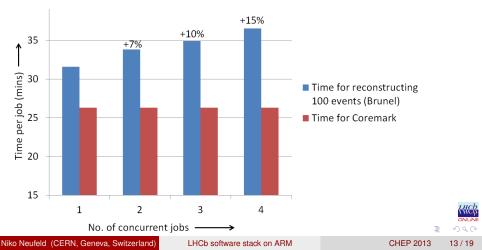
	CARMA	Viridis	x86 L5520
freq. (GHz)	1.3	1.1	2.27
# cores	4	4	8 (with HT)
total RAM (GB)	4	4	48
time (h)	$\sim$ 10	$\sim$ 2.5	$\sim 0.5$

- Time for reconstructing the same 1000 events in Brunel
- Events read from network share (NFS/AFS)
- Test results stable

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# Scaling

- Loading the entire machine with identical jobs
- x86 scales linearly for real cores, HT add about 40%
- ARM memory bandwidth does not scale



# Correctness

"Brem Match"	sum		mean/eff^*		rms∕err^*	
	ARMv7	x86_64	ARMv7	x86_64	ARMv7	x86_64
#calos	50085	50085	60.489	60.489	30.140	30.140
#chi2	2.73710 <b>9</b> e+09	2.73710 <b>5</b> e+09	5009.1	5009.1	2866.4	2866.4
#links	5464 <b>30</b>	5464 <b>15</b>	659.9 <b>4</b>	659.9 <mark>2</mark>	611.3 <mark>8</mark>	611.3 <mark>3</mark>
#overflow	403843 <mark>4</mark>	403843 <mark>0</mark>	4877. <mark>3</mark>	4877. <mark>2</mark>	5074. <mark>2</mark>	5074. <mark>0</mark>
#tracks	586 <b>10</b>	586 <mark>09</mark>	70.78 <mark>5</mark>	70.784	48.51 <mark>3</mark>	48.51 <b>1</b>



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# On the way

- Many small problems with very recent OS releases (FC18, Ubuntu 12)
- Kernel updates a bit more complicated, every platform needs specific patches, because there is no "ARM-PC"
- Obviously problems with closed-source, x86-only, software (NeuroBayes)

- Delicious architecture specific problems for the conaisseur
  - x86-icisms (e.g. sizeof empty struct)
  - Bad instructions issued by compiler (refused by assembler), toolchain problem?
- ROOT (v5.34.05) cintex not working completely (test fails), but subset required by LHCb seems to work.
- Loads of patches left, right and center due to newer compiler, boost, etc...versions

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# Building

- Compile-times are long on ARM. make -j 4 build of ROOT about 30 minutes on Viridis
- x-compiler chain has been setup.
- Problem with "fancy" builds creating and using intermediate binaries
- Can fix this with tweaking binfmt and using a VM
- In practice x-builds are painful for this stack, lots of room for improvement

# Summary

- ARM is clearly a "hype" we wanted to do a reality check
- Ported entire LHCb software stack to ARM (v7) on FC18
- Results are correct (up to small rounding errors)
- Single core performance about a factor 5 to 7 slower (compared to now obsolete Nehalem μ-architecture!)
- ARM memory bandwidth does not scale (yet)
- Power promise holds
- ARM-based microservers still need a strong TCO argument to be interesting

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# What's next?

- Improve multi-architecture build (cmake)
- Prepare maintainable, automatised cross-build system
- Wait for establishment of 64-bit ARM micro-servers, redo tests
- Compare with upcoming improved Intel micro-servers

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# Thanks

- Thanks to all members of the SFT group who supported us
- and to Boston HPC, UK, who kindly provided remote access to their Viridis platform

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