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ATLAS Phase-II High Luminosity UK Planar Pixel Sensors

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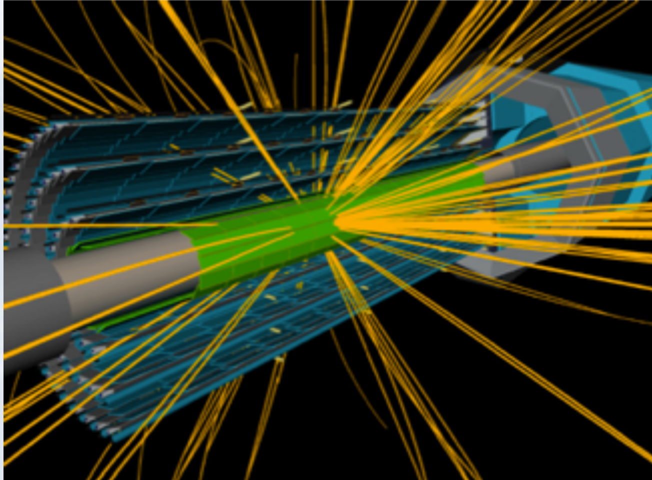
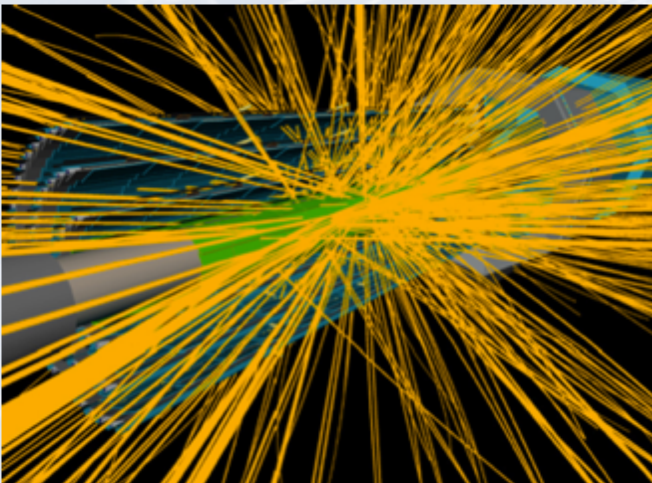
On behalf of the UK ATLAS Pixel Upgrade group

University of Liverpool

MICRON SEMICONDUCTOR ltd

Introduction



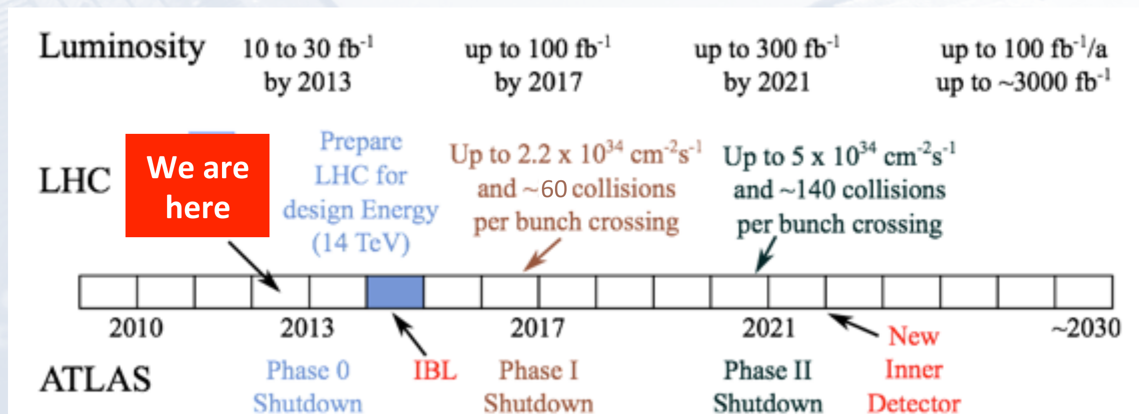


Luminosity upgrade to LHC driven by

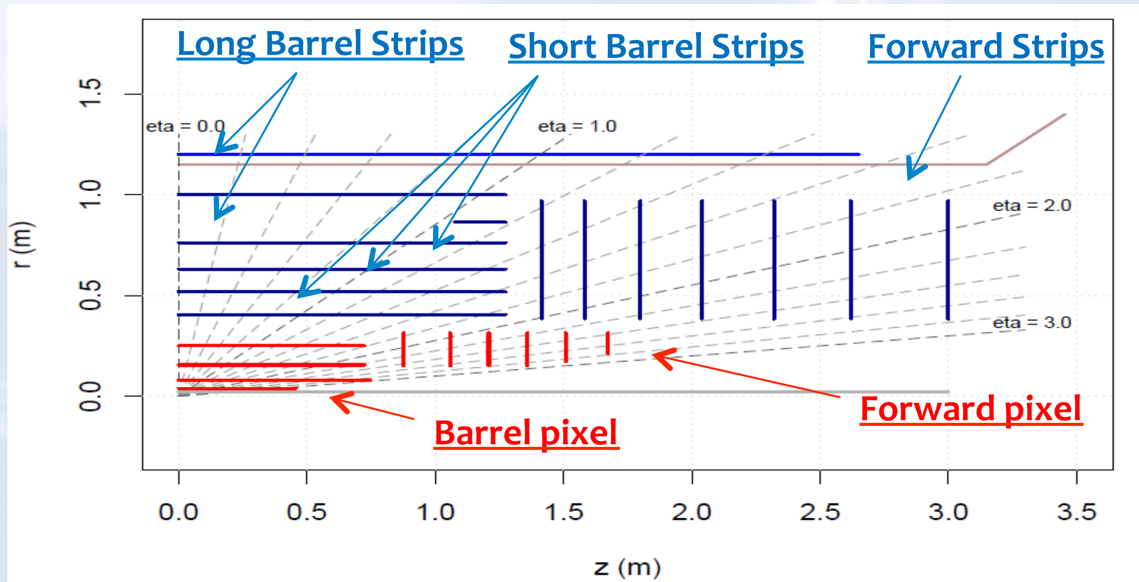
- Desire to reduce statistical uncertainties
- Desire to increase search for new physics at higher energy via lower probability events

Luminosity increase by an order of magnitude

- Corresponding increase in occupancy(depends on luminosity leveling)
- Radiation damage to a maximum of $2 \cdot 10^{16}$ 1MeV n_{eq}/cm^2



Phase-II ATLAS ITk baseline layout



- 4 pixel barrel layers
  - Radius from 39 mm to 250 mm
  - Z: ±449 mm to ±694 mm (outer 2 layers)
- 6 Pixel disks
  - R_{inner} = 150 mm
  - R_{outer} = 315 mm
  - Z: 820 mm to 1890 mm

2 outer Pixel Barrel layers / **Disks**

Sensor
- planar n-in-p
- 150 µm

Pixel size 50 µm x 250 µm
ROC (ReadOut Chip) thickness 150 µm
ToT (Time over threshold) = 4 bits
2x2 (Quad) and 2x3 (Hex) chip modules
Data rates of 640 Mbit/s per module

2 Inner Pixel Barrel layers

- Sensors
  - PPS and 3D – Diamond, n-in-n/n-in-p silicon
  - 150 µm silicon/diamond or thinner
- Pixel size 25 µm x 150 µm
- ROC (ReadOut Chip) thickness 150 µm
- ToT (Time over Threshold) = 0-8 bits
- 2x1 and 2x2 chip modules
- 2x2 sensor = 33.9 mm x 40.6 mm
- Data rate as high as 2 Gbit/s per module

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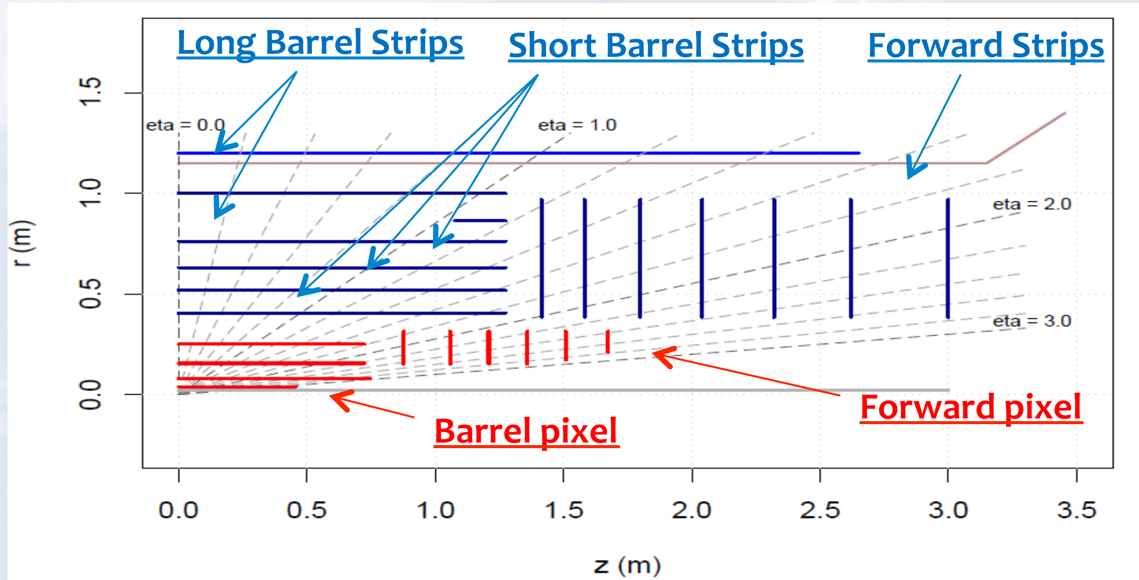

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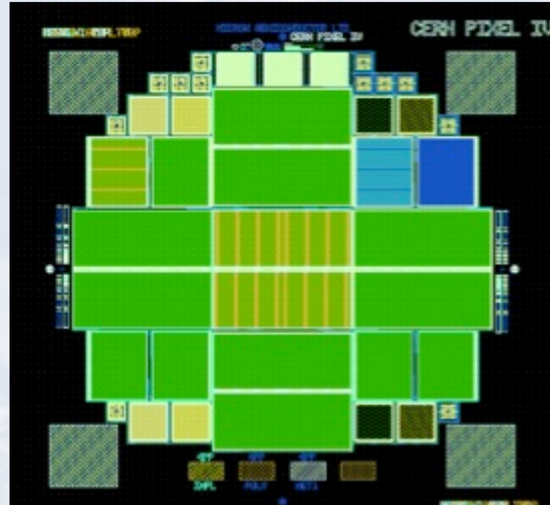
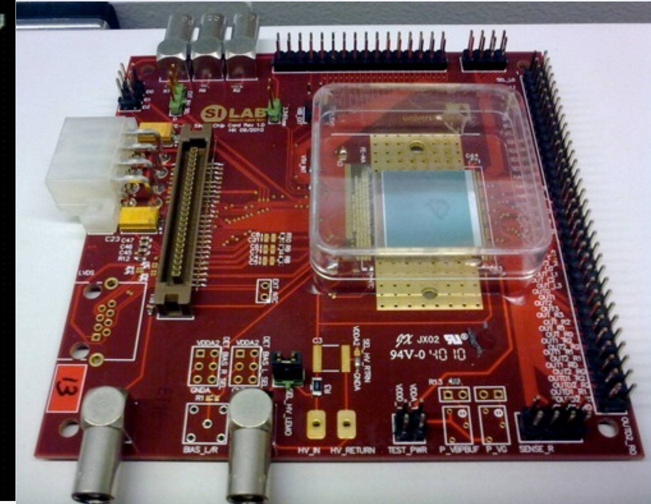
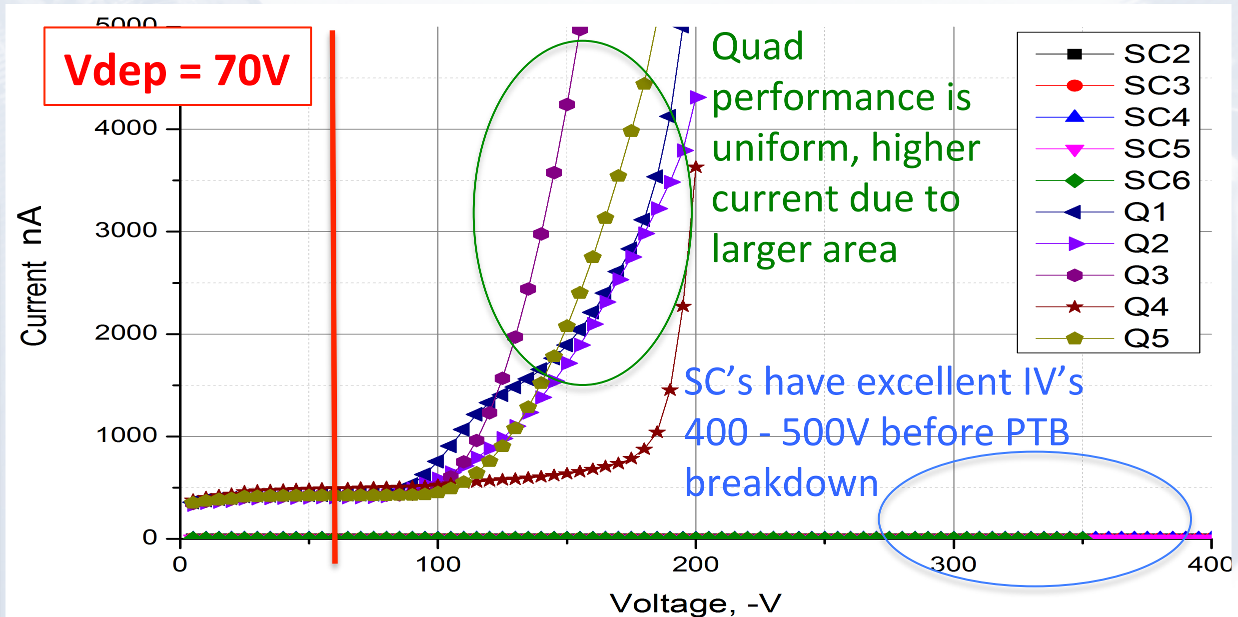
Sensors and ROC

- Sensors produced by Micron Semiconductors LTD based in Worthing, UK
- ATLAS IBL FE-I4 ROC used
- General silicon resistivity used ~10kΩ, 300µm thick
- Single and Quad FE-I4 compatible sensors Vdep = 70V
- All sensors show reduced current after flip chipping by a factor of 5-10 times less than on die IV measurements, Punch Through Bias is bypassed after bump bonding







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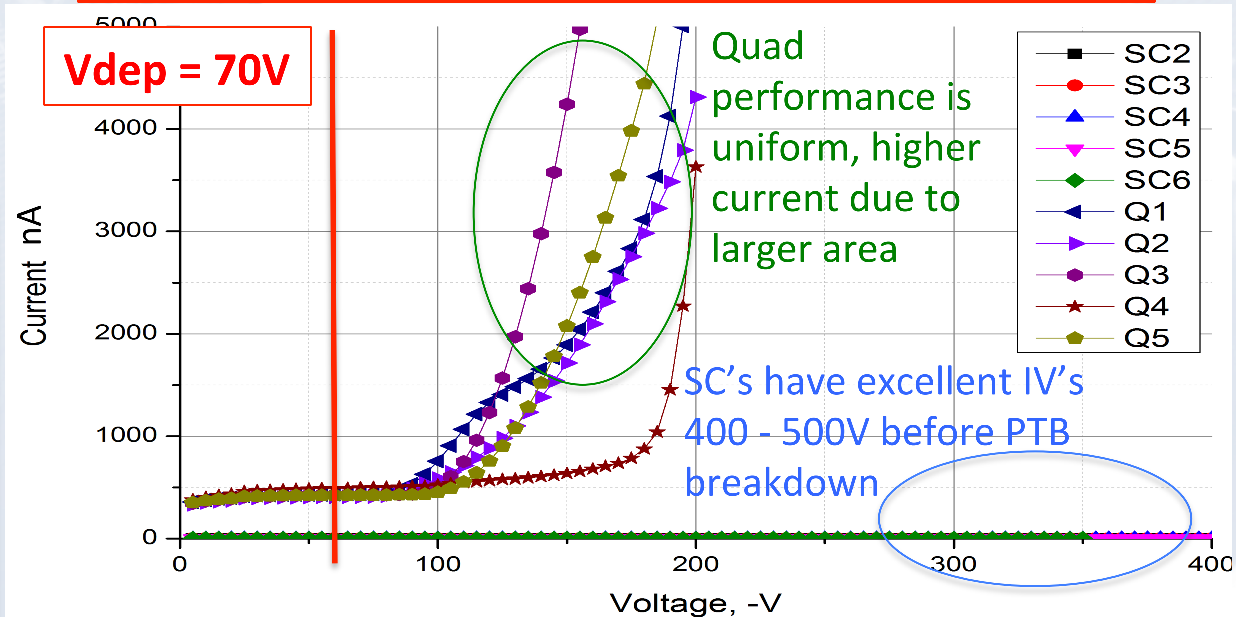
Quad sensor on rigid test board has leakage current of ~80nA with all four ROC's powered, with sensor at -100V

On die wafer IV measurements at -100V are around 500nA

The cause is high bias dot density for pre bump bond testing – required by ATLAS



Non-standard designs for Phase-II

Liverpool CERN Pixel V wafer - Test vehicle for different layouts and structures. All compatible with FE-I4

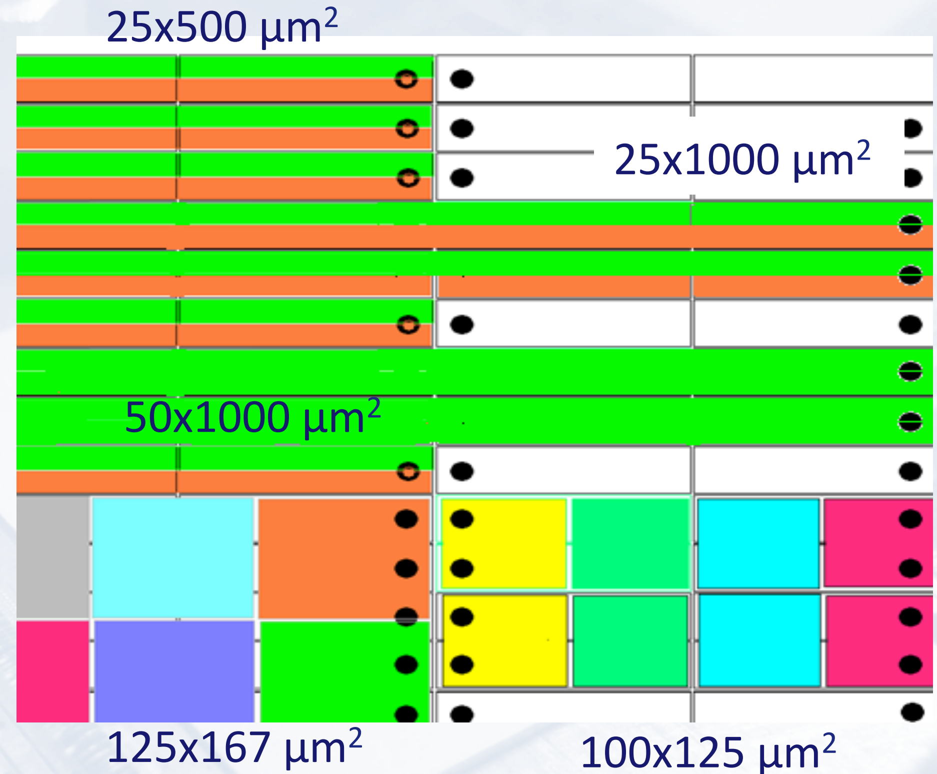
Disks
- Square pixels may be an advantage for tracking

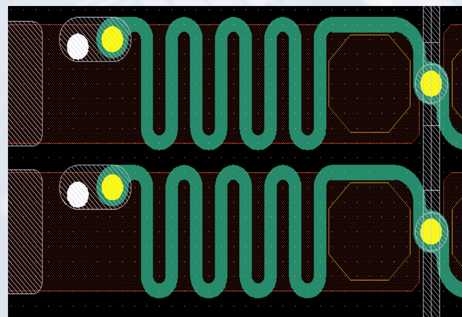
Large radius use strips
- Lower position resolution requirements
- Lower power and cost

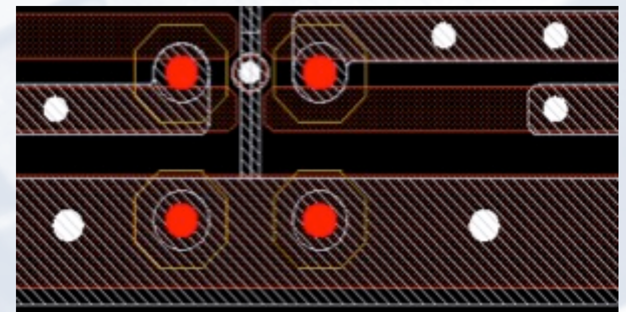
Long large area implants
- Turn off some pixels to save cost
- Lower density flip-chip to reduce cost

Bias dot optimization to increase detection efficiency after high radiation dose

Poly-silicon bias structures
- Remove bias dot completely
- AC couple detectors possible







QUAD FE-I4 Sensors

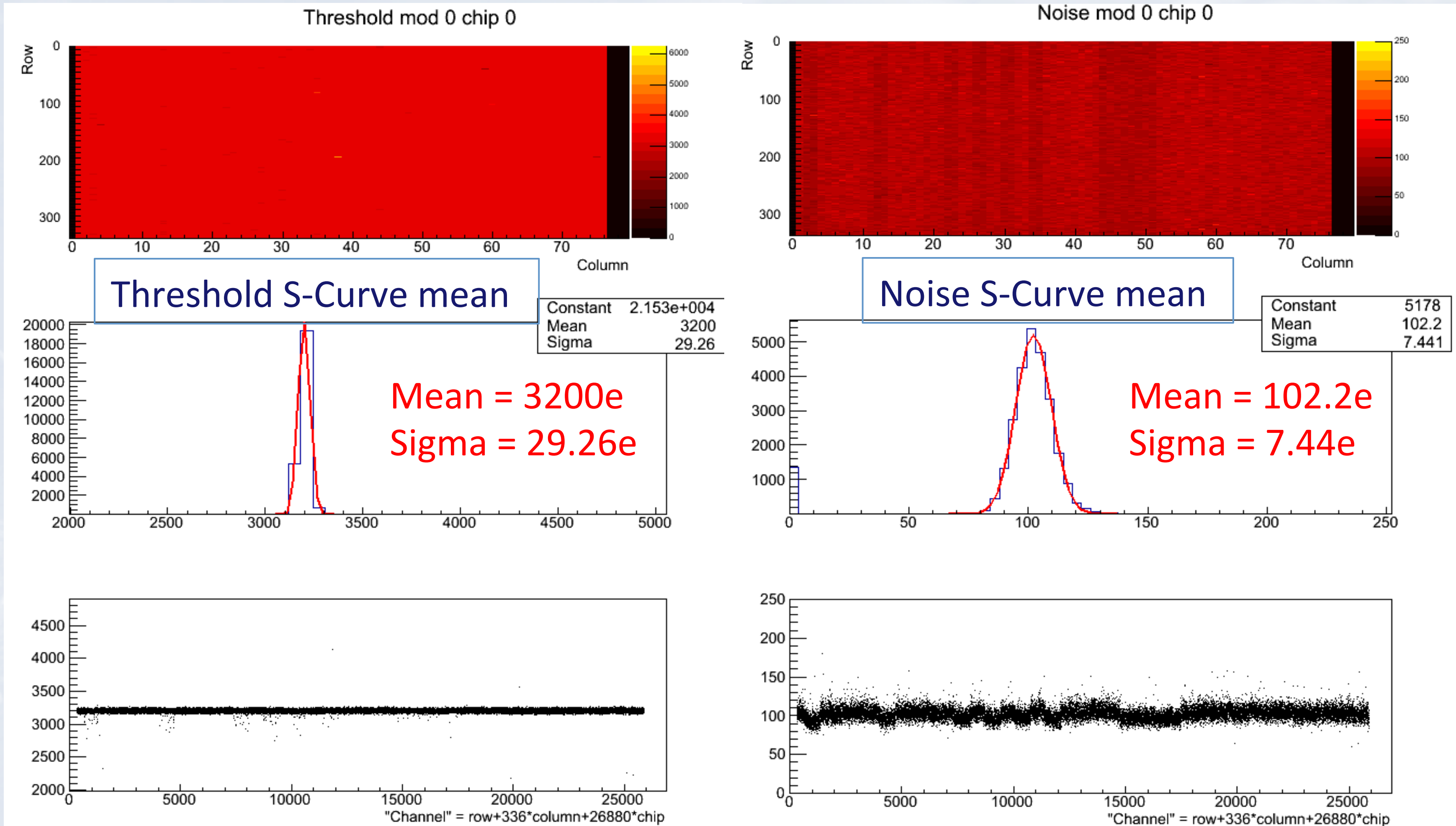
- Quads are roughly 4x4cm (singles 2x2cm)
- Only group to have a dedicated QUAD sensor design.
- UK have 4 fully bumped QUAD assemblies
- 2 have been irradiated to $5E15n_{eq}/cm^2$ in CERN's PS before shutdown, awaiting testing. Modifications to the Liverpool rigid test card needed
- 1 QUAD has been glued to a Bonn flex and mounted onto a rigid card for multiplexing testing.
- 1 QUAD mounted on a rigid test card similar to the SC rigid card IBL sensors used, Sensor can be un-mounted without breaking wire bonds from ROC
- A Further 10 QUADs to be produced in 2013 for use in building a pixel disk segment

Manchester Multiplexer test card

Liverpool Quad Rigid test card

Tuning of assemblies

Each device tuned for in-time threshold, 3200e then tuned down to lower thresholds. ToT (Time Over Threshold) is calibrated according to device thickness but will not be shown



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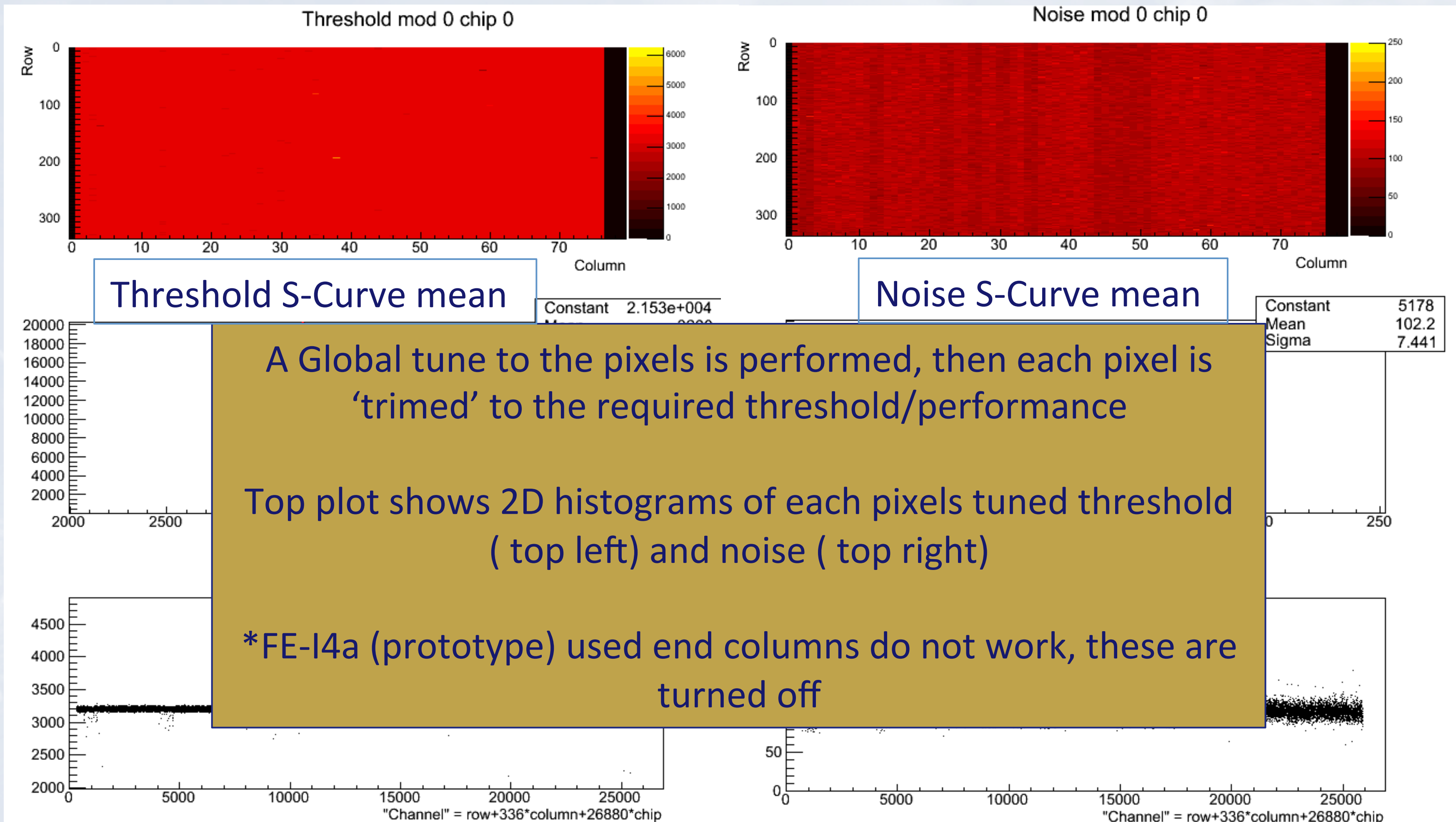

A Global tune to the pixels is performed, then each pixel is 'trimed' to the required threshold/performance

Top plot shows 2D histograms of each pixels tuned threshold (top left) and noise (top right)

*FE-I4a (prototype) used end columns do not work, these are turned off

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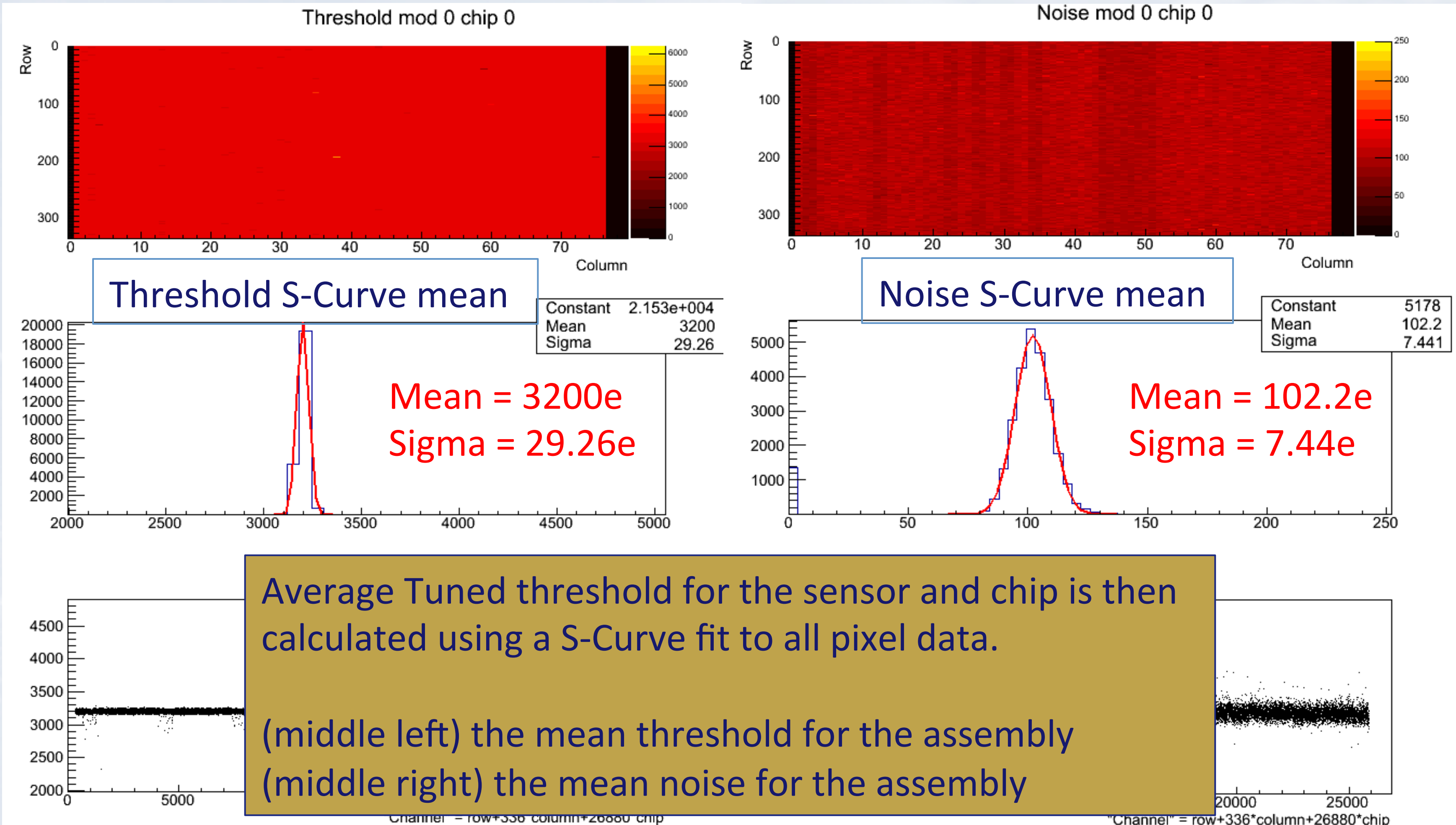

Average Tuned threshold for the sensor and chip is then calculated using a S-Curve fit to all pixel data.

(middle left) the mean threshold for the assembly
(middle right) the mean noise for the assembly

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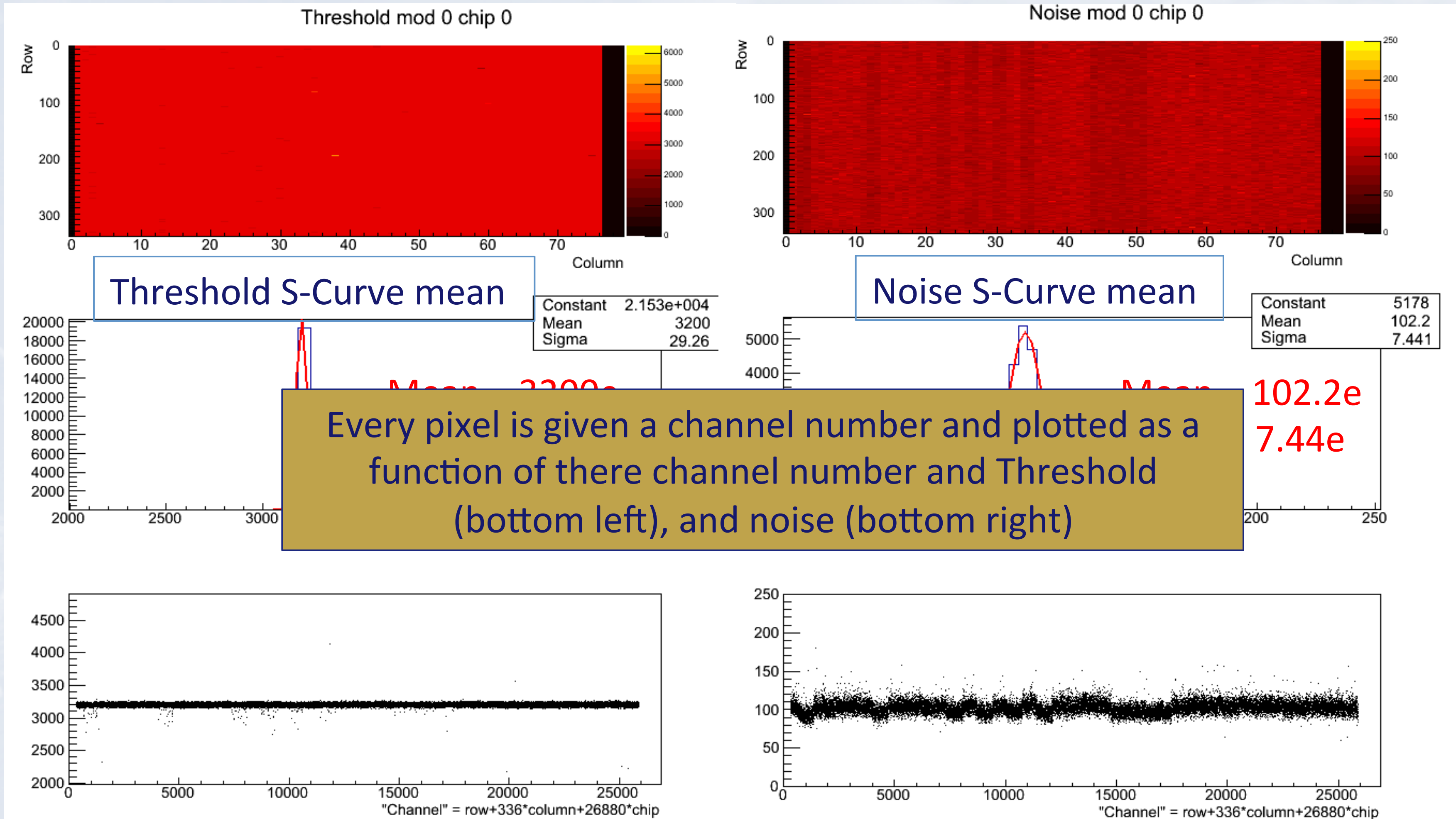
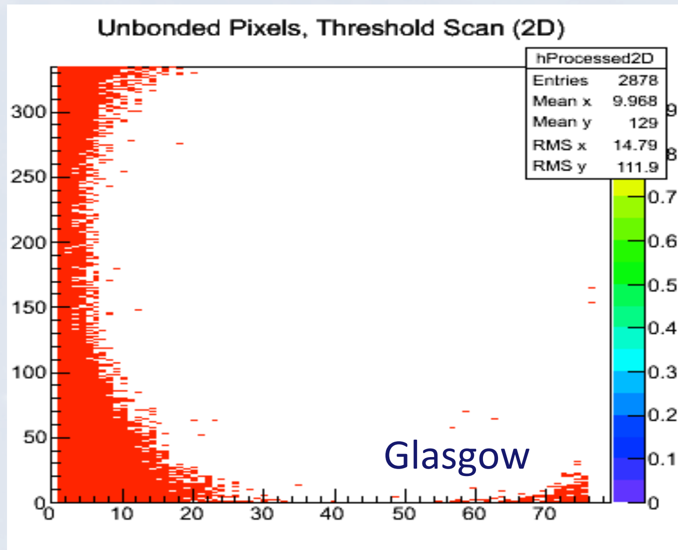


Every pixel is given a channel number and plotted as a function of there channel number and Threshold (bottom left), and noise (bottom right)

Disconnected pixels

Pre bump bonding thinned ROC's show some disconnected pixels, due to roc bowing with temperature



Large areas of non-boned pixels at the corners & edges (only for very thin readout chips)

Disconnected pixels are rare for full thickness ROC's and for post bumped thinned ROC and sensors for single and quad sensors

Bump Process Flow

1. Deposit UBM and bumps on ROIC
2. Thin ROIC to 200 µm / Diced
3. On vacuum jigs perform flip-chip for tack bond
4. Re-flow in reducing atmosphere in oven (260C) unsupported assembly
   - Self-align bumps
   - Obtain good electrical properties

ROIC bows due to non-symmetric layers

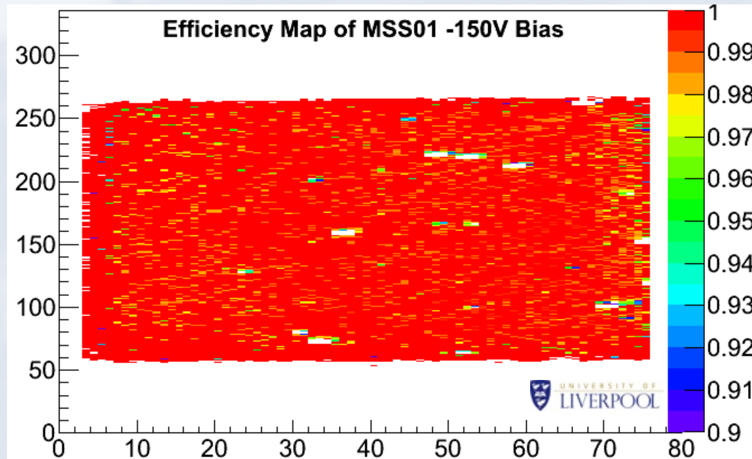
- Thick dielectric layers on top side
- Just silicon on back side

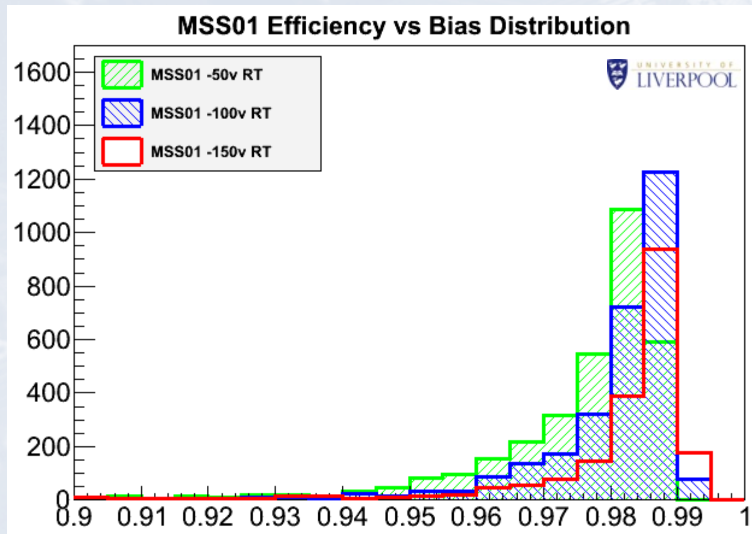
Solution under investigation

- Support wafer technology
- Deposition of balancing dielectric on ROIC

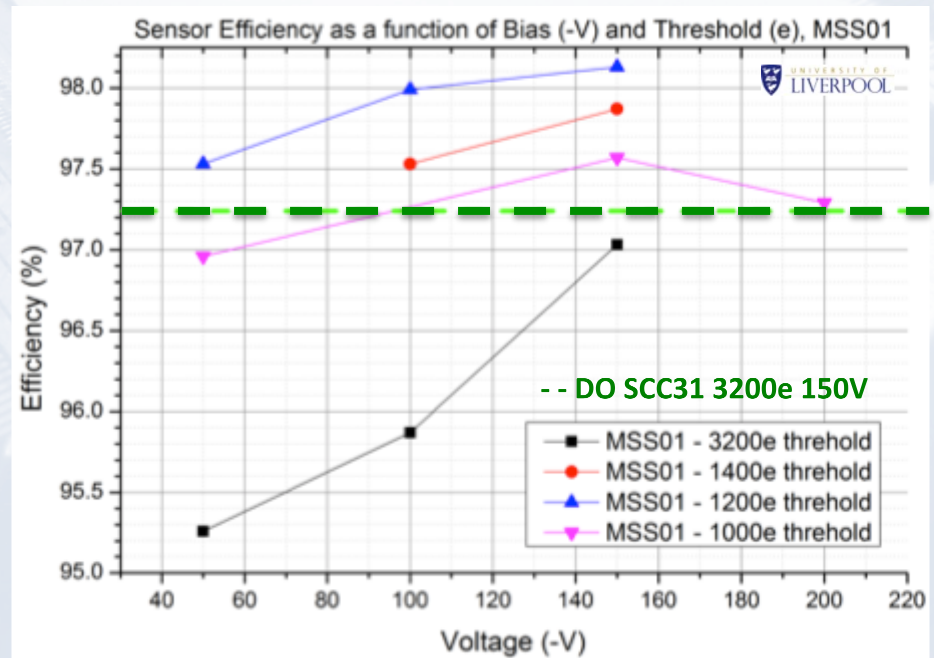
First test beam results

DESY – 4GeV Positrons





- Devices are tested for high tracking efficiency vs Bias voltage and tuned Threshold
- high hit efficiency seen even for under depleted devices
- High hit efficiency important at low threshold operation to benefit from charge sharing after irradiation without losing hits that would normally be under threshold



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Ongoing UK progress

- Production of new Liverpool Cern Pixel 5 wafer, (square pixels, strixels, increased Rϕ resolution sensors), Liverpool/Micron
- Irradiated Quad tests (2 irradiated quads at 5E15 1MeV n_{eq}/cm^2), Liverpool
- Testbeam data reconstruction/analysis, Liverpool
- Quad/Hex Module multiplexing, Manchester
- Thin ROC support wafer/ backside dielectric for production flip chipping, Glasgow
- FE-I4a/b wafer probing (FE-I4 ROC pass/fail), Glasgow/Edinburgh
- Pixel disk segment prototype mechanics/structure, Liverpool, Manchester, Glasgow
- Disk tapes, Edinburgh
- Wafer cleaning and passivation of FE-I4 wafers and material identification of pads, RAL
- Flip chipping, RAL
- Flex serial powering, RAL

Summary

Micron 6inch FE-I4 single and quad sensors available for production with high yield

300, 200, 150, 100μm thick, and n-in-n and n-in-p geometry types

Assemblies with flip-chip VTT

Excellent assembly IV characteristics

Problems at the edge due to bow with low bump yield

Quad module

Preliminary tests are very promising, first group to have a dedicated design

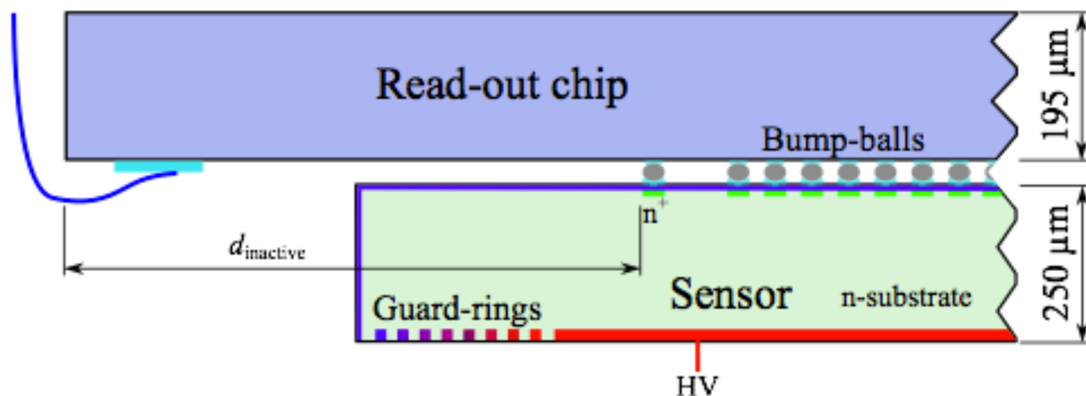
Testbeam analysis

Work under way into publishing test beam data for standard and non standard single and quad modules

ATLAS PPS 2012 and 2013 results papers
As well as general R&D papers for the quad and other designs

BACKUP

Current ATLAS Pixel Detector



Sensor design

- DOFZ Si n-substrate, 250µm thick
- Read-out chip planar n+-in-n pixels, 400x50µm2
- 16 guard rings on p side to shape HV step
- 1.1 mm inactive edge incl. safety margin

Read-out and interconnection

- FE-I3: 2880 channels
- DC coupled and bump bonding
- Shaper + Amplifier + Discriminator
- ToT ∝ Charge