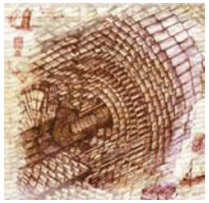


Upgrade of the CMS Tracker

Katja Klein

1. Physikalisches Institut B

RWTH Aachen University

2013 EPS Conference on High Energy Physics, Stockholm, Sweden
19th of July, 2013

The CMS Tracker Upgrade: Overview

2013	**Long Shutdown 1**	• **Consolidation:** Improvement of tracker thermal insulation
2014		• New beam pipe • Installation of pixel test slice } preparation for phase-1
2015	*Data taking*	
2016		
	Technical stop	**Installation of new CMS phase-1 pixel detector**
2017	*"Phase-1"*	
2018	**LS2**	
2019	*Data taking "Phase-1" ≈ 500 fb^{-1}*	Exchange of innermost pixel layer after ~ 250fb^{-1}
2020		
2021		
2022	**LS3**	**Installation of a new CMS tracker** • Phase-2 pixel detector • Phase-2 outer tracker • Track trigger
2023		
2024	*Data taking "Phase-2" ≈ 3000 fb^{-1}*	
↓		

The CMS Tracker Upgrade: Overview

2013	**Long Shutdown 1**	• **Consolidation:** Improvement of tracker thermal insulation • New beam pipe • Installation of pixel test slice } preparation for phase-1
2014		
2015	*Data taking*	
2016		
	Technical stop	**Installation of new CMS phase-1 pixel detector**
2017	*“Phase-1“*	
2018	**LS2**	
2019	*Data taking “Phase-1“ ≈ 500 fb^{-1}*	Exchange of innermost pixel layer after ~ 250fb^{-1}
2020		
2021		
2022	**LS3**	**Installation of a new CMS tracker** • Phase-2 pixel detector • **Phase-2 outer tracker** • **Track trigger**
2023		
2024	*Data taking “Phase-2“ ≈ 3000 fb^{-1}*	
↓		

Red = covered in this presentation

The Phase-1 Pixel Upgrade

- Present pixel detector was designed for $1 \cdot 10^{34}$ $cm^{-2}s^{-1}$ @ 25ns bunch spacing
- Conditions at LHC Phase-1: $2 \cdot 10^{34}$ $cm^{-2}s^{-1}$ @ 25 or 50ns → 50 or 100 pile-up events; int. luminosity of 500 fb^{-1} and hit rates of ≈ 600 MHz/cm^2 → data losses of up to 50%

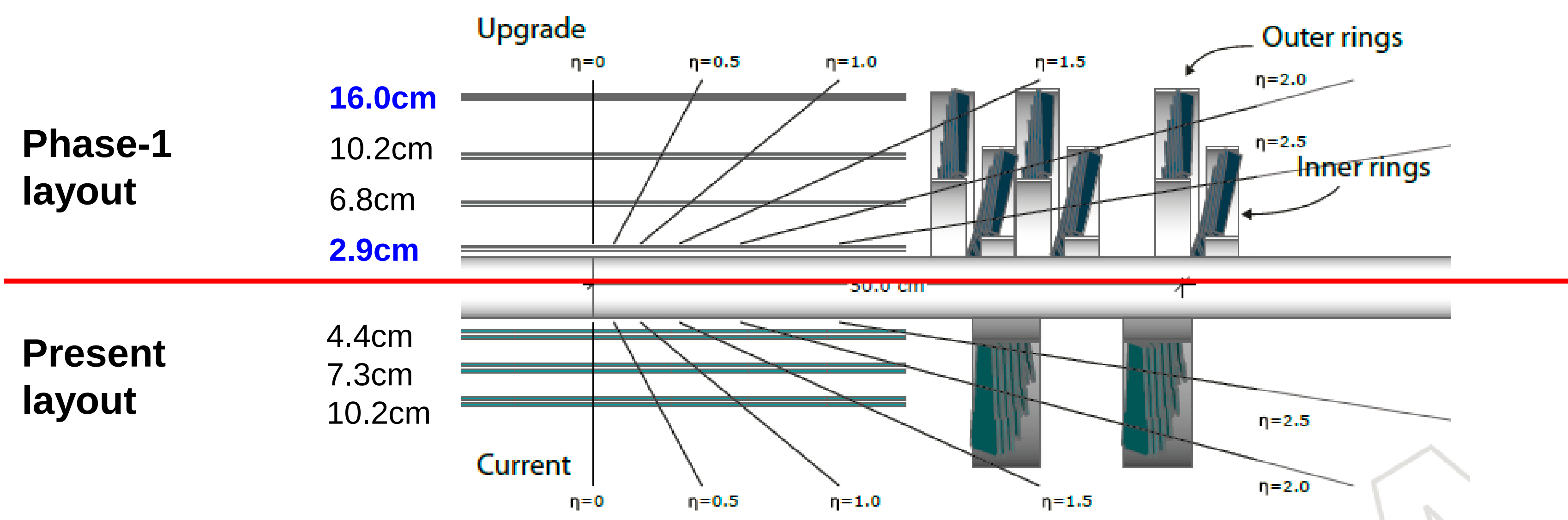
→ “Evolutionary upgrade“ with minimal impact on data taking

The Phase-1 Pixel Upgrade

- Present pixel detector was designed for $1 \cdot 10^{34}$ $cm^{-2}s^{-1}$ @ 25ns bunch spacing
- Conditions at LHC Phase-1: $2 \cdot 10^{34}$ $cm^{-2}s^{-1}$ @ 25 or 50ns → 50 or 100 pile-up events; int. luminosity of 500 fb^{-1} and hit rates of ≈ 600 MHz/cm^2 → data losses of up to 50%

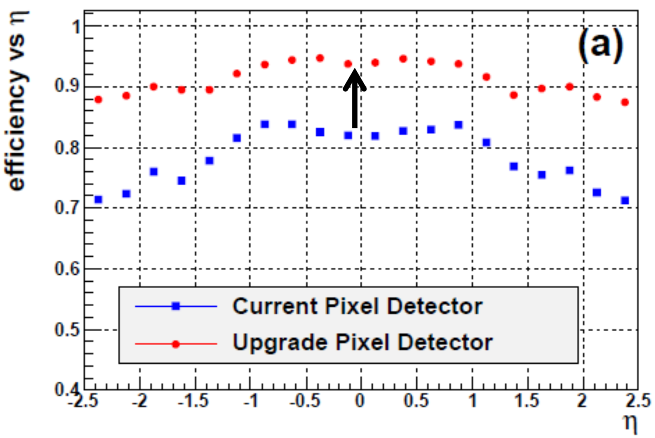
→ “Evolutionary upgrade“ with minimal impact on data taking

- 4 hit coverage → robust tracking
- Smaller radius of innermost layer → better vertex resolution & b-tagging efficiency
- Improved readout chip → recovery of hit efficiency
- Evaporative CO_2 cooling, relocation of patch panels, lighter mechanics → less material
- Novel powering scheme allows to power factor of 1.9 more channels

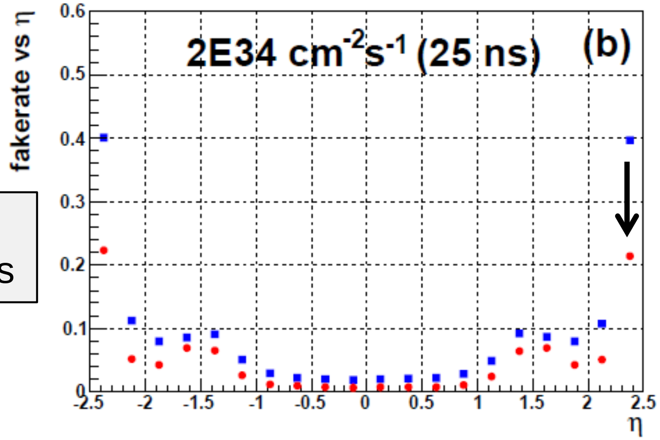


Simulated Performance

Tracking efficiency

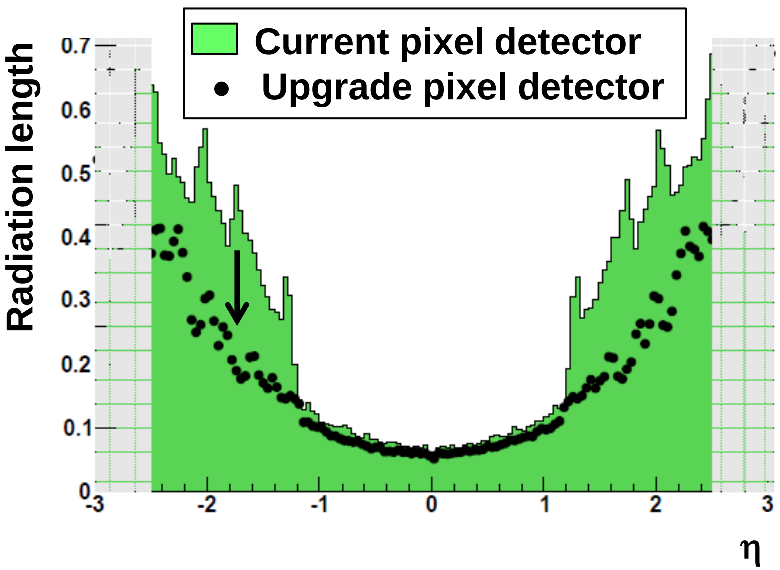


Fake rate

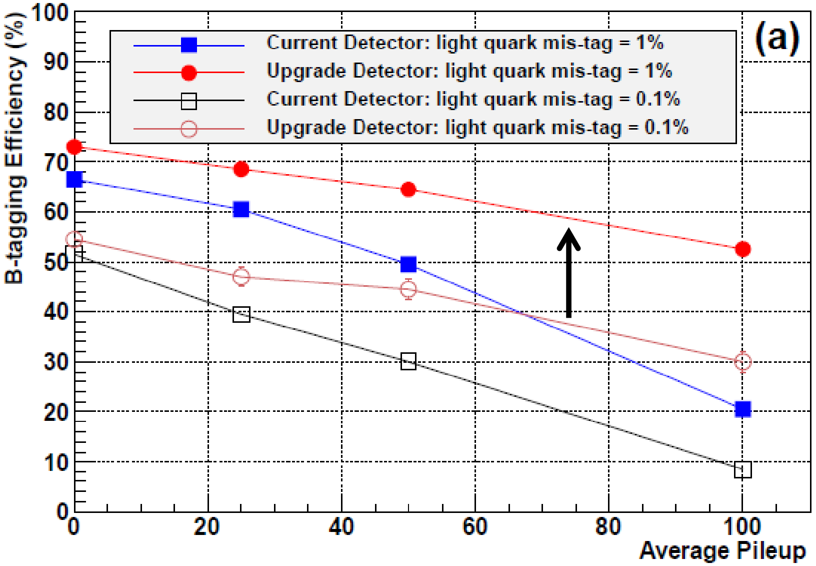


ttbar sample
50 pileup events

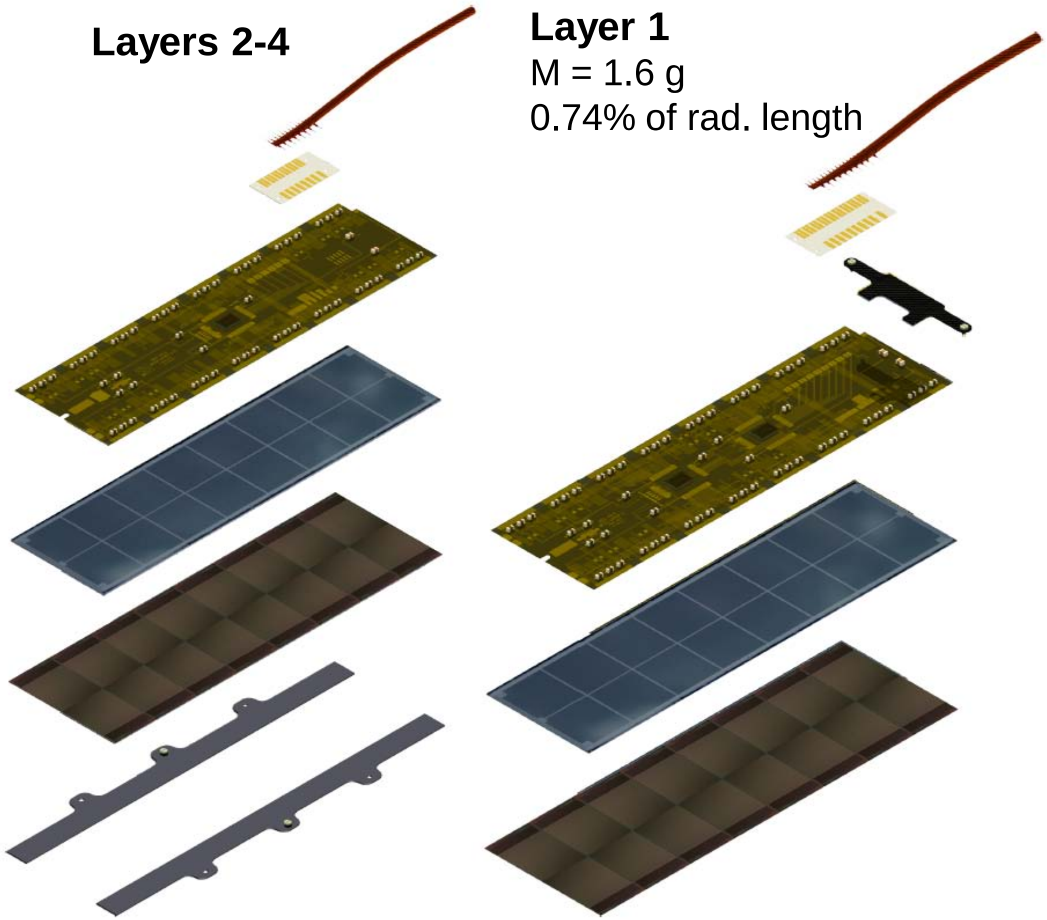
Material budget



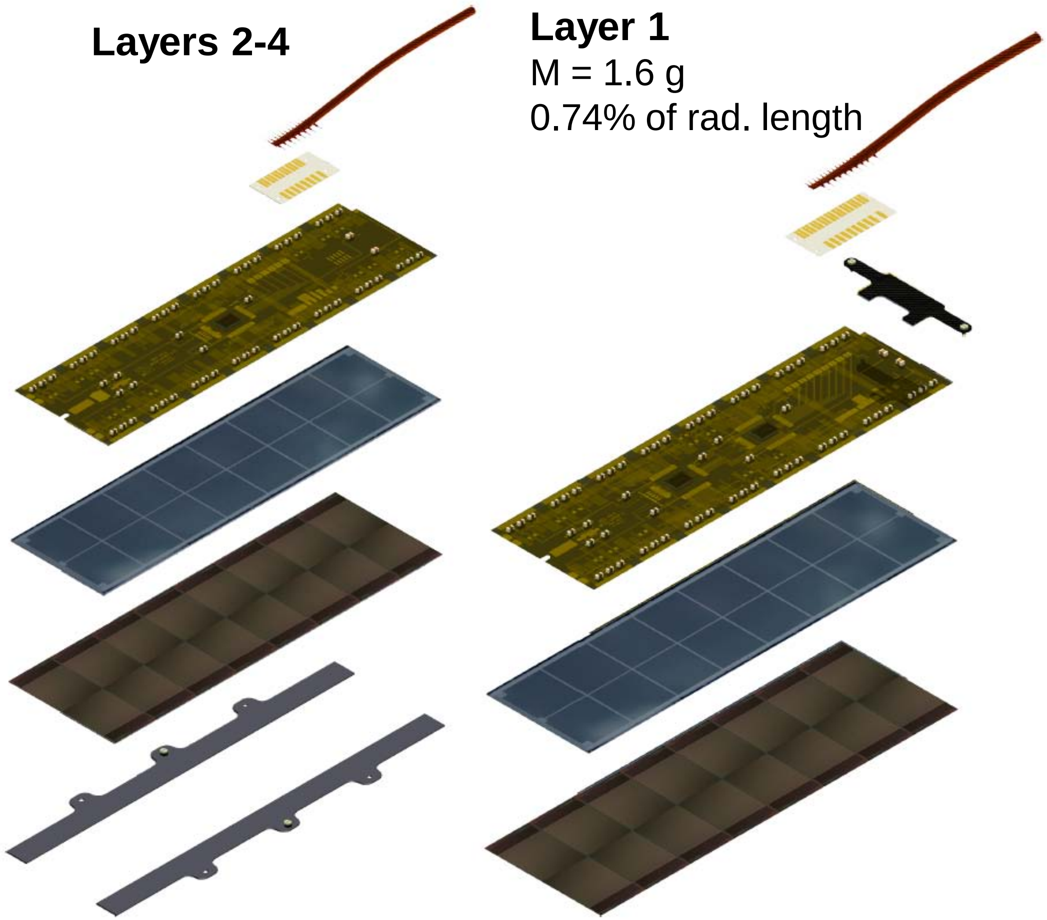
B-tagging efficiency vs. pile-up



Pixel Modules

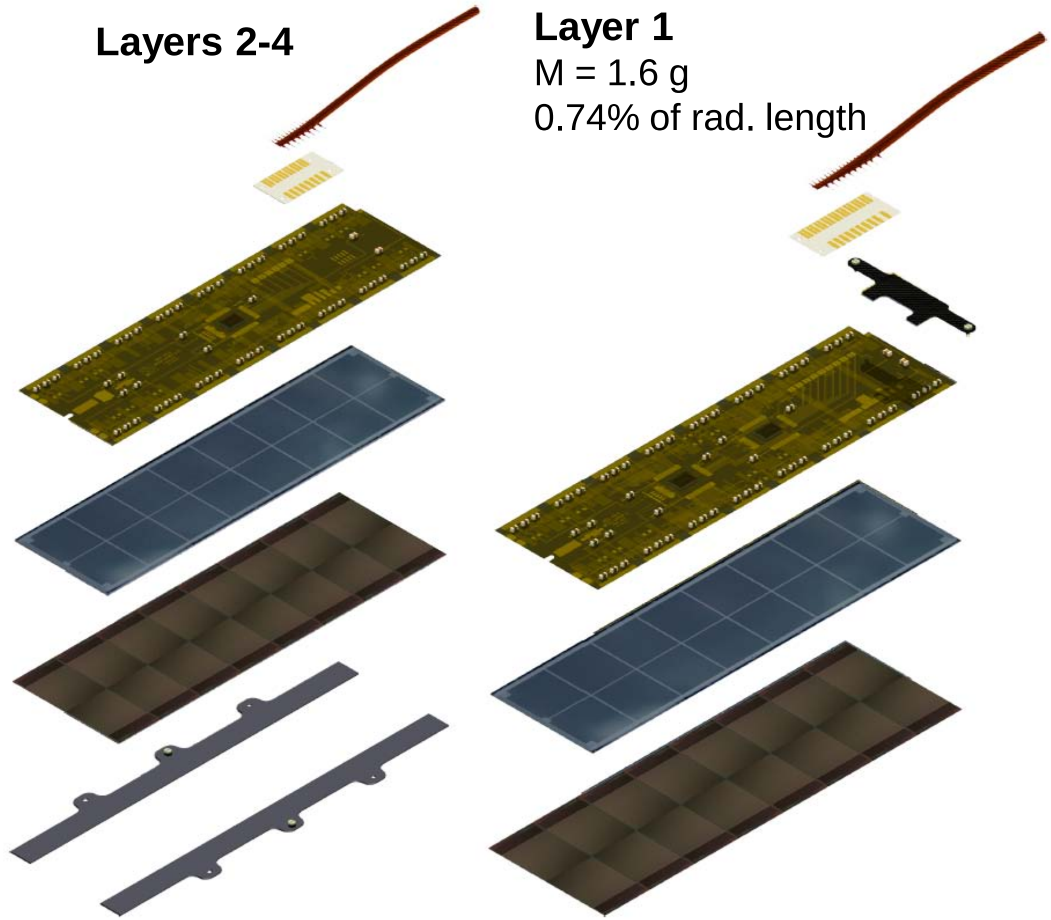


Pixel Modules



Si_3N_4 base-strips, 250µm thick
or carbon fiber clip (L1)

Pixel Modules



16 readout chips (ROCs)
Bump-bonded to sensor
Thinned to 180µm & 75µm (L1)

Si_3N_4 base-strips, 250µm thick
or carbon fiber clip (L1)

Pixel Modules

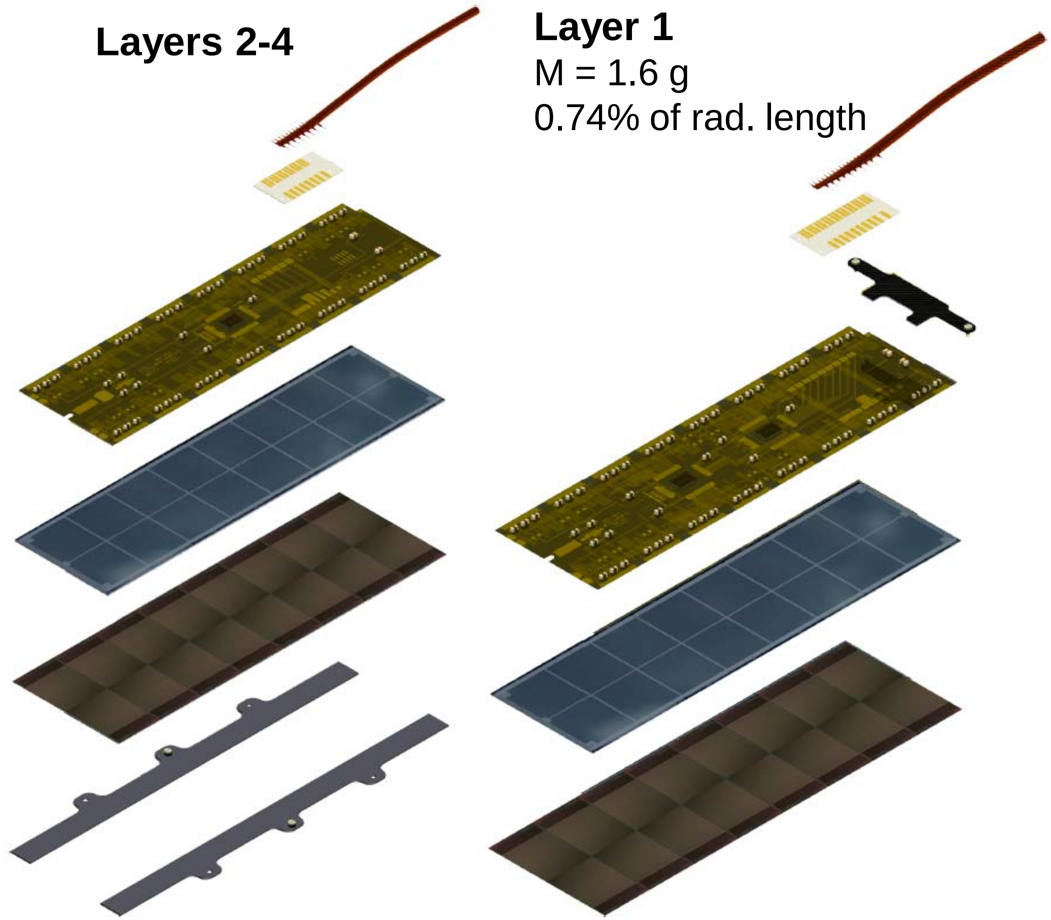
n+-in-n silicon sensor (as today)
Active area: 16.2 x 64.8 mm^2
100µm x 150µm pixels
66 560 pixels per sensor

16 readout chips (ROCs)
Bump-bonded to sensor
Thinned to 180µm & 75µm (L1)

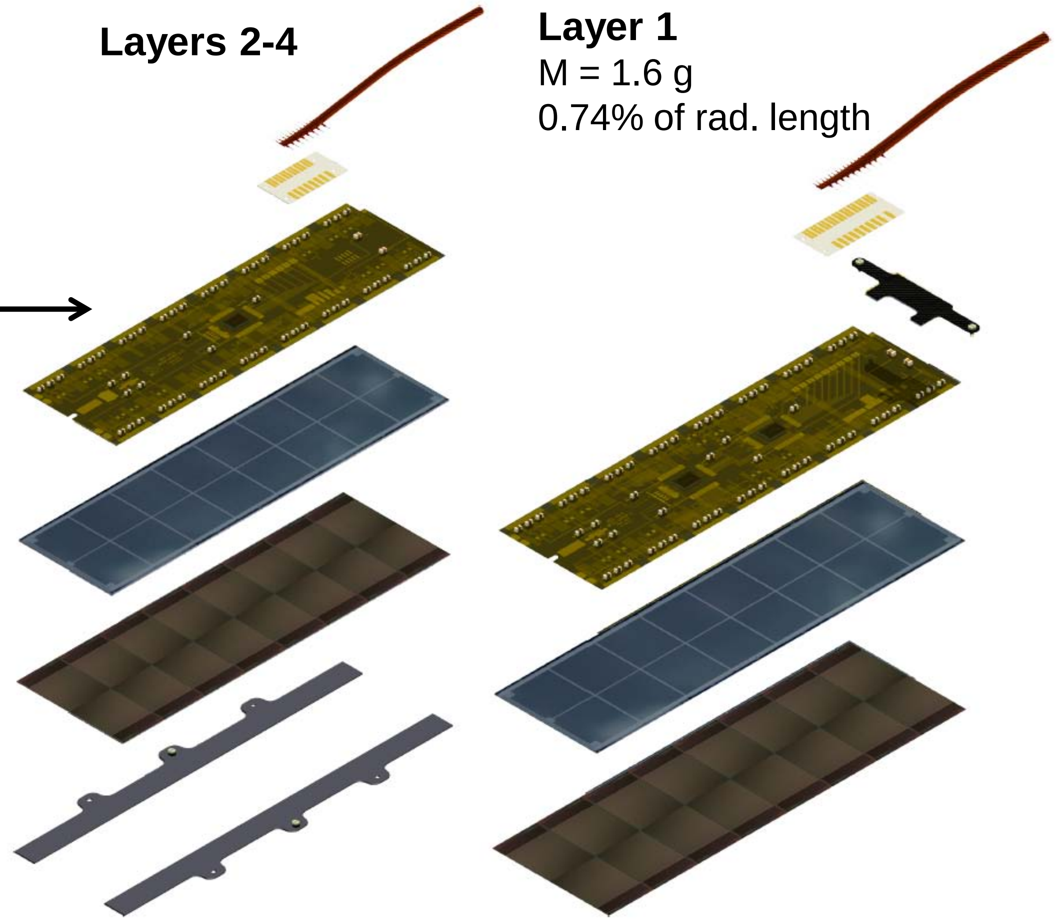
Si_3N_4 base-strips, 250µm thick
or carbon fiber clip (L1)

Layers 2-4

Layer 1
M = 1.6 g
0.74% of rad. length



Pixel Modules



PCB with data manager chips
3 x 2µm Cu layers

n+-in-n silicon sensor (as today)
Active area: 16.2 x 64.8 mm^2
100µm x 150µm pixels
66 560 pixels per sensor

16 readout chips (ROCs)
Bump-bonded to sensor
Thinned to 180µm & 75µm (L1)

Si_3N_4 base-strips, 250µm thick
or carbon fiber clip (L1)

Pixel Modules

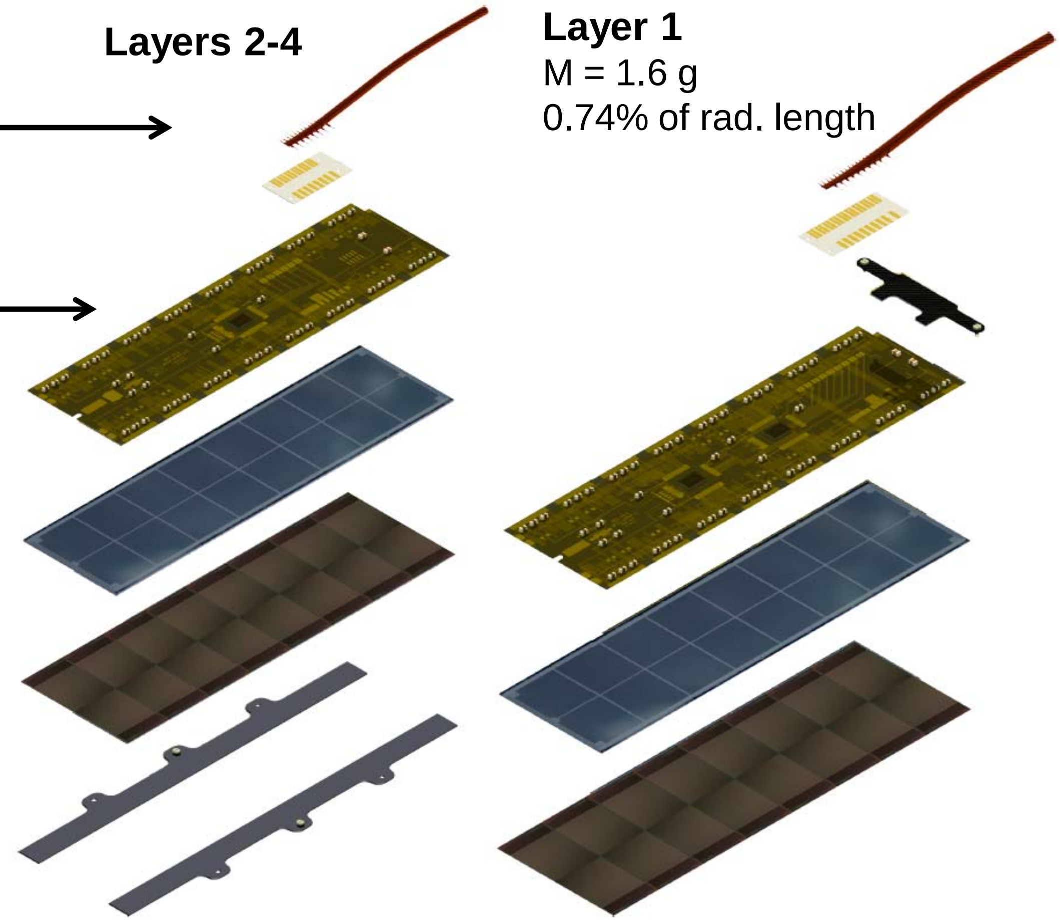
Power & data cable
Copper-cladded Al (125 & 360µm diam.)

PCB with data manager chips
3 x 2µm Cu layers

n+-in-n silicon sensor (as today)
Active area: 16.2 x 64.8 mm^2
100µm x 150µm pixels
66 560 pixels per sensor

16 readout chips (ROCs)
Bump-bonded to sensor
Thinned to 180µm & 75µm (L1)

Si_3N_4 base-strips, 250µm thick
or carbon fiber clip (L1)



Pixel Modules

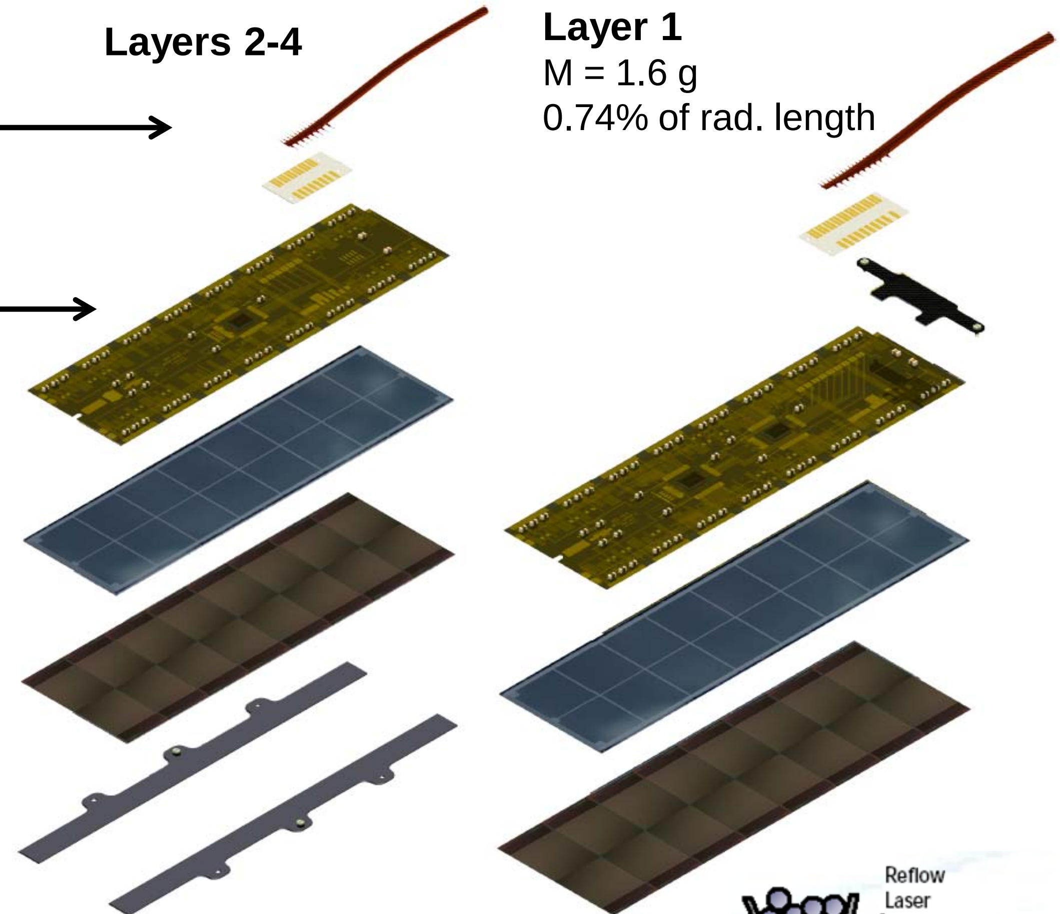
Power & data cable
Copper-cladded Al (125 & 360µm diam.)

PCB with data manager chips
3 x 2µm Cu layers

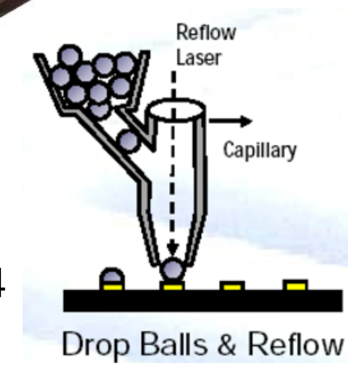
n+-in-n silicon sensor (as today)
Active area: 16.2 x 64.8 mm^2
100µm x 150µm pixels
66 560 pixels per sensor

16 readout chips (ROCs)
Bump-bonded to sensor
Thinned to 180µm & 75µm (L1)

Si_3N_4 base-strips, 250µm thick
or carbon fiber clip (L1)

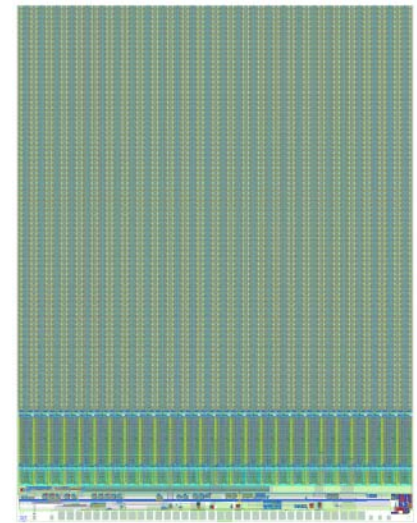


- In total 1 846 modules and 124 million channels
- Same module geometry for barrel and end caps → simplification
- Qualification of bump-bonding (e.g. laser jet method) → mass production 2014



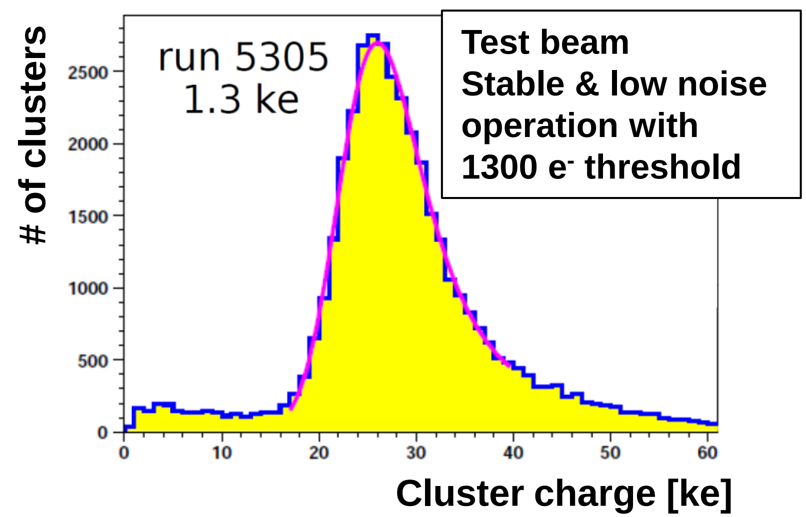
The Readout Chip

- **New readout chip based on present PSI46 ROC**
  - Column drain architecture (as before)
  - Chip readout: 40 MHz analog → 160 Mbit/s digital
  - Increase of data buffer and time stamp buffer depth
  - Smaller cross-talk + improved comparator → smaller threshold
  - Dedicated version for layer 1: 4x4 clusters transfered in parallel
  - Output data stream per module: 40MHz → 400 Mbit/s
- PSI46digV2 under test, so far performing well
- Chip version for layer 1 to be submitted 11/2013



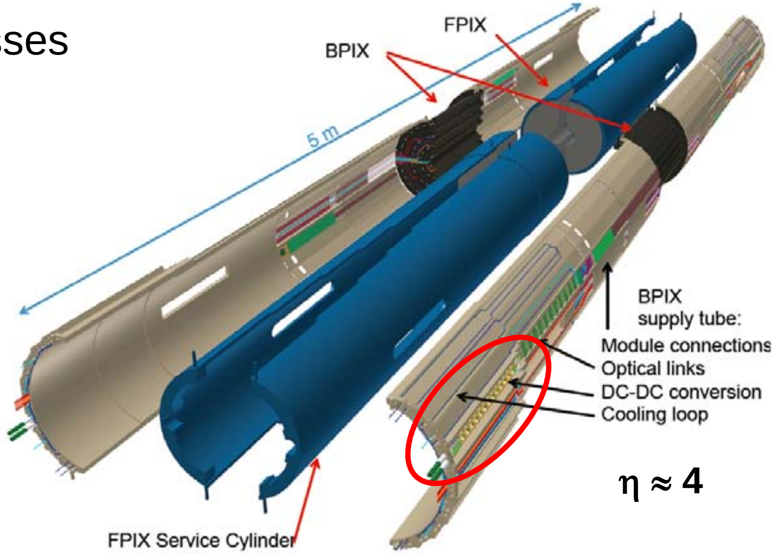
simulation

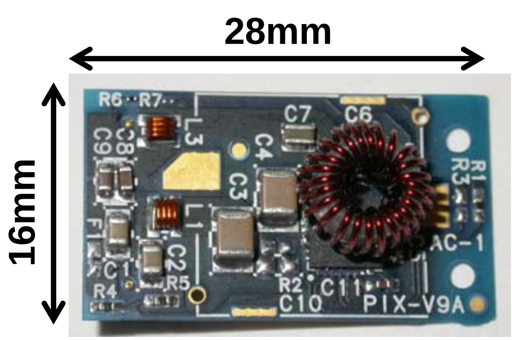
Detector	% Data loss for ($cm^{-2}s^{-1}$ @ ns)		
	1×10^{34} @ 25	2×10^{34} @ 25	2×10^{34} @ 50
Current detector			
BPIX1	4.0	16.0	50.0
Upgrade detector			
BPIX1	1.19	2.38	4.76
BPIX2	0.23	0.46	0.93

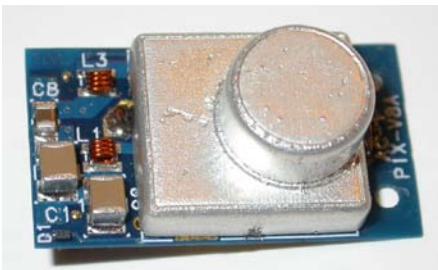


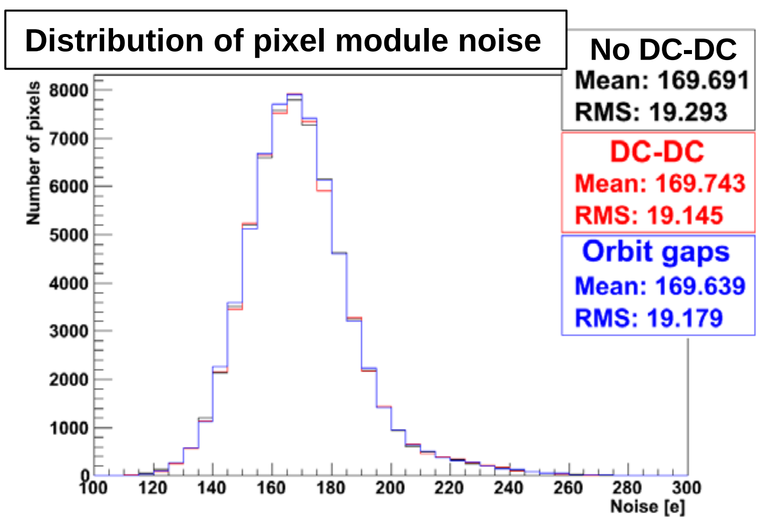
DC-DC Conversion Powering

- Factor 1.9 more channels → factor 4 larger ohmic losses
- Cables & power supplies to be re-used →
  DC-DC conversion: P = (r·U) x (I/r) with r = 3-4
  ➔ losses reduced by factor of ≈ 10
    - Buck converters convert 10V to 2.5V & 3.0V
    - 1 converter powers 1-4 pixel modules
    - ASIC by CERN
    - Power efficiency ≈ 80%
    - Good performance, including system tests with pixel modules









The Phase-2 Tracker Upgrade

Requirements:

- Radiation-hardness compatible with 3000 fb^{-1}
- High granularity compatible with few % occupancy at $5 \cdot 10^{34}$ $cm^{-2}s^{-1}$
  - Resolve 100-200 collisions per bunch crossing
- Reduction of material, to improve tracking performance at low p_T
- Provide tracker input to Level 1 (L1) trigger → reduction of trigger rates without loss of performance

The Phase-2 Tracker Upgrade

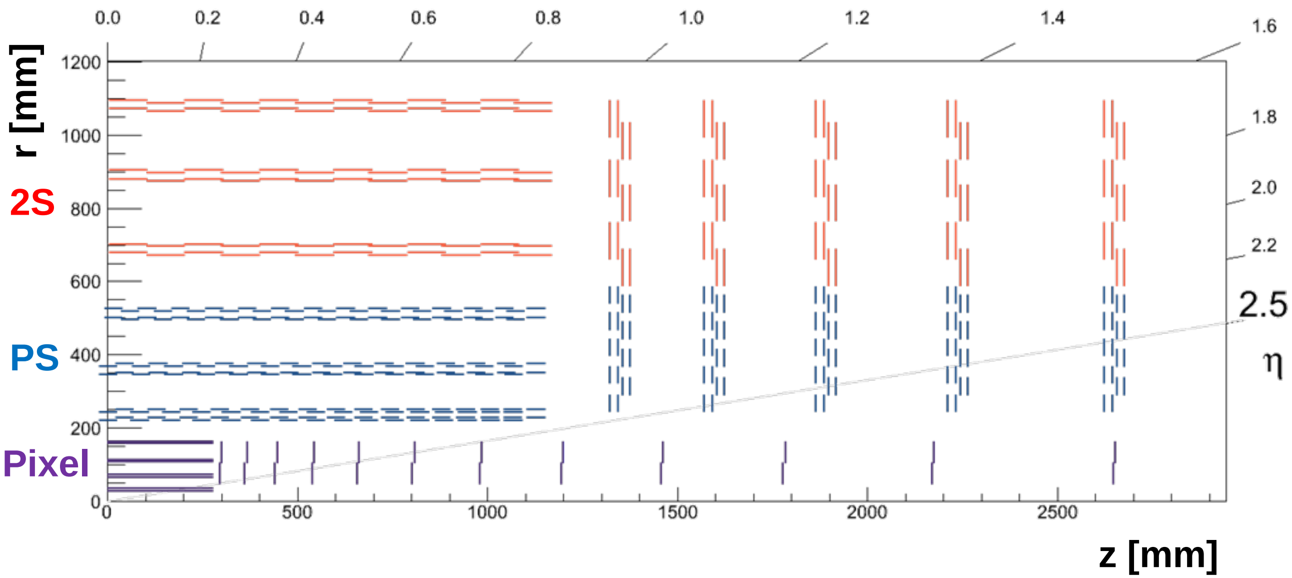
Requirements:

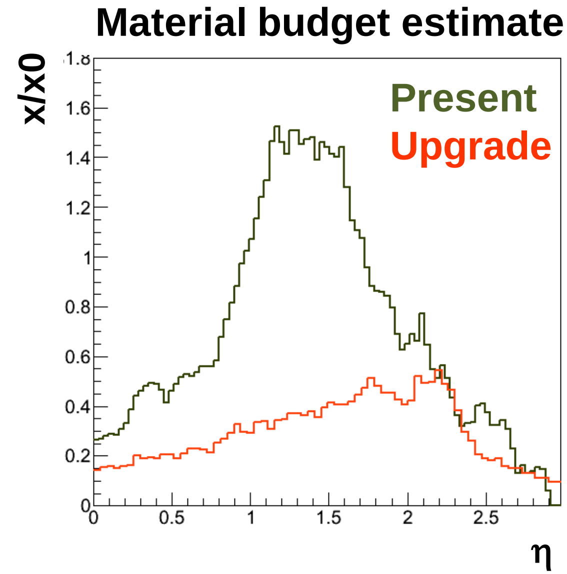
- Radiation-hardness compatible with 3000 fb^{-1}
- High granularity compatible with few % occupancy at $5 \cdot 10^{34}$ $cm^{-2}s^{-1}$
    - Resolve 100-200 collisions per bunch crossing
- Reduction of material, to improve tracking performance at low p_T
- Provide tracker input to Level 1 (L1) trigger → reduction of trigger rates without loss of performance

Basic concept:

- Tracker provides “readout data“ when triggered and “L1 trigger data“ @ 40MHz
- Local rejection of low p_T tracks to reduce volume of trigger data
- Discrimination on dedicated “p_T modules“ (details later)
- Level 1 tracks with $p_T > 2$ GeV are formed in the back-end

Tracker Layout

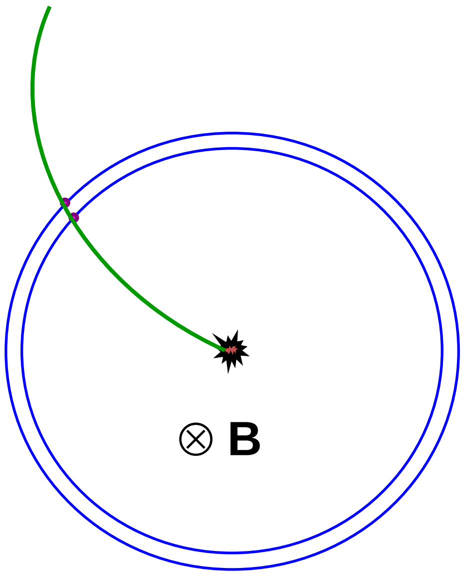




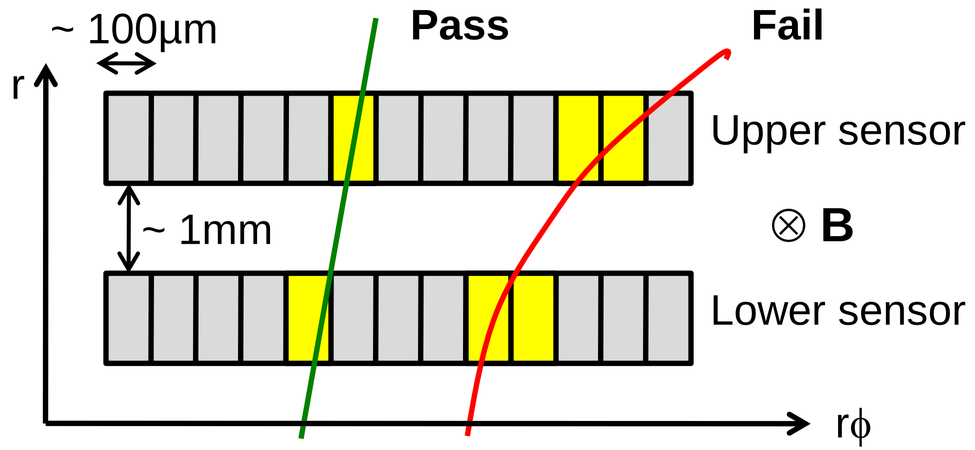
- **Baseline layout is a classical barrel + endcap layout with 5 disks**
  - Better performance at lower power, material & cost than a long barrel geometry
  - 15 348 modules, 58kW of front-end power (today: 15 148 modules, 33kW)
  - Option to extend pixel coverage to $\eta \approx 4$ is under consideration (baseline: $\eta < 2.5$)
- Two basic module types in outer tracker:
  - Modules with 2 strip sensors back-to-back ("2S p_T-modules")
  - Modules with 1 pixel and 1 strip sensor back-to-back ("PS p_T-modules")

Track Trigger

- Currently tracker data is used at High Level Trigger (HLT) only
  → too large trigger rates at phase-2 conditions
- Solution: tracker provides data to L1 trigger
- Data reduction by rejection of low p_T tracks exploiting bending in B field
- Compare hit patterns in closely spaced layers → 2-cluster tracklets (“stubs“)
- Tracks are formed from stubs at back-end, e.g. with associative memories



rϕ-view

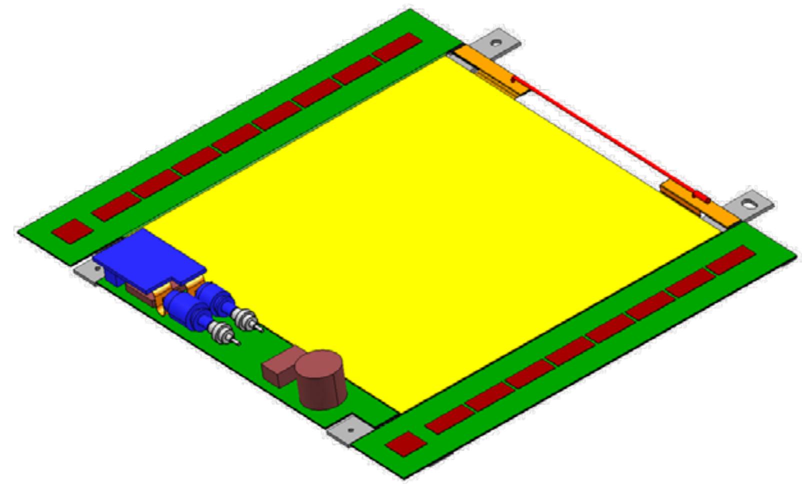


hit offset depends on radius
→ optimize search window or sensor spacing per layer

p_T -Modules

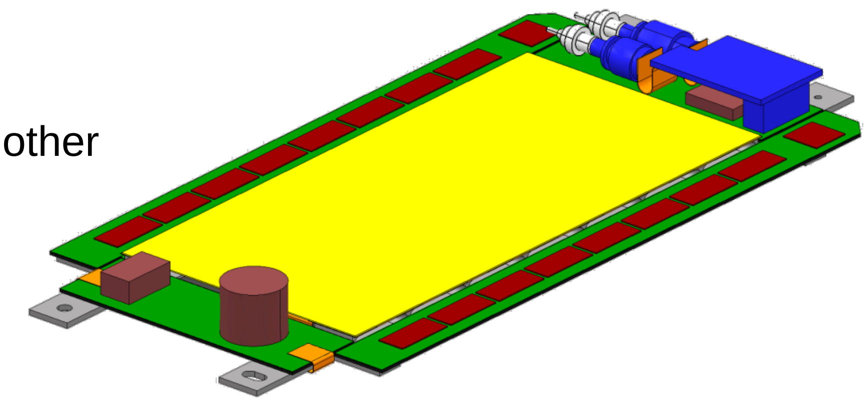
2S p_T -module

- For r > 40cm
- 2 strip sensor on top of each other
- Sensors wire-bonded to hybrid from top & bottom
- Strip dimensions: 5cm x 90µm
- 10 cm x 10 cm



PS p_T -module

- For r > 20cm
- 1 strip sensor and 1 pixel sensor on top of each other
- Strip dimensions: 2.5cm x 100µm
- Pixel dimensions: 1.5mm x 100µm
- Provides z information
- 5 cm x 10 cm

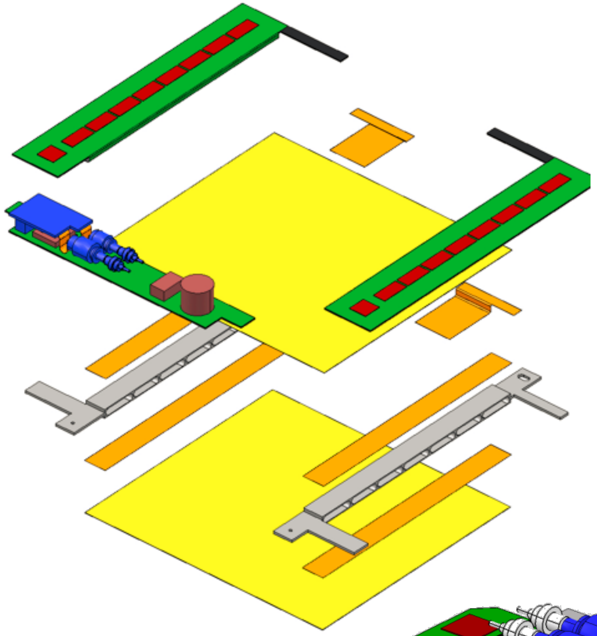


2S p_T -module is more advanced → will concentrate on 2S p_T -module

p_T -Modules

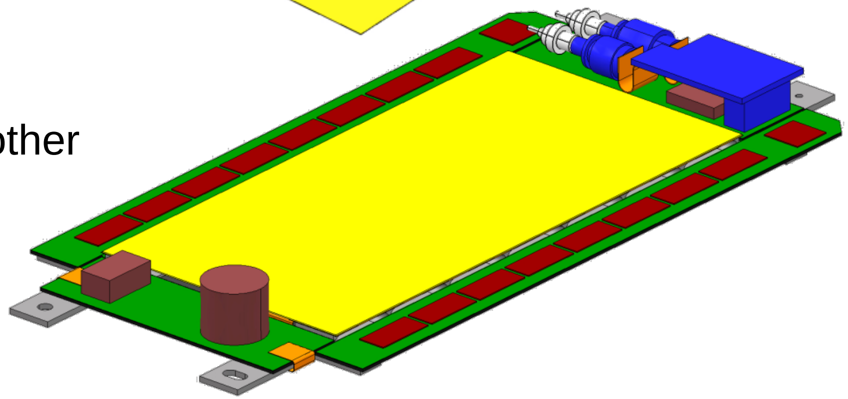
2S p_T -module

- For r > 40cm
- 2 strip sensor on top of each other
- Sensors wire-bonded to hybrid from top & bottom
- Strip dimensions: 5cm x 90µm
- 10 cm x 10 cm



PS p_T -module

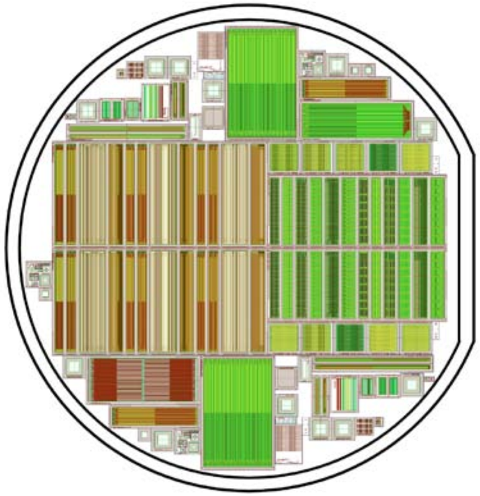
- For r > 20cm
- 1 strip sensor and 1 pixel sensor on top of each other
- Strip dimensions: 2.5cm x 100µm
- Pixel dimensions: 1.5mm x 100µm
- Provides z information
- 5 cm x 10 cm



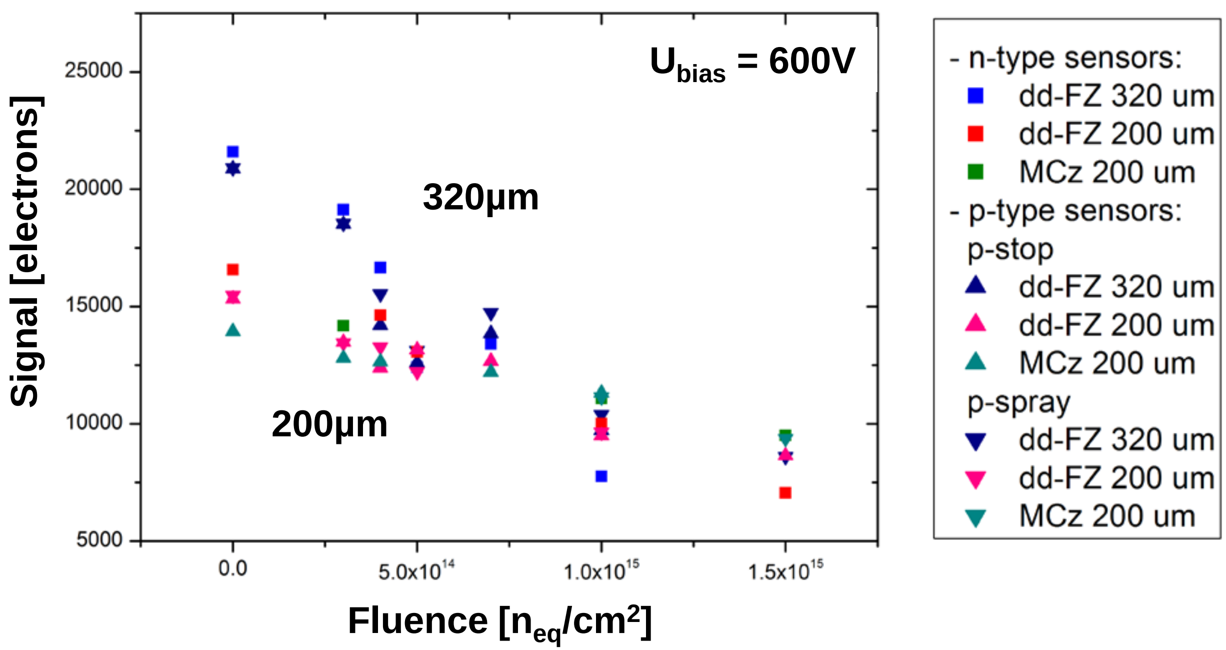
2S p_T -module is more advanced → will concentrate on 2S p_T -module

Sensors for Phase-2 Outer Tracker

- Test campaign to identify **silicon sensors** for phase-2 outer tracker
- Comparison of sensors from same supplier (HPK)
- Floatzone (FZ), Magnetic Czochralski (MCz), Epitaxial
- Different polarities, thicknesses and geometries
- Irradiation with protons and neutrons, various steps
  e.g. r = 20cm: 1.5×10^{15} neq/cm^2



→ **Several viable options identified, decision in August**

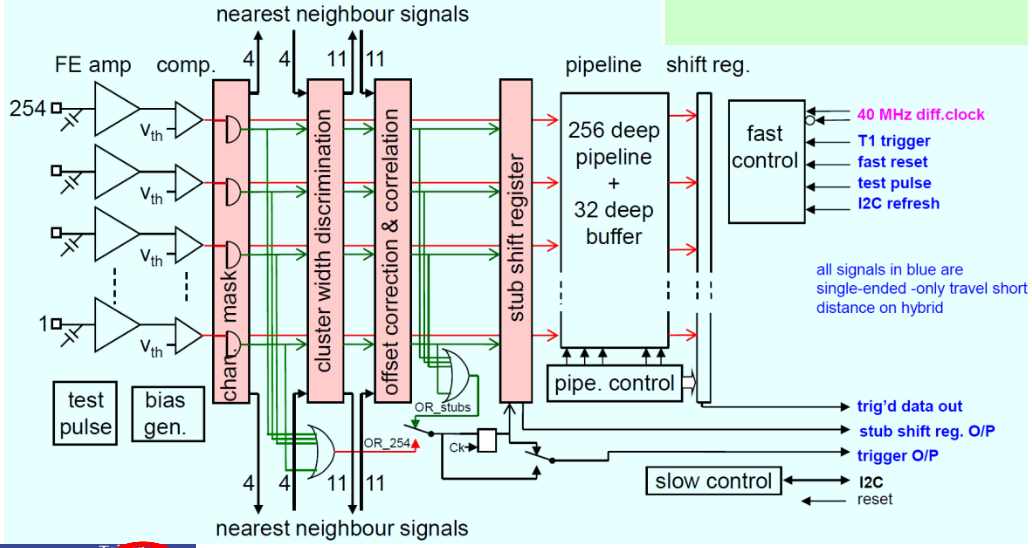


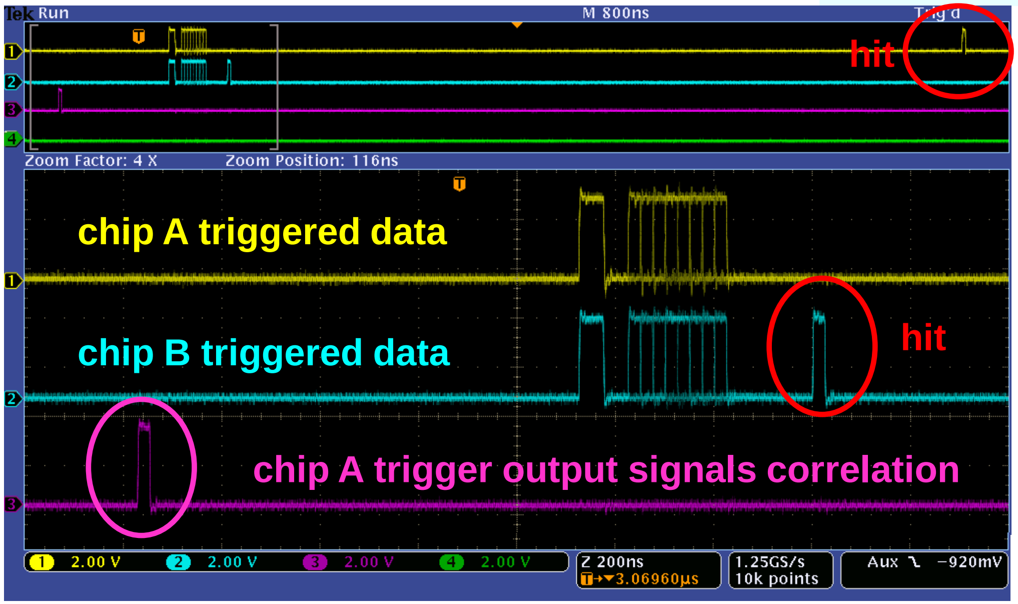
dd=deep diffused

Expected noise level ~ 1ke

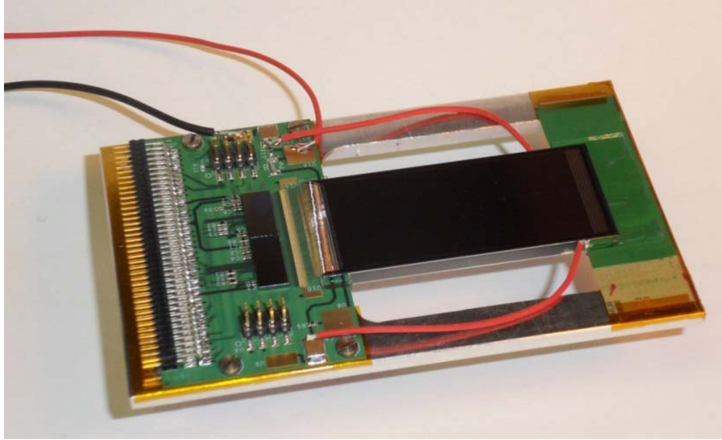
The CMS Binary Chip (CBC2)

- 130nm CMOS, C4 bump-bonds
- Unsparsified binary readout
- Receives data from both sensors
- Performs cluster correlation with programmable window width and offset
- Chip works, tests are ongoing
- Tests with charge injection & cosmics: stub finding works!





Mini-module with 2 CBC2s + hybrid prototype + test sensor



Conclusions

- **Phase-1 pixel detector is well under way**
- **New geometry, improved readout chip and reduction of material leads to improved performance**
- **Target installation date: 2016/2017 extended technical stop**

Conclusions

- Phase-1 pixel detector is well under way
- New geometry, improved readout chip and reduction of material leads to improved performance
- Target installation date: 2016/2017 extended technical stop

- R&D on phase-2 pixel detector has started
- Common R&D project on chip development with ATLAS

Conclusions

- Phase-1 pixel detector is well under way
- New geometry, improved readout chip and reduction of material leads to improved performance
- Target installation date: 2016/2017 extended technical stop

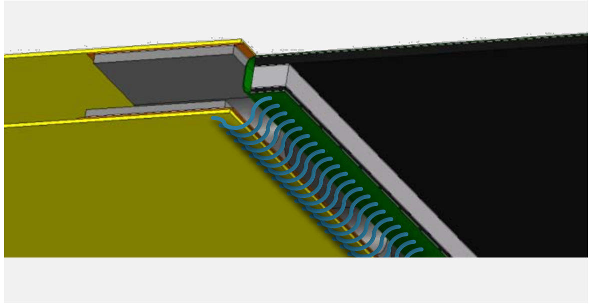
- R&D on phase-2 pixel detector has started
- Common R&D project on chip development with ATLAS

- Phase-2 outer tracker based on silicon sensors
- Baseline layout and baseline module design has recently been chosen
- Very active R&D on many fronts (could show only few highlights)
- Track trigger requirement presents an unprecedented challenge
- Technical proposal in 2014

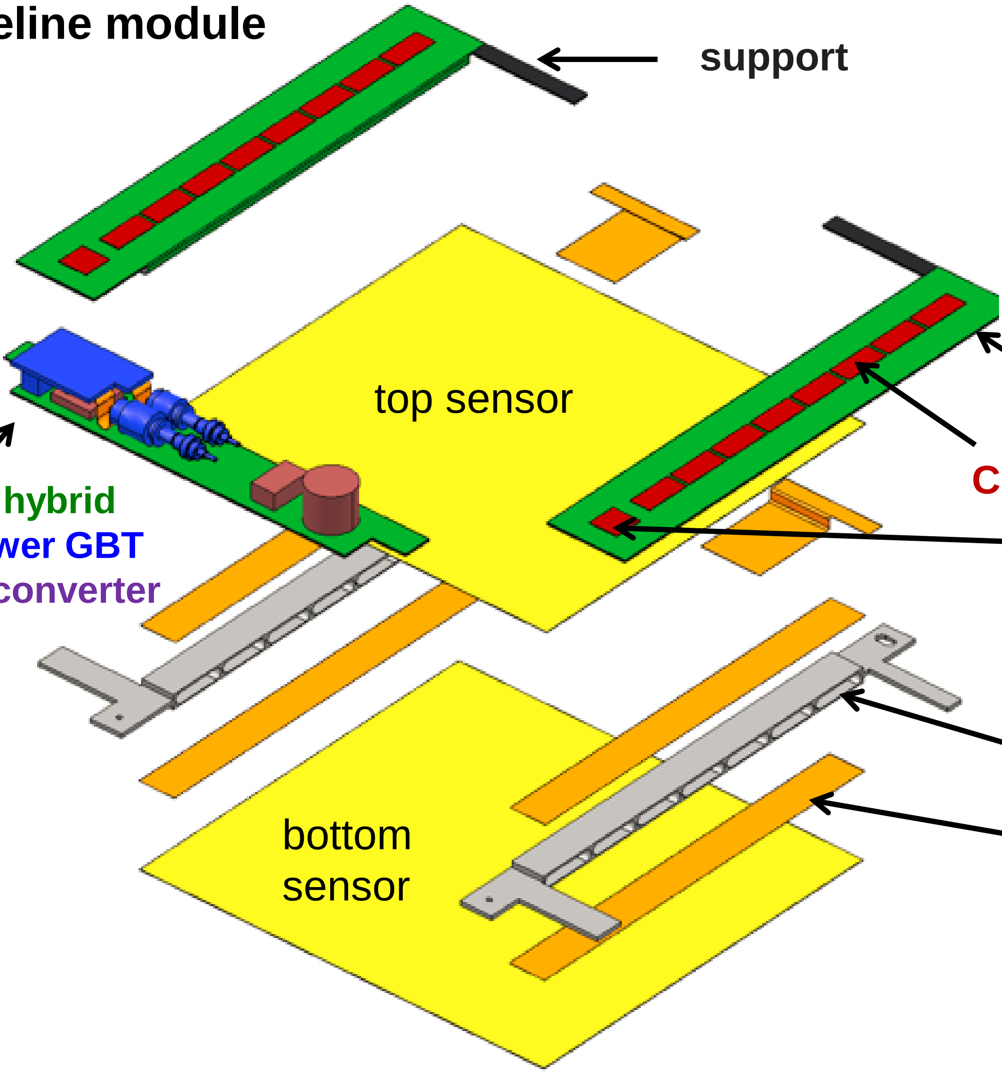
Additional Material

2S p_T -Modules

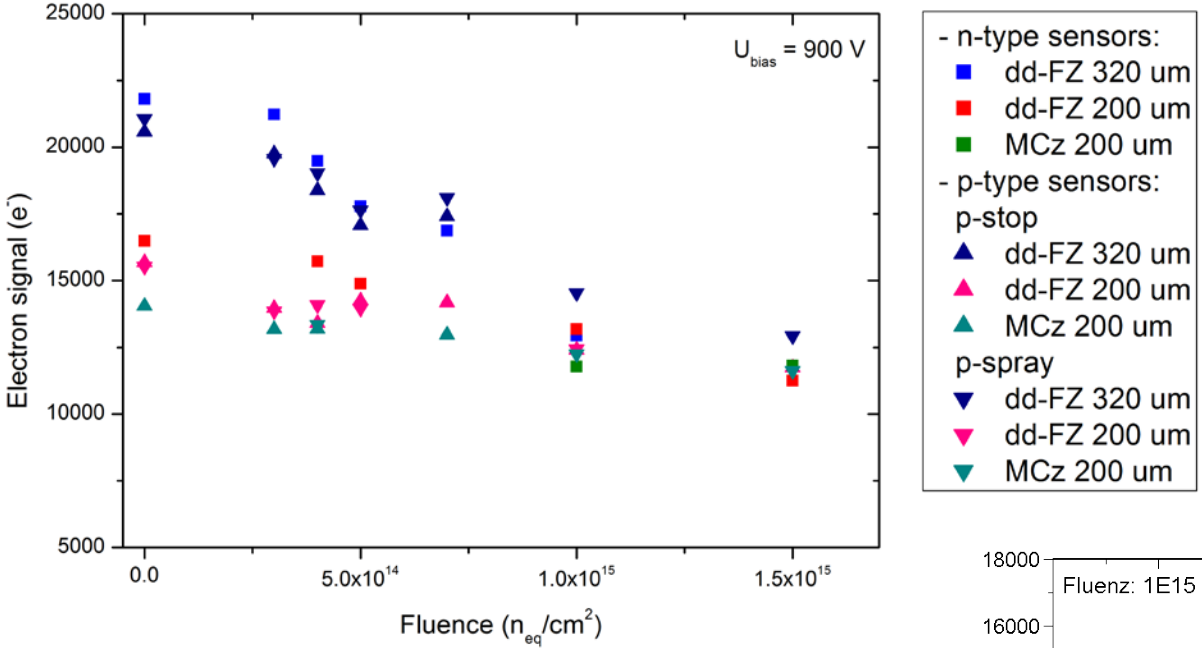
Sensors are wire-bonded to hybrid from top and bottom

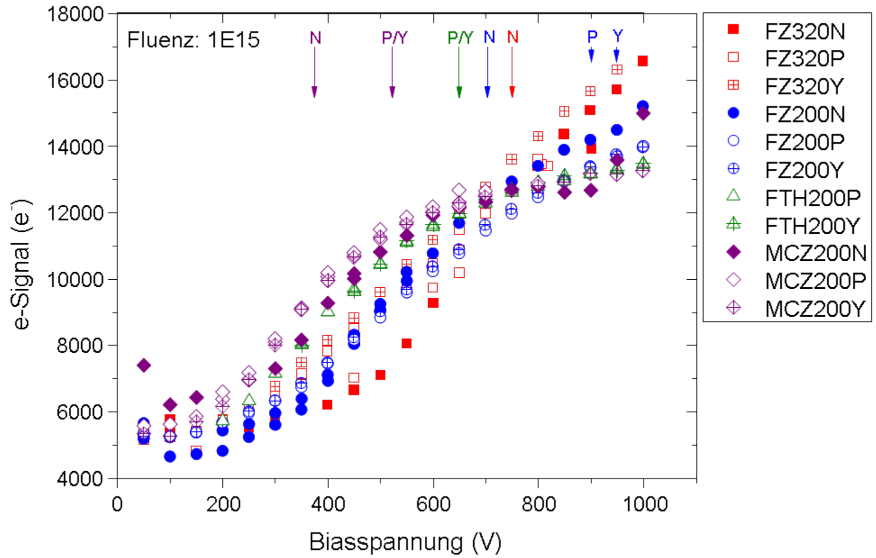


Baseline module



Sensors for Phase-2 Outer Tracker





Stub Processing at Back-End

- Reconstruct L1 tracks within trigger latency of 10 μsecs (today: 3.2μsec)
- L1 tracks are then matched with calorimeter and muon trigger objects
- Requires mapping of detector geometry into trigger towers
- Associative memories (AM) could be used for fast pattern recognition → then track fit
    - Estimate 100M patterns for the tracker