Upgrade of the CMS Tracker

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## The CMS Tracker Upgrade: Overview

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<thead>
<tr>
<th>Year</th>
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<td>&quot;Phase-1&quot;</td>
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| 2017 | LS1 | "Phase-1"  
Data taking  
≈ 500 fb⁻¹  
Exchange of innermost pixel layer after ~ 250fb⁻¹ |
| 2018 | LS2 | |
| 2019 | Data taking | Installation of a new CMS tracker  
"Phase-2"  
≈ 3000 fb⁻¹  
• Phase-2 pixel detector  
• Phase-2 outer tracker  
• Track trigger |
| 2020 | Data taking | "Phase-2"  
≈ 3000 fb⁻¹ |
| 2021 | | |
| 2022 | LS3 | |
| 2023 | | |
| 2024 | | |

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<tr>
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<td>“Phase-2”</td>
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**Red = covered in this presentation**
• Present pixel detector was designed for $1 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1} @ 25\text{ns}$ bunch spacing

• Conditions at LHC Phase-1: $2 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1} @ 25$ or $50\text{ns}$ → 50 or 100 pile-up events; int. luminosity of 500 fb$^{-1}$ and hit rates of $\approx 600 \text{ MHz/cm}^2$ → data losses of up to 50%

→ “Evolutionary upgrade“ with minimal impact on data taking
The Phase-1 Pixel Upgrade

- Present pixel detector was designed for $1 \cdot 10^{34}$ cm$^{-2}$s$^{-1}$ @ 25ns bunch spacing
- Conditions at LHC Phase-1: $2 \cdot 10^{34}$ cm$^{-2}$s$^{-1}$ @ 25 or 50ns → 50 or 100 pile-up events; int. luminosity of 500 fb$^{-1}$ and hit rates of $\approx 600$ MHz/cm$^2$ → data losses of up to 50%

→ “Evolutionary upgrade“ with minimal impact on data taking

- 4 hit coverage → robust tracking
- Smaller radius of innermost layer → better vertex resolution & b-tagging efficiency
- Improved readout chip → recovery of hit efficiency
- Evaporative CO$_2$ cooling, relocation of patch panels, lighter mechanics → less material
- Novel powering scheme allows to power factor of 1.9 more channels
Simulated Performance

Tracking efficiency

- Efficiency vs. $\eta$
- Current Pixel Detector: $\pm 0.5$ efficiency drop
- Upgrade Pixel Detector: $\pm 0.3$ efficiency drop

Fake rate

- $2 \times 10^{34}$ cm$^{-2}$s$^{-1}$ (25 ns)
- ttbar sample
- 50 pileup events

Material budget

- Radiation length
- Current pixel detector: $\pm 0.1$ deviation
- Upgrade pixel detector: $\pm 0.2$ deviation

B-tagging efficiency vs. pile-up

- Efficiency (%) vs. average pileup
- Current Detector: light quark mis-tag = 1%
- Upgrade Detector: light quark mis-tag = 0.1%
Pixel Modules

Layers 2-4

Layer 1
M = 1.6 g
0.74% of rad. length
Pixel Modules

Layers 2-4

Layer 1
M = 1.6 g
0.74% of rad. length

Si$_3$N$_4$ base-strips, 250µm thick or carbon fiber clip (L1)
**Pixel Modules**

**Layers 2-4**
- M = 1.6 g
- 0.74% of rad. length

**Layer 1**
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16 readout chips (ROCs)
- Bump-bonded to sensor
- Thinned to 180µm & 75µm (L1)

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**Pixel Modules**

**Layers 2-4**

- **n+-in-n silicon sensor (as today)**
  - Active area: $16.2 \times 64.8$ mm²
  - $100\mu$m x $150\mu$m pixels
  - 66,560 pixels per sensor

- **16 readout chips (ROCs)**
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5
**Pixel Modules**

**Layers 2-4**
- Power & data cable
  - Copper-cladded Al (125 & 360µm diam.)

**Layer 1**
- **M = 1.6 g**
- **0.74% of rad. length**

- PCB with data manager chips
  - 3 x 2µm Cu layers

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- **Layers 2-4**
  - **Layer 1**
    - M = 1.6 g
    - 0.74% of rad. length

- **In total 1 846 modules and 124 million channels**
- **Same module geometry for barrel and end caps → simplification**
- **Qualification of bump-bonding (e.g. laser jet method) → mass production 2014**

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The Readout Chip

- **New readout chip based on present PSI46 ROC**
  - Column drain architecture (as before)
  - Chip readout: 40 MHz analog → 160 Mbit/s digital
  - Increase of data buffer and time stamp buffer depth
  - Smaller cross-talk + improved comparator → smaller threshold
  - Dedicated version for layer 1: 4x4 clusters transferred in parallel
  - Output data stream per module: 40MHz → 400 Mbit/s

- PSI46digV2 under test, so far performing well
- Chip version for layer 1 to be submitted 11/2013

<table>
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<tr>
<th>Detector</th>
<th>% Data loss for (cm(^{-2})s(^{-1}) @ ns)</th>
</tr>
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<tbody>
<tr>
<td></td>
<td>1 × 10(^{34}) @ 25</td>
</tr>
<tr>
<td><strong>Current detector</strong></td>
<td></td>
</tr>
<tr>
<td>BPIX1</td>
<td>4.0</td>
</tr>
<tr>
<td><strong>Upgrade detector</strong></td>
<td></td>
</tr>
<tr>
<td>BPIX1</td>
<td>1.19</td>
</tr>
<tr>
<td>BPIX2</td>
<td>0.23</td>
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Test beam
Stable & low noise operation with 1300 e\(^{-}\) threshold

Cluster charge [ke]

run 5305
1.3 ke

# of clusters
• Factor 1.9 more channels → factor 4 larger ohmic losses
• Cables & power supplies to be re-used → DC-DC conversion: \( P = (r \cdot U) \times (I/r) \) with \( r = 3-4 \) → losses reduced by factor of \( \approx 10 \)
  • Buck converters convert 10V to 2.5V & 3.0V
  • 1 converter powers 1-4 pixel modules
  • ASIC by CERN
  • Power efficiency \( \approx 80\% \)
  • Good performance, including system tests with pixel modules

\[ \eta \approx 4 \]

Distribution of pixel module noise

<table>
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<tr>
<th>No DC-DC</th>
<th>DC-DC</th>
<th>Orbit gaps</th>
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<td>Mean: 169.691</td>
<td>Mean: 169.743</td>
<td>Mean: 169.639</td>
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The Phase-2 Tracker Upgrade

Requirements:

- Radiation-hardness compatible with 3000 fb\(^{-1}\)
- High granularity compatible with few % occupancy at \(5 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1}\)
  - Resolve 100-200 collisions per bunch crossing
- Reduction of material, to improve tracking performance at low \(p_T\)
- Provide tracker input to Level 1 (L1) trigger \(\rightarrow\) reduction of trigger rates without loss of performance
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Basic concept:

• Tracker provides “readout data“ when triggered and “L1 trigger data“ $\leftrightarrow$ 40MHz
• Local rejection of low $p_T$ tracks to reduce volume of trigger data
• Discrimination on dedicated “$p_T$ modules“ (details later)
• Level 1 tracks with $p_T > 2$ GeV are formed in the back-end
• Baseline layout is a classical barrel + endcap layout with 5 disks
  • Better performance at lower power, material & cost than a long barrel geometry
  • 15 348 modules, 58kW of front-end power (today: 15 148 modules, 33kW)
  • Option to extend pixel coverage to $\eta \approx 4$ is under consideration (baseline: $\eta < 2.5$)

• Two basic module types in outer tracker:
  • Modules with 2 strip sensors back-to-back (“2S p_T -modules“)
  • Modules with 1 pixel and 1 strip sensor back-to-back (“PS p_T -modules“)
• Currently tracker data is used at High Level Trigger (HLT) only → too large trigger rates at phase-2 conditions
• Solution: tracker provides data to L1 trigger
• Data reduction by rejection of low $p_T$ tracks exploiting bending in B field
• Compare hit patterns in closely spaced layers → 2-cluster tracklets ("stubs")
• Tracks are formed from stubs at back-end, e.g. with associative memories
**p_T -Modules**

**2S p_T -module**

- For $r > 40cm$
- 2 strip sensor on top of each other
- Sensors wire-bonded to hybrid from top & bottom
- Strip dimensions: 5cm x 90µm
- 10 cm x 10 cm

**PS p_T -module**

- For $r > 20cm$
- 1 strip sensor and 1 pixel sensor on top of each other
- Strip dimensions: 2.5cm x 100µm
- Pixel dimensions: 1.5mm x 100µm
- Provides z information
- 5 cm x 10 cm

**2S p_T -module is more advanced → will concentrate on 2S p_T -module**
2S $p_T$-module

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2S $p_T$-module is more advanced $\rightarrow$ will concentrate on 2S $p_T$-module
Sensors for Phase-2 Outer Tracker

- Test campaign to identify **silicon sensors** for phase-2 outer tracker
- Comparison of sensors from same supplier (HPK)
- Floatzone (FZ), Magnetic Czochralski (MCz), Epitaxial
- Different polarities, thicknesses and geometries
- Irradiation with protons and neutrons, various steps e.g. r = 20cm: $1.5 \times 10^{15}$ neq/cm²

→ **Several viable options identified, decision in August**

\[ \text{Expected noise level} \sim 1\text{ke} \]
The CMS Binary Chip (CBC2)

- 130nm CMOS, C4 bump-bonds
- Unsparsified binary readout
- Receives data from both sensors
- Performs cluster correlation with programmable window width and offset
- Chip works, tests are ongoing
- Tests with charge injection & cosmics: stub finding works!

Mini-module with 2 CBC2s + hybrid prototype + test sensor
Conclusions

• Phase-1 pixel detector is well under way
• New geometry, improved readout chip and reduction of material leads to improved performance
• Target installation date: 2016/2017 extended technical stop
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• Common R&D project on chip development with ATLAS
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• Phase-2 outer tracker based on silicon sensors
• Baseline layout and baseline module design has recently been chosen
• Very active R&D on many fronts (could show only few highlights)
• Track trigger requirement presents an unprecedented challenge
• Technical proposal in 2014
Additional Material
2S $p_T$-Modules

Baseline module

Sensors are wire-bonded to hybrid from top and bottom

Hybrid

CMS Binary Chips (CBC)

Data concentrator chip

Cooling bridge and spacer

Kapton

Service hybrid
Low power GBT
DC-DC converter

Support from top and bottom

top sensor

bottom sensor

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Sensors for Phase-2 Outer Tracker

- **n-type sensors:**
  - dd-FZ 320 um
  - dd-FZ 200 um
  - MCz 200 um

- **p-type sensors:**
  - p-stop
    - dd-FZ 320 um
    - dd-FZ 200 um
    - MCz 200 um
  - p-spray
    - dd-FZ 320 um
    - dd-FZ 200 um
    - MCz 200 um

Fluence ($n_{eq}/cm^2$) vs. Electron signal ($e^-$).

Fluence: $1E15$
Stub Processing at Back-End

- Reconstruct L1 tracks within trigger latency of 10 µsecs (today: 3.2µsec)
- L1 tracks are then matched with calorimeter and muon trigger objects
- Requires mapping of detector geometry into trigger towers
- Associative memories (AM) could be used for fast pattern recognition → then track fit
  - Estimate 100M patterns for the tracker

Emulated pattern recognition efficiency for electrons
(Example: 5 end cap disks)

4 stubs out of 5
5 stubs out of 5