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(info@eps-hep2013.eu)

Radiation-hard Active Pixel Detectors based on HV-CMOS Technology for HL-LHC Detector Upgrades

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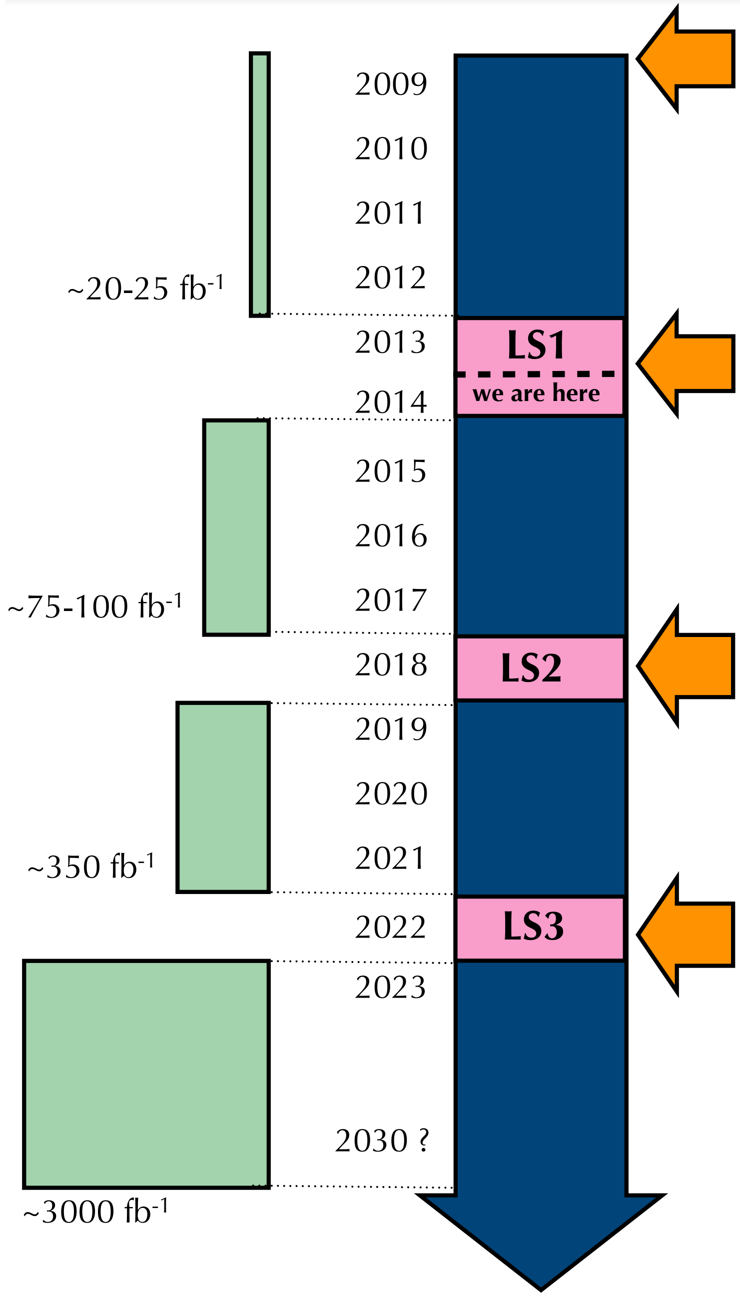
on behalf of the participating institutes:
U. Bonn, CERN, CPPM Marseille, U. Geneva, U. Glasgow, U. Heidelberg, LBNL

The High-Luminosity LHC (HL-LHC)



LHC startup $\sqrt{s} = 900\,\mathrm{GeV}$

$\sqrt{s} = 7 \sim 8\,\mathrm{TeV}$
$\mathcal{L} = 6 \times 10^{33}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$
Bunch spacing 50 ns

Go to design energy, nominal luminosity (**Phase-0**)

$\sqrt{s} = 13 \sim 14\,\mathrm{TeV}$
$\mathcal{L} \sim 1 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$
Bunch spacing 25 ns

Injector and LHC **Phase-1** upgrade to full design luminosity

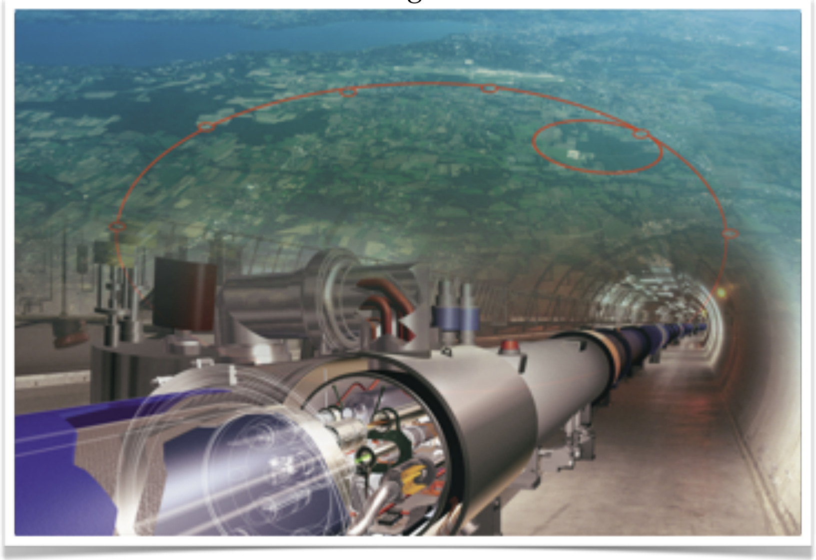
$\sqrt{s} = 14\,\mathrm{TeV}$
$\mathcal{L} \sim 2 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$
Bunch spacing 25 ns

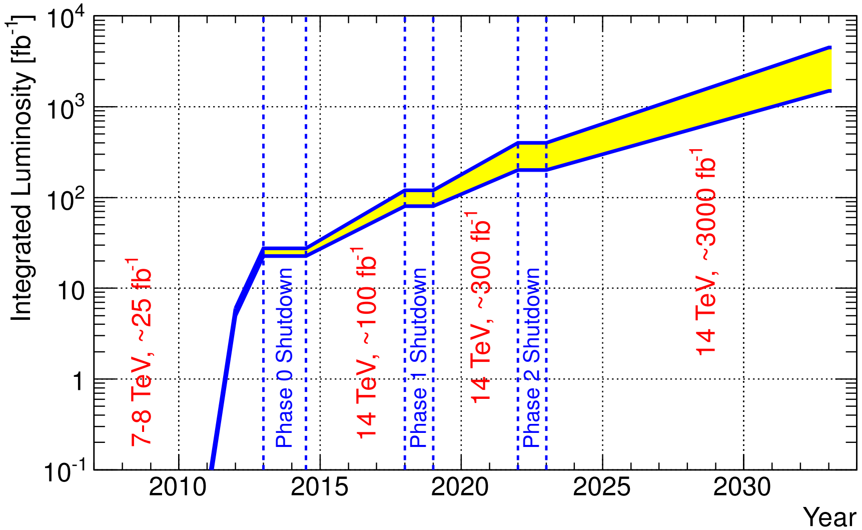
HL-LHC **Phase-2** upgrade, SC crab cavities

$\sqrt{s} = 14\,\mathrm{TeV}$
$\mathcal{L} = 5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$
Luminosity leveling

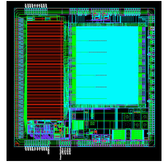
HE-LHC: $\sqrt{s} = 33\,\mathrm{TeV}$
300 - 3000 fb^{-1}

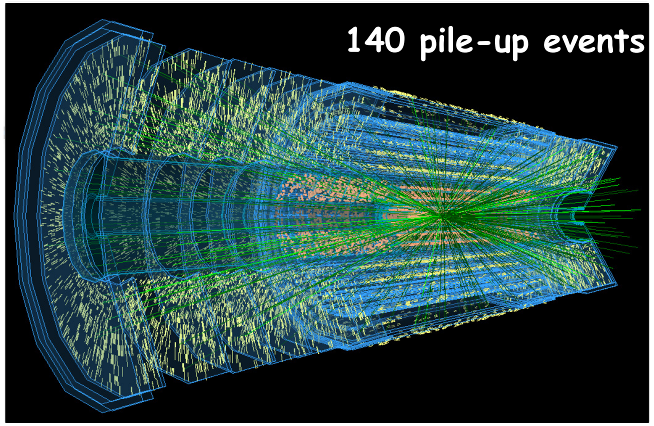
Large Hadron Collider (LHC)



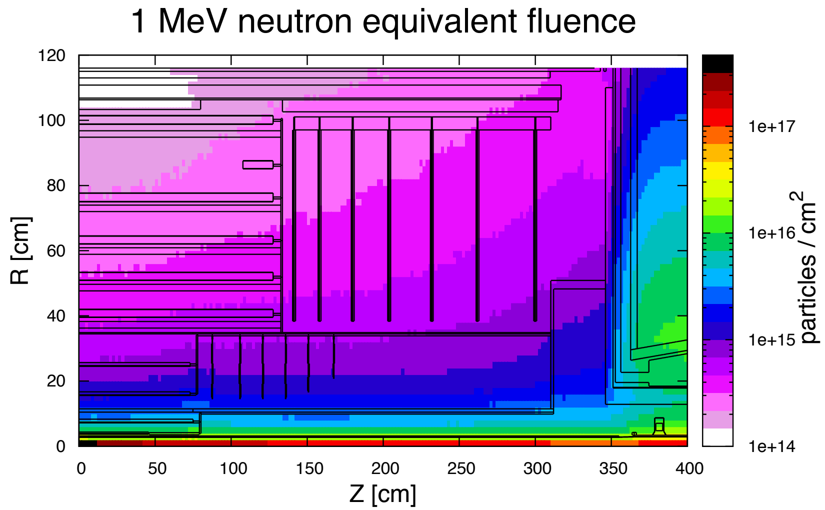


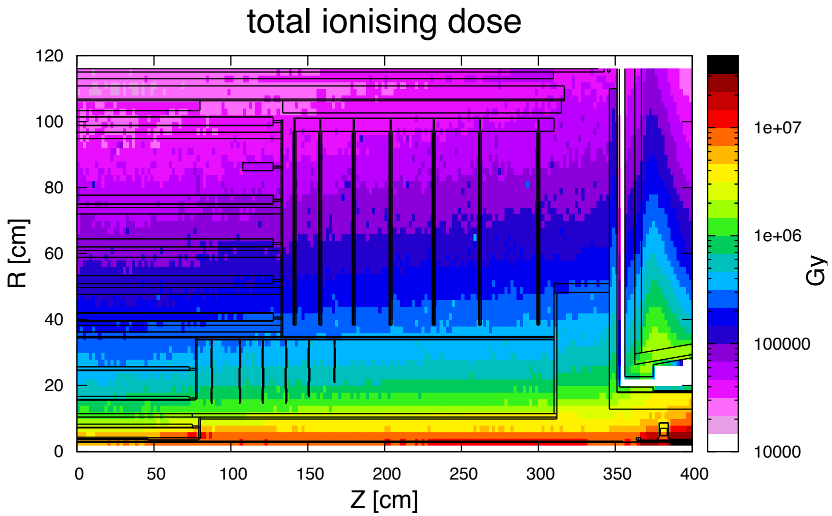
New ATLAS tracker



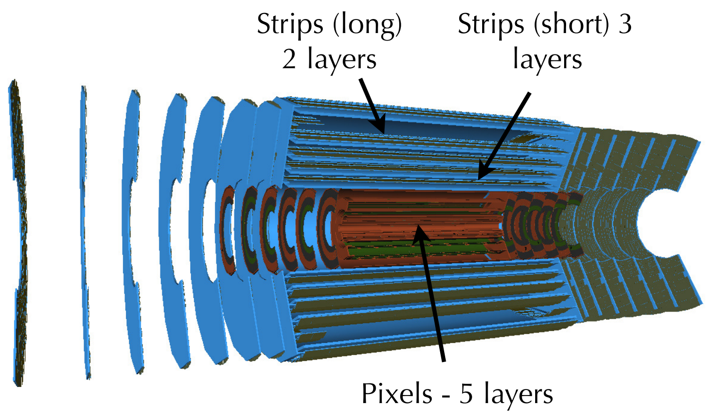


- Conditions at 5×10^{34} cm^{-2}s^{-1}:
  - radiation damage
  - channel occupancy
    - particle multiplicity > 10^5 particles $|\eta|<3.2$

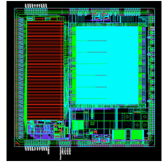




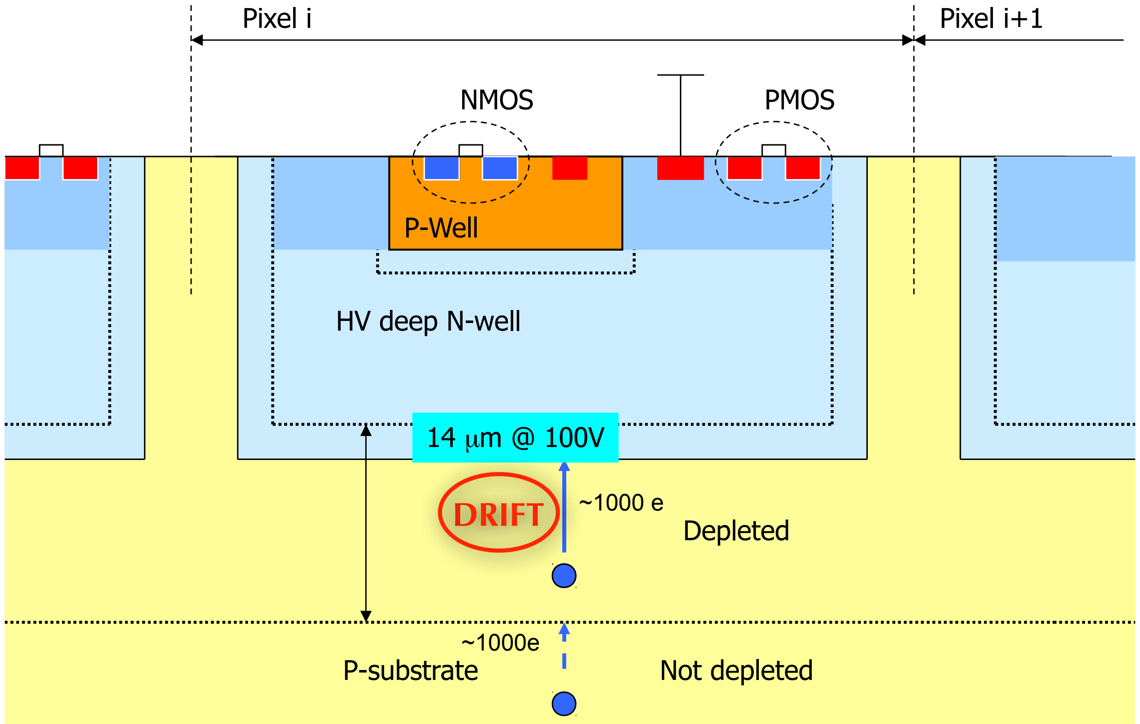
- New ATLAS Inner Detector
  - silicon-based tracker (pixels + strips)
  - maintain / improve current tracking capabilities
  - better detector granularity, radiation hardness
- New Detectors: lowest price while rad-hard !
  - possibility of existing industrialized processes ?



High-Voltage CMOS



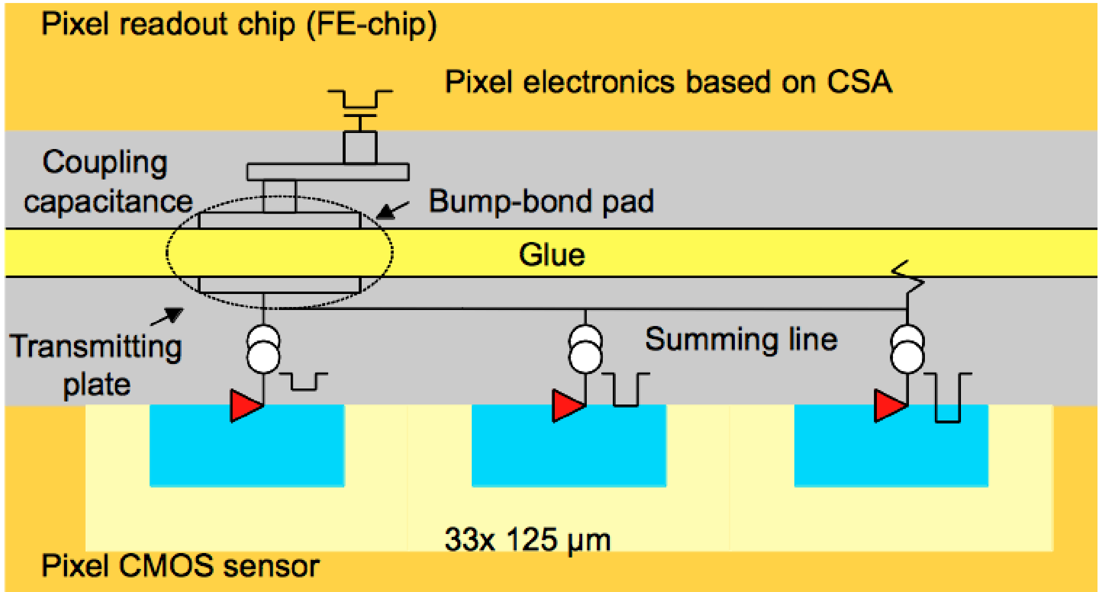
- High Voltage-CMOS (HV-CMOS) technology
  - standard industrialized process (low-cost, large availability)
- HV-CMOS as monolithic pixel particle detector
  - project initiated by I. Peric (U. Heidelberg)
  - sensor based on multiple-well structure
    - entire CMOS electronics inside the deep N-well ➡ "smart diode" ➡ "smart diode array"
      - PMOS transistors directly in the deep N-well
      - NMOS transistors within P-well embedded in deep N-well



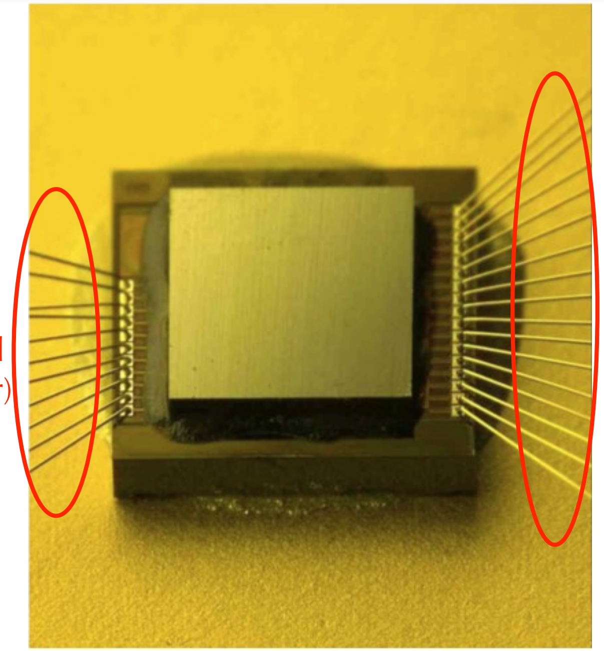
Technology	Austria Microsystems (AMS) + IBM 350 nm / 180 nm
Substrate resitivity	> 10 Ωcm
Pixel size	down to 20 μm
Depletion depth	~ 10 - 20 μm
Reverse bias voltage	~ 60 - 100 V
Charge collection time	~ 40 ps
Signal (mip)	~ 2000 e

Capacitively coupled detector

- Implementation of on-sensor CMOS electronics (e.g. charge sensitive amplifier, etc.) ➡ signal transmission by **capacitive (AC) coupling**
  - signal transmitted to the charge sensitive amplifier in the the readout ASIC
  - no need of costly bump-bonding process
- Gluing process:
  - alignment precision: $< 5\ \mu m$
  - glue layer thickness: $< 5\ \mu m$

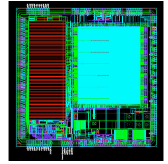


CCPD (Capacitive Coupled Pixel Detector)



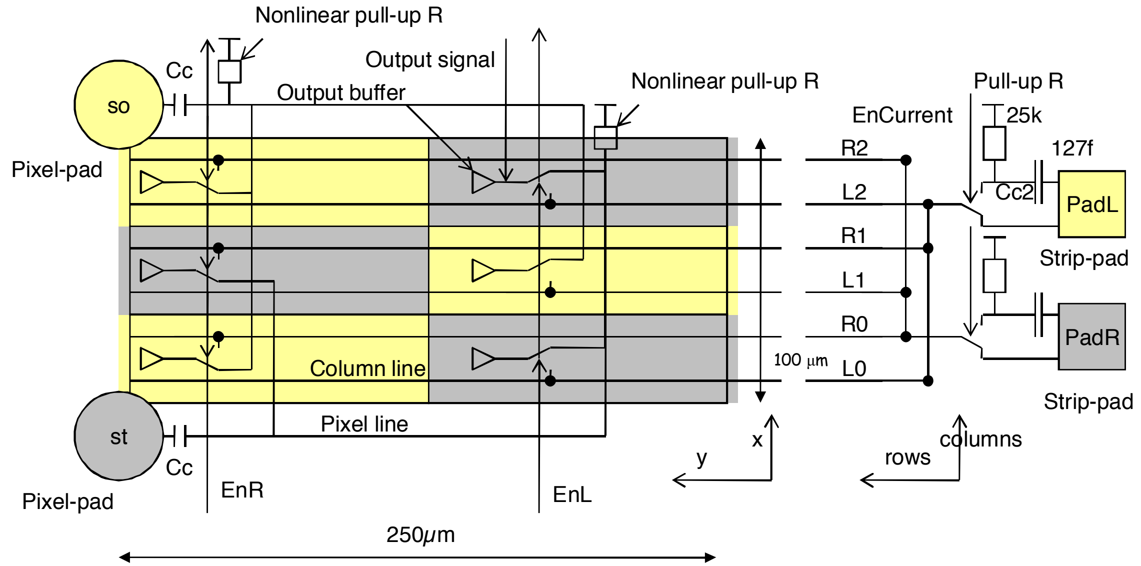
SNR: ~ 45 - 60

HV2FEI4 prototype chip

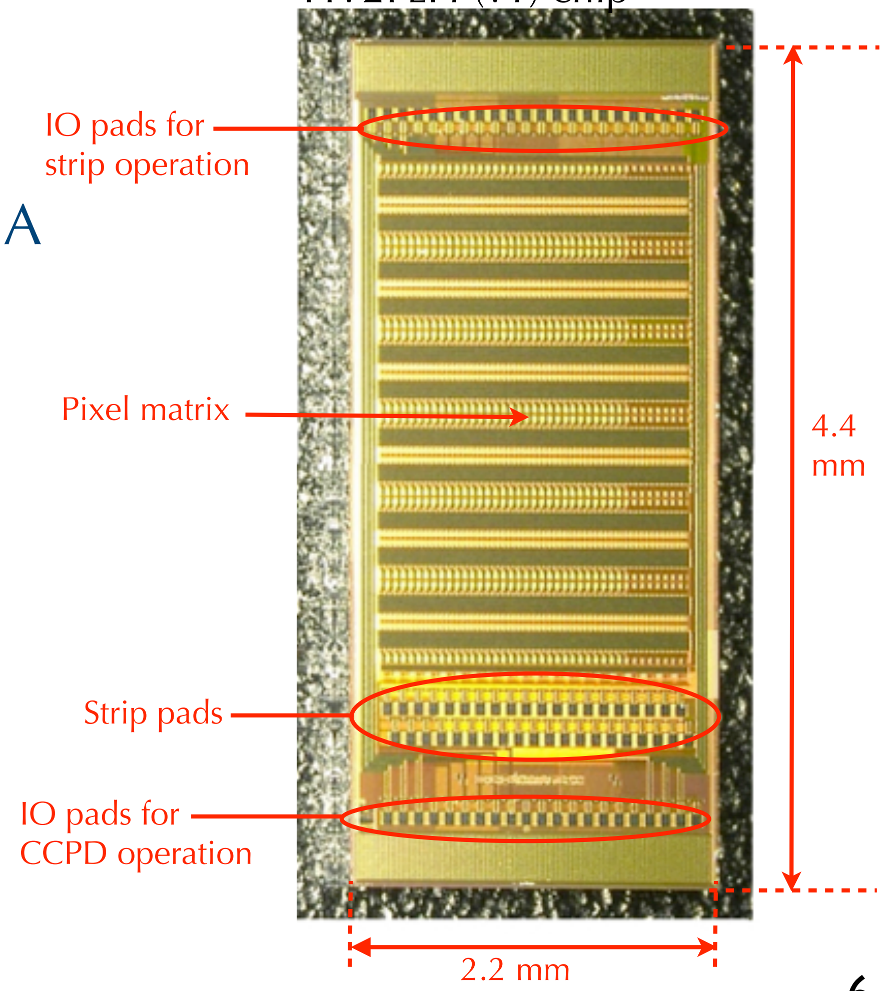


- Chip-size: 2.2x4.4 mm^2
  - pixel matrix: 60x24 sub-pixels (unit cell = 6 pixels, each 125 x 33 μm^2)
- HV2FEI4 compatible with:
  - ATLAS FEI4 (ATLAS pixel readout ASIC)
    - bump-bonding or capactive coupling
  - strip readout
- Charge sensitive amplifier, discriminator
- On-chip bias DAC, configuration via FPGA

Unit cell structure of the HV2FEI4 prototype



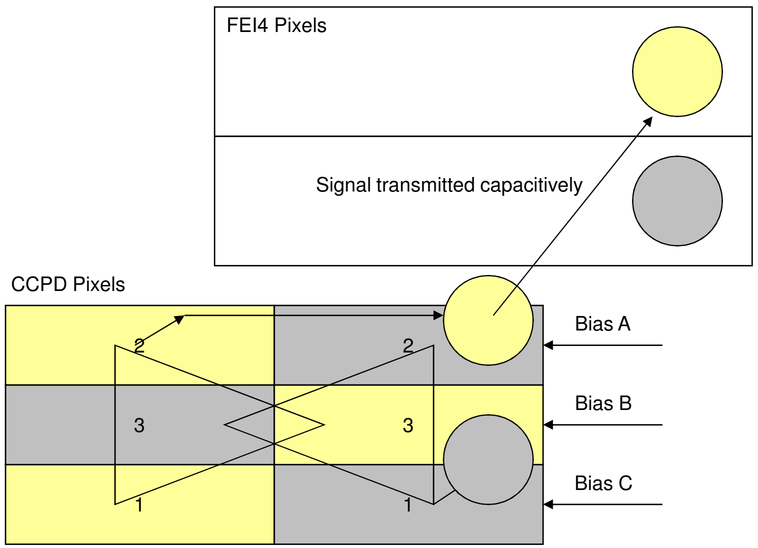
HV2FEI4 (v1) chip



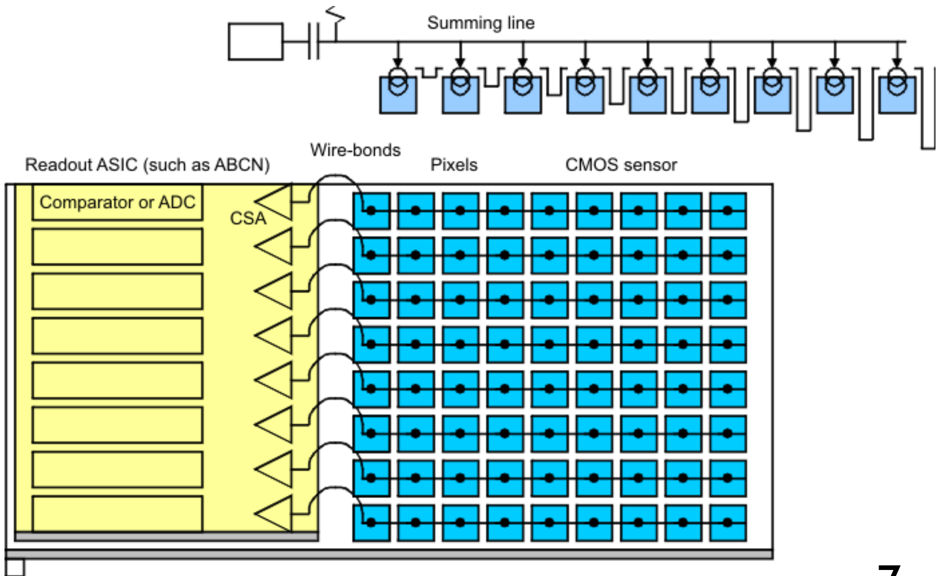
Readout modes

- Capactively coupled readout chip
  - unit cell corresponding to two ATLAS FEI4 readout-chip pixels
  - combine sensor sub-pixels for AC readout
  - different current amplitude per pixel ➡ hit position from pulse-height information
    - improvement in resolution without changes in readout chip
- Readout as a strip-like detector
  - sum all pixels in a row ➡ "virtual strip"
    - multiple connections possible (crossed-strips)
  - hit position along strip encoded as pulse-height ➡ Z-resolution improved

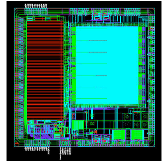
Pixel readout (AC coupling)



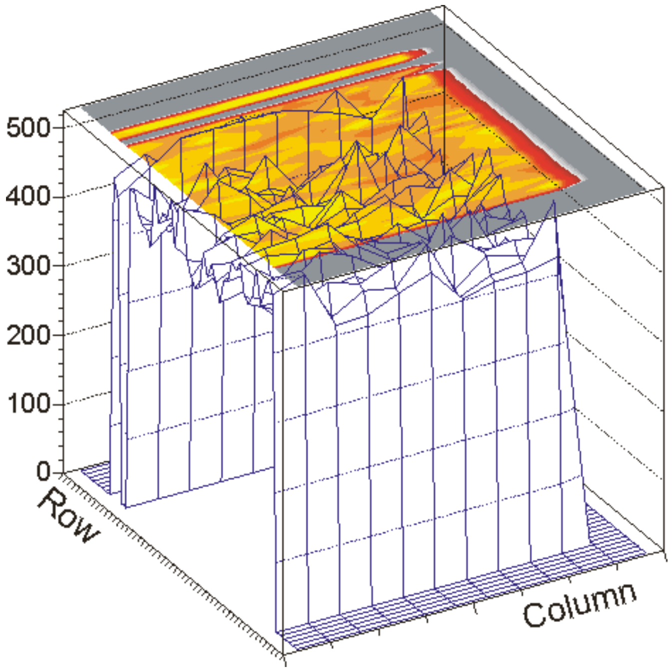
Strip readout

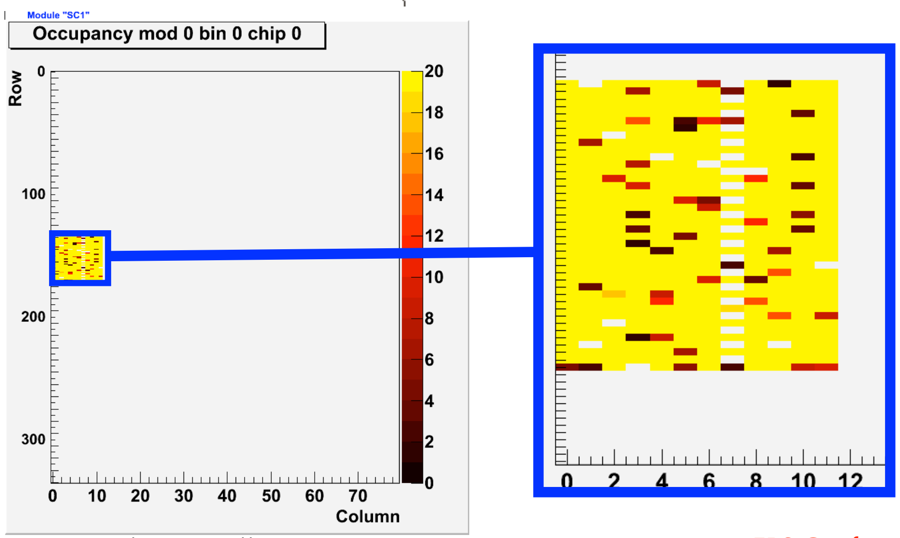


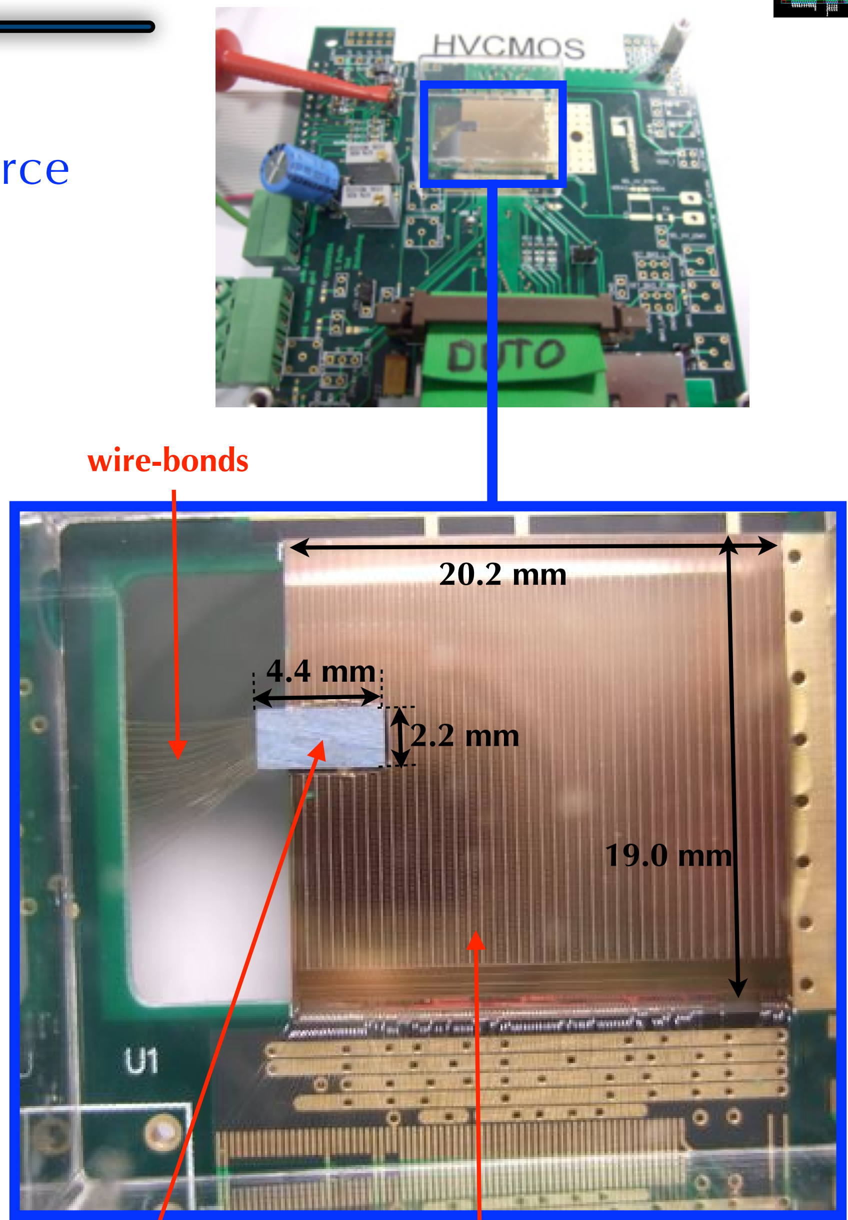
Pixel readout



- FEI4 ASIC glued to HV-CMOS sensor
  - β^+ signal detection from ^{22}Na radiactive source

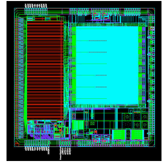






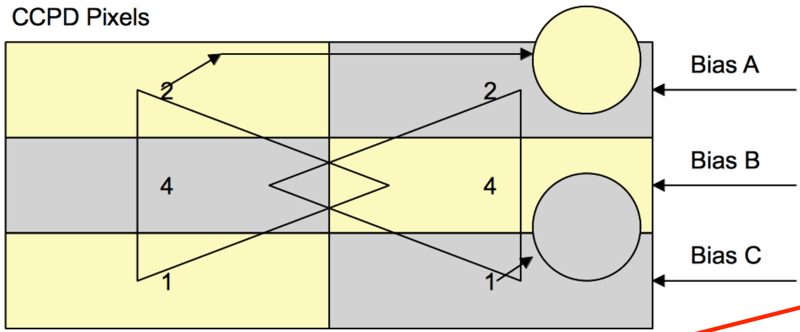
HV2FEI4
- pixel size: 125 μm x 33 μm
- 60 columns x 24 rows

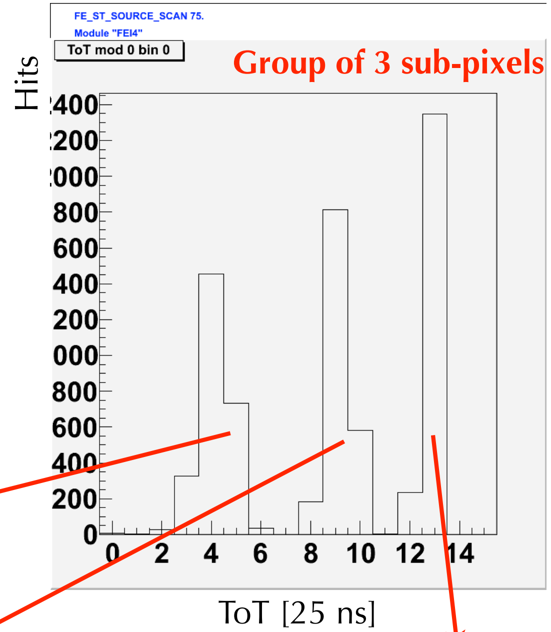
FEI4 readout chip
- pixel size: 250 μm x 50 μm
- 80 columns x 336 rows

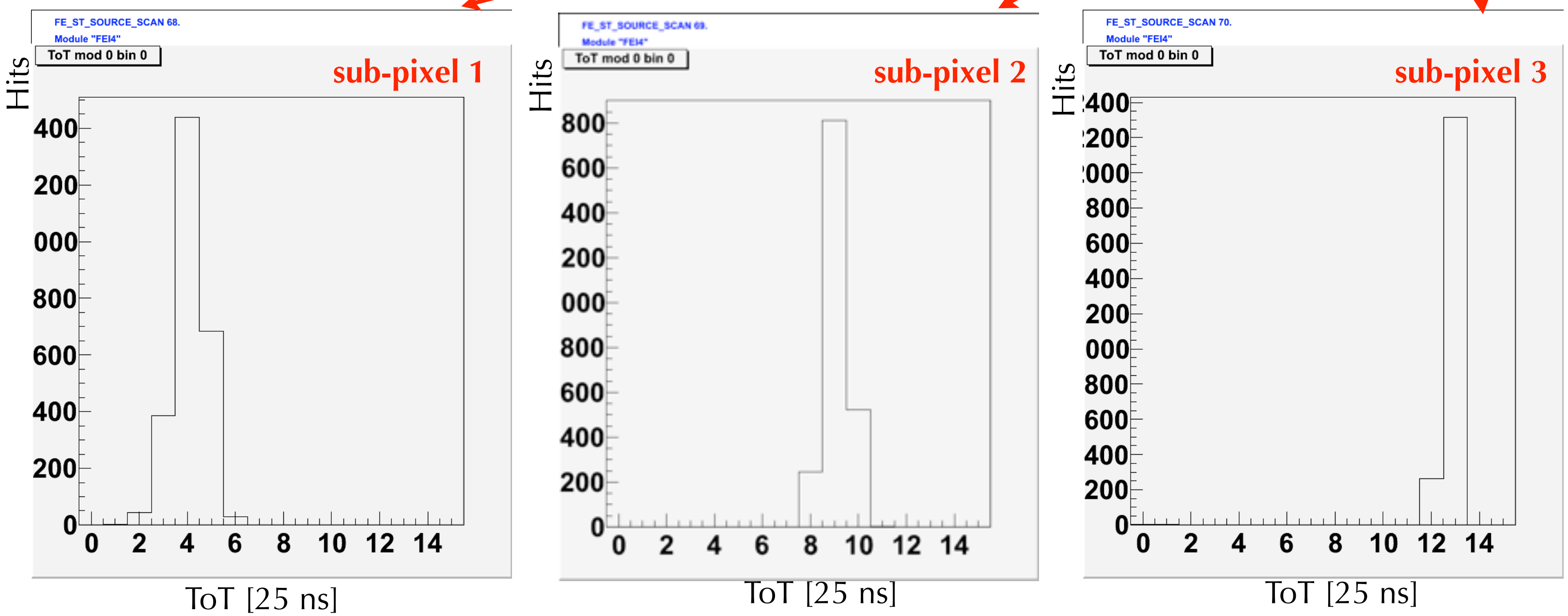


Sub-pixel encoding

- FEI4 readout chip:
  - Time-Over-Threshold (ToT) information (4 bits)
- sub-pixels within group of three could be distinguished

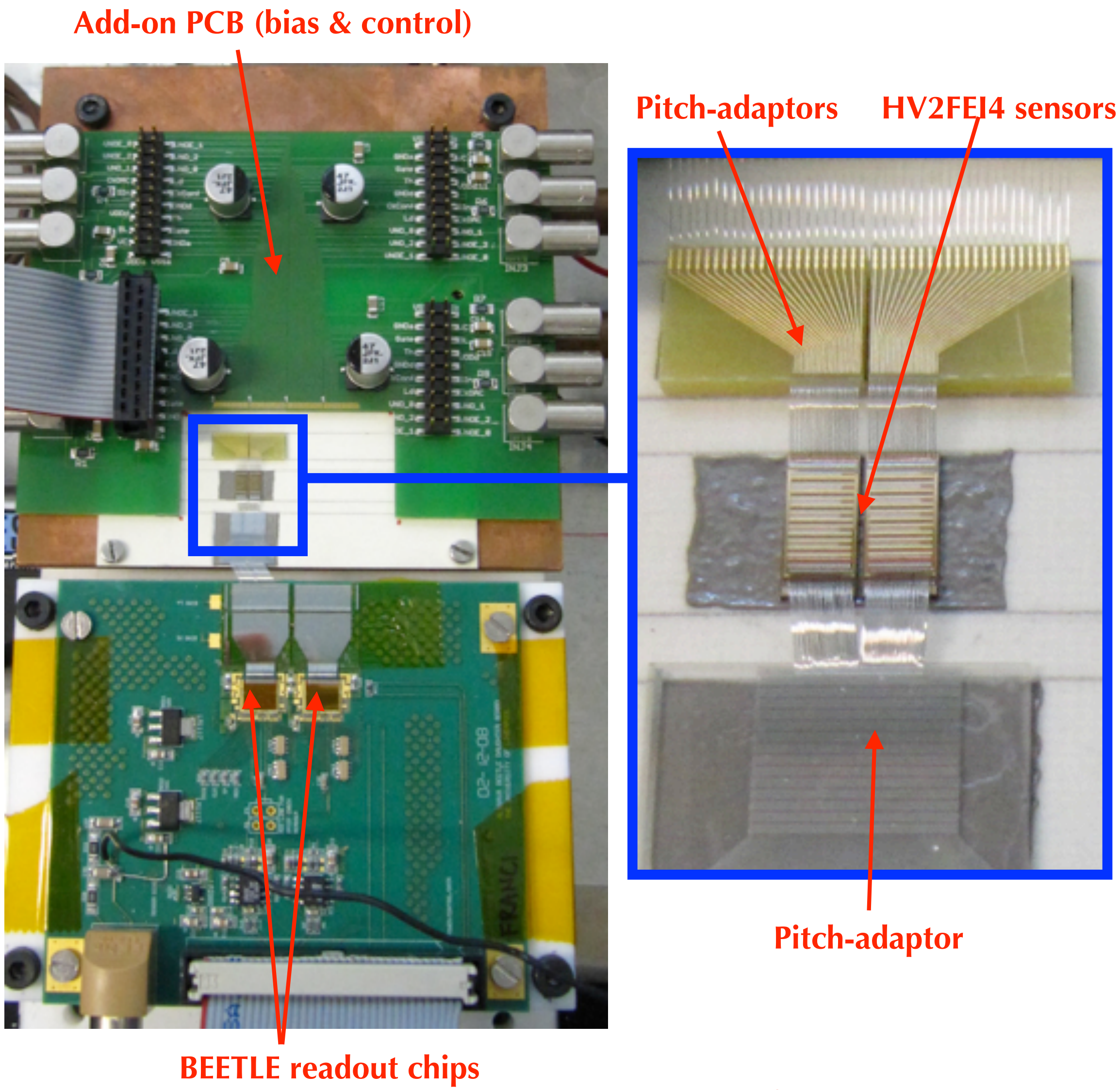


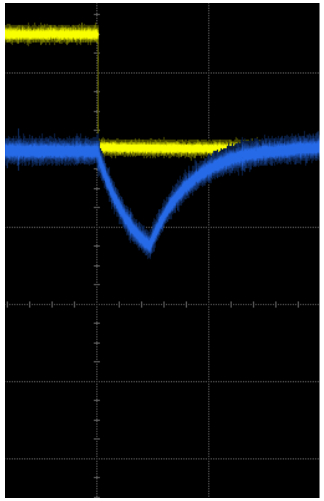


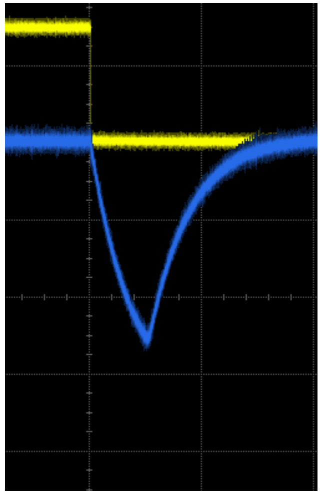


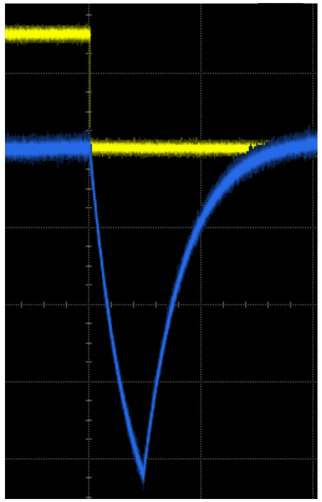
Strip readout

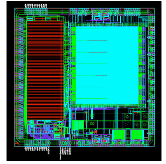
- Analog readout chip: BEETLE (LHCb velo)
- Proof-of-principle of position-encoding along virtual strip



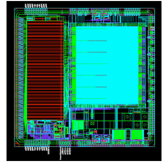

Row 0


Row 12


Row 23

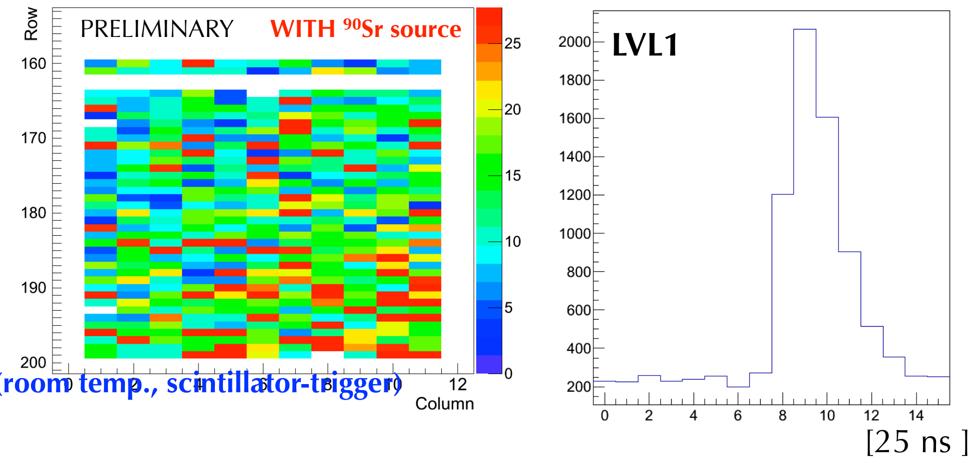


Irradiation results on HV2FEI4_v1 (1/2)



- Neutron irradiation (Ljubljana)
  - 10^{15}, 10^{16} n_{eq}/cm^2
- measurements with ^{90}Sr source
- Running conditions:
  - room temperature
  - bias voltage: ~ -20 V
  - self-trigger & scintillator

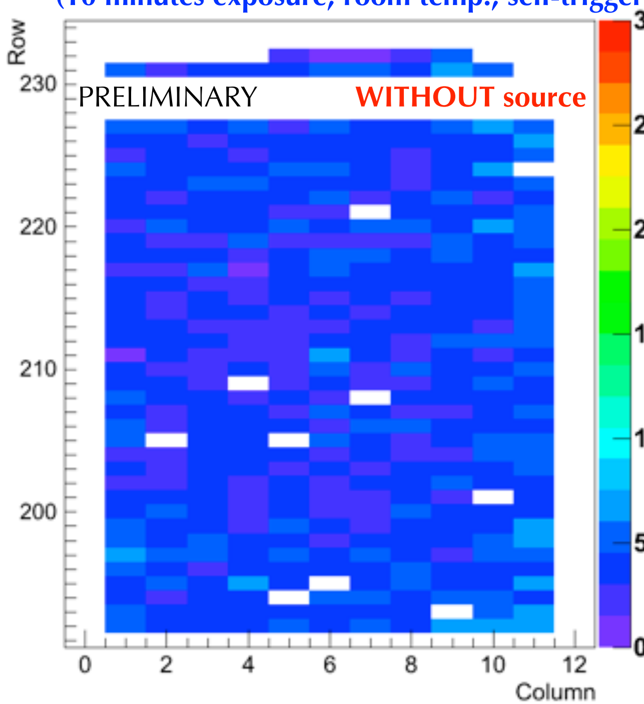
Neutron irradiation: $1x10^{15}$ n_{eq}/cm^2

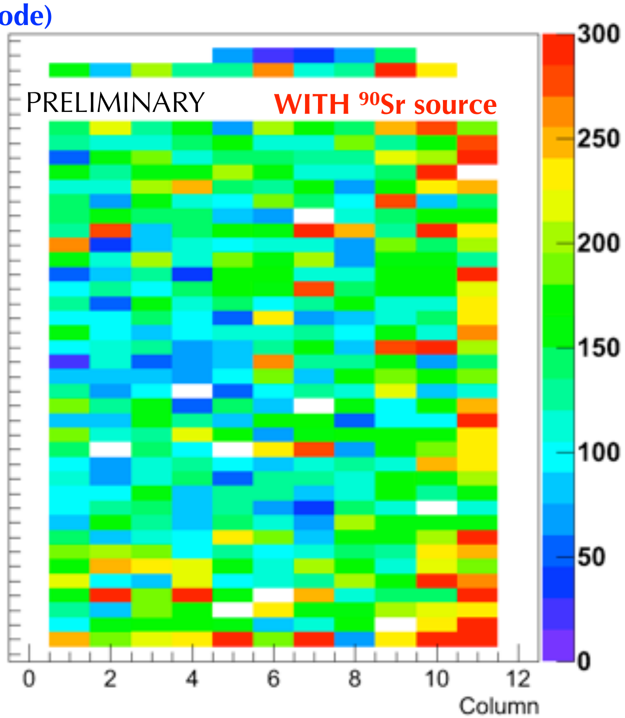


(room temp., scintillator-trigger)

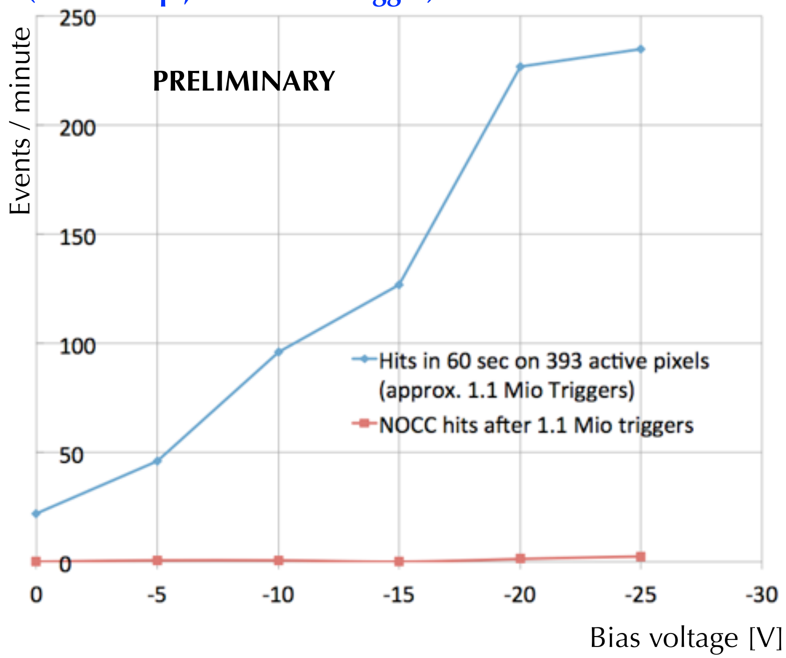
Neutron irradiation: $1x10^{16}$ n_{eq}/cm^2

(10 minutes exposure, room temp., self-trigger mode)

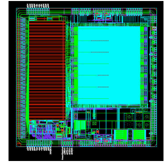




(room temp., scintillator-trigger)

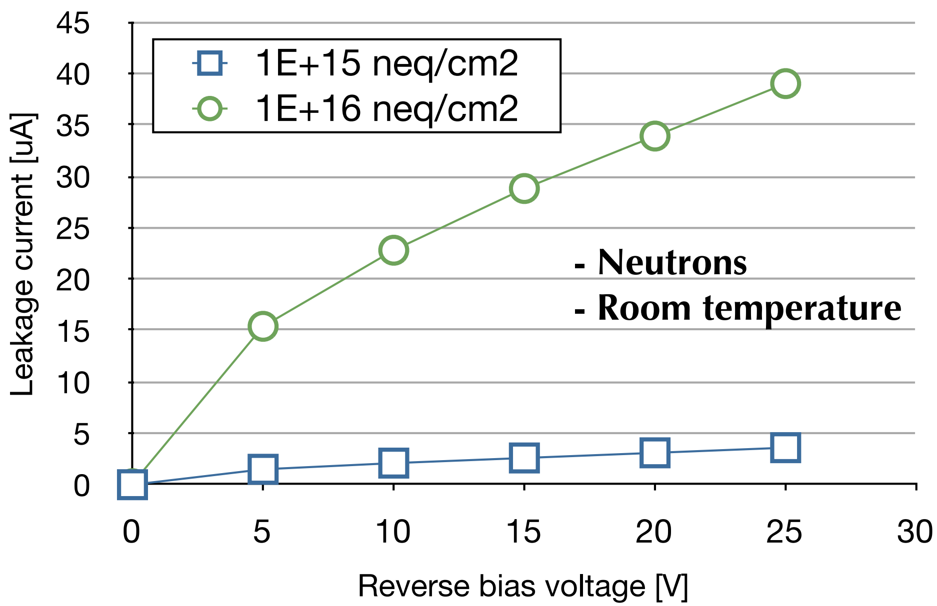


Irradiation results on HV2FEI4_v1 (2/2)

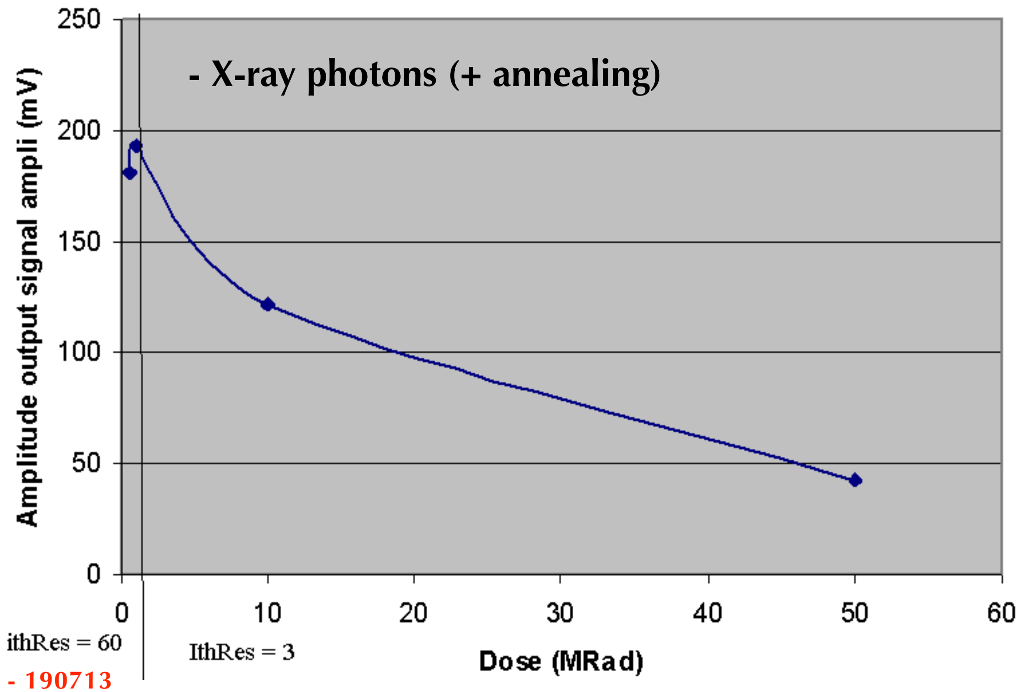


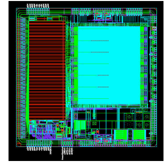
- Additional irradiations:
  - protons (CERN SPS)
  - X-rays (CERN) ➡ up to 50 MRad
- First version of HV2FEI4 not fully rad-hard
  - expected !!
    - usage of standard cells
  - rad-hard wrt bulk damage

IV characteristics



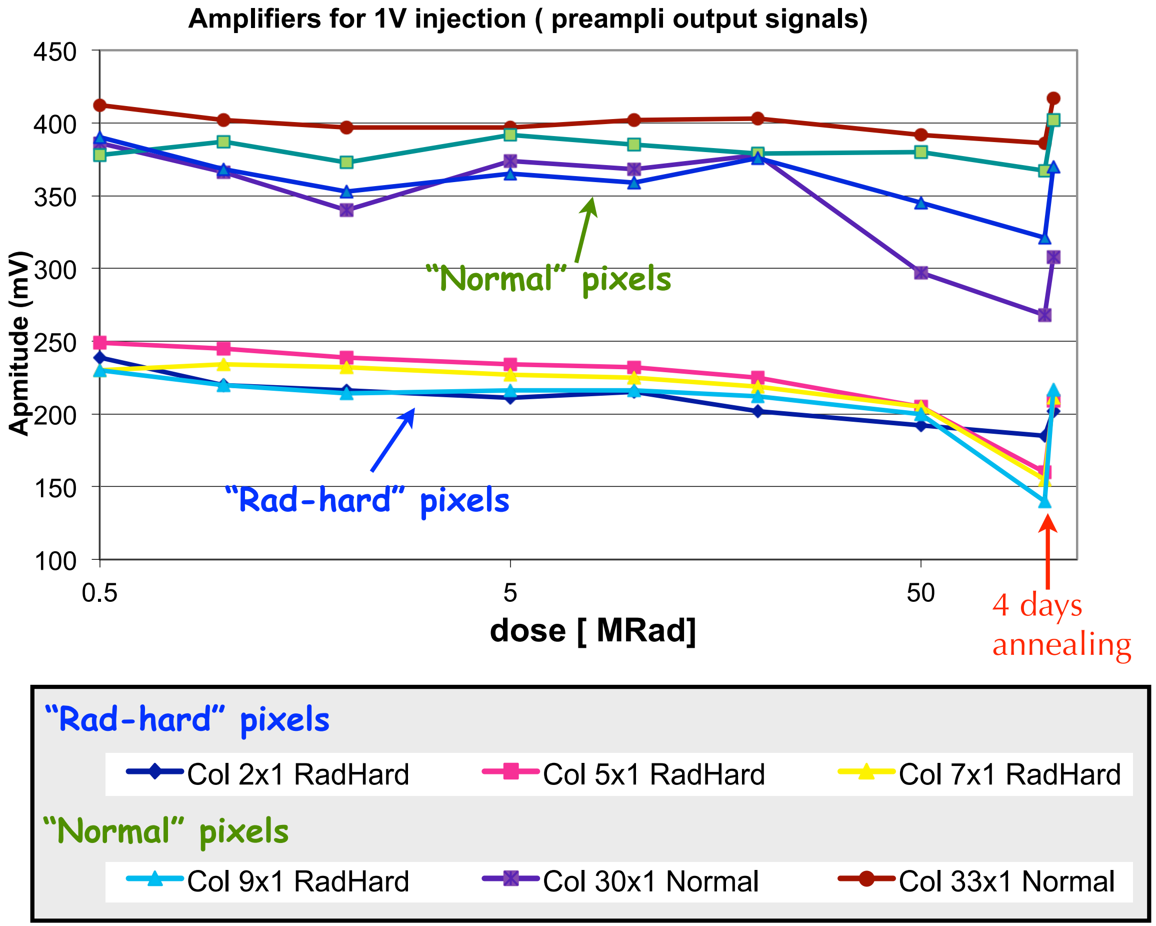
Amplifier output response to test-pulses (1 V)

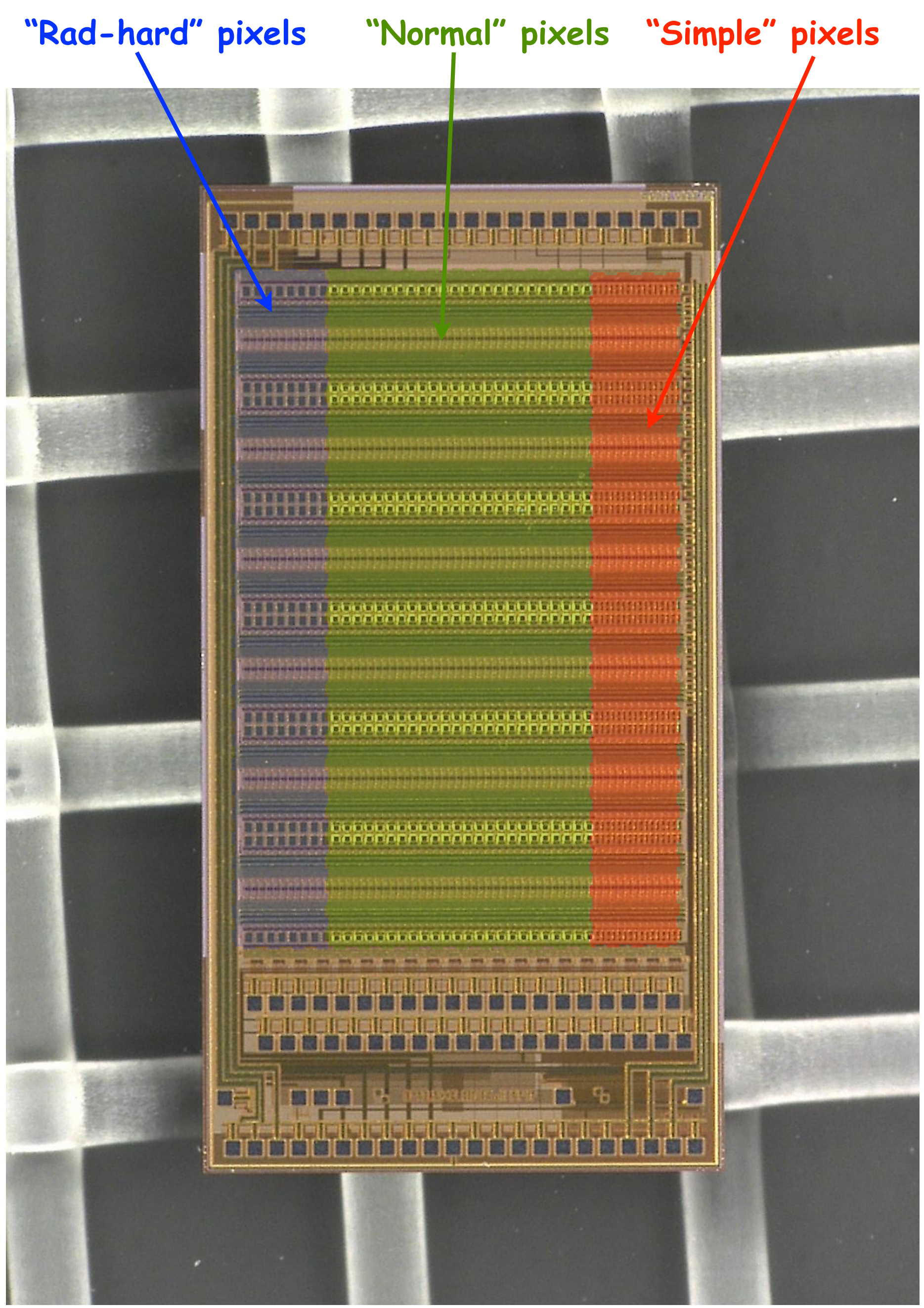




HV2FEI4_v2

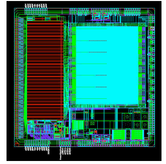
- Second version of the HV2FEI4 chip
  - more radiation tolerant
    - circular devices, guard rings, etc.
- First irradiation results (X-rays)
  - no significant degradation (50 MRad)





HV2FEI4_v2 chip

Summary



- First prototypes of HV2FEI4 chip fully working
  - Compatible with both pixel (AC & DC) readout, strip-readout
  - Very promising results so far:
    - demonstration of sub-pixel encoding (CCPD) and position encoding (virtual strip)
    - first prototype sensor (specifically non-radhard) alive after 10^{16} n_{eq}/cm^2 !!
    - second version (HV2FEI4_v2) with improved radiation hardness

- HV-CMOS appears as a very promising technology for future particle tracking detectors in the HL-LHC
  - low-cost commercial technology, high-availability
    - no bump-bonding needed !!
  - low-mass (thin) sensors, low-power, high SNR (even at room temperature)
  - rad-hard, improved spatial resolution

- Next steps:
  - more radiation-hardness studies
  - prototypes for ATLAS pixel and strip detector modules