Radiation-hard Active Pixel Detectors based on HV-CMOS Technology for HL-LHC Detector Upgrades

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on behalf of the participating institutes:
The High-Luminosity LHC (HL-LHC)

LHC startup \( \sqrt{s} = 900 \text{ GeV} \)

\( \sqrt{s} = 7 \sim 8 \text{ TeV} \)
\( \mathcal{L} = 6 \times 10^{33} \text{ cm}^{-2}\text{s}^{-1} \)
Bunch spacing 50 ns

Go to design energy, nominal luminosity (Phase-0)

\( \sqrt{s} = 13 \sim 14 \text{ TeV} \)
\( \mathcal{L} \sim 1 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1} \)
Bunch spacing 25 ns

Injector and LHC Phase-1 upgrade to full design luminosity

\( \sqrt{s} = 14 \text{ TeV} \)
\( \mathcal{L} \sim 2 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1} \)
Bunch spacing 25 ns

HL-LHC Phase-2 upgrade, SC crab cavities

\( \sqrt{s} = 14 \text{ TeV} \)
\( \mathcal{L} = 5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1} \)
Luminosity leveling

HE-LHC: \( \sqrt{s} = 33 \text{ TeV} \)
300 - 3000 fb\(^{-1}\)
New ATLAS tracker

- Conditions at $5 \times 10^{34}$ cm$^{-2}$s$^{-1}$:
  - radiation damage
  - channel occupancy
    - particle multiplicity $> 10^5$ particles $|\eta| < 3.2$

- New ATLAS Inner Detector
  - silicon-based tracker (pixels + strips)
    - maintain / improve current tracking capabilities
    - better detector granularity, radiation hardness

- New Detectors: lowest price while rad-hard!
  - possibility of existing industrialized processes?
High-Voltage CMOS

- High Voltage-CMOS (HV-CMOS) technology
  - standard industrialized process (low-cost, large availability)

- HV-CMOS as monolithic pixel particle detector
  - project initiated by I. Peric (U. Heidelberg)
  - sensor based on multiple-well structure
    - entire CMOS electronics inside the deep N-well ➔ “smart diode” ➔ “smart diode array”
      - PMOS transistors directly in the deep N-well
      - NMOS transistors within P-well embedded in deep N-well

### Technology Specifications

<table>
<thead>
<tr>
<th></th>
<th>Austria Microsystems (AMS) + IBM 350 nm / 180 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate resistance</td>
<td>&gt; 10 Ωcm</td>
</tr>
<tr>
<td>Pixel size</td>
<td>down to 20 µm</td>
</tr>
<tr>
<td>Depletion depth</td>
<td>~ 10 - 20 µm</td>
</tr>
<tr>
<td>Reverse bias voltage</td>
<td>~ 60 - 100 V</td>
</tr>
<tr>
<td>Charge collection</td>
<td>~ 40 ps</td>
</tr>
<tr>
<td>Signal (mip)</td>
<td>~ 2000 e</td>
</tr>
</tbody>
</table>
Capacitively coupled detector

- Implementation of on-sensor CMOS electronics (e.g. charge sensitive amplifier, etc.) → signal transmission by **capacitive (AC) coupling**
  - signal transmitted to the charge sensitive amplifier in the readout ASIC
  - no need of costly bump-bonding process

- Gluing process:
  - alignment precision: < 5 μm
  - glue layer thickness: < 5 μm

SNR: ~ 45 - 60
HV2FEI4 prototype chip

- Chip-size: 2.2x4.4 mm²
  - pixel matrix: 60x24 sub-pixels (unit cell = 6 pixels, each 125 x 33 µm²)

- HV2FEI4 compatible with:
  - ATLAS FEI4 (ATLAS pixel readout ASIC)
    - bump-bonding or capacitive coupling
  - strip readout

- Charge sensitive amplifier, discriminator
- On-chip bias DAC, configuration via FPGA

Unit cell structure of the HV2FEI4 prototype

[Diagram of unit cell structure]

HV2FEI4 (v1) chip

[Diagram of chip dimensions: 4.4 mm height, 2.2 mm width]
Readout modes

- **Capacitively coupled readout chip**
  - unit cell corresponding to two ATLAS FEI4 readout-chip pixels
  - combine sensor sub-pixels for AC readout
  - different current amplitude per pixel ➔ hit position from pulse-height information
    - improvement in resolution without changes in readout chip

- **Readout as a strip-like detector**
  - sum all pixels in a row ➔ “virtual strip”
    - multiple connections possible (crossed-strips)
  - hit position along strip encoded as pulse-height ➔ Z-resolution improved

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**Pixel readout (AC coupling)**

- FEI4 Pixels
- Signal transmitted capacitively
- CCPD Pixels
- Bias A
- Bias B
- Bias C

**Strip readout**

- Summing line
- Wire-bonds
- Pixels
- CMOS sensor
- Comparator or ADC

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HV2FEI4: CCPD readout

EPS Conference - 190713
Pixel readout

- FEI4 ASIC glued to HV-CMOS sensor
  - $\beta^+$ signal detection from $^{22}$Na radiactive source

- FEI4 readout chip
  - pixel size: 250 $\mu$m x 50 $\mu$m
  - 80 columns x 336 rows

- HV2FEI4
  - pixel size: 125 $\mu$m x 33 $\mu$m
  - 60 columns x 24 rows

wire-bonds
Sub-pixel encoding

- FEI4 readout chip:
  - Time-Over-Threshold (ToT) information (4 bits)
- Sub-pixels within group of three could be distinguished
Strip readout

- Analog readout chip: BEETLE (LHCb velo)
- Proof-of-principle of position-encoding along virtual strip
Irradiation results on HV2FEI4_v1 (1/2)

- Neutron irradiation (Ljubljana)
  - $10^{15}, 10^{16}$ $n_{eq}/cm^2$
- measurements with $^{90}$Sr source
- Running conditions:
  - room temperature
  - bias voltage: ~ -20 V
  - self-trigger & scintillator

![Neutron irradiation: $1x10^{16}$ $n_{eq}/cm^2$](image1)

![Neutron irradiation: $1x10^{15}$ $n_{eq}/cm^2$](image2)

 Erements / minute (room temp., scintillator-trigger)

![Neutron irradiation: $1x10^{16}$ $n_{eq}/cm^2$](image3)

 Erements / minute (room temp., scintillator-trigger)

![Neutron irradiation: $1x10^{15}$ $n_{eq}/cm^2$](image4)

 Erements / minute (room temp., scintillator-trigger)
Irradiation results on HV2FEI4_v1 (2/2)

- Additional irradiations:
  - protons (CERN SPS)
  - X-rays (CERN) ➔ up to 50 MRad

- First version of HV2FEI4 not fully rad-hard
  - expected !!
    - usage of standard cells
  - rad-hard wrt bulk damage

**IV characteristics**

- Leakage current [µA]
  - Neutrons
  - Room temperature

**Amplifier output response to test-pulses (1 V)**

- X-ray photons (+ annealing)
HV2FEI4_v2

- Second version of the HV2FEI4 chip
  - more radiation tolerant
    - circular devices, guard rings, etc.
- First irradiation results (X-rays)
  - no significant degradation (50 MRad)

Amplifiers for 1V injection (preamp output signals)

<table>
<thead>
<tr>
<th>Amplitude (mV)</th>
<th>Dose (MRad)</th>
</tr>
</thead>
<tbody>
<tr>
<td>450</td>
<td>0.5</td>
</tr>
<tr>
<td>400</td>
<td>5</td>
</tr>
<tr>
<td>350</td>
<td>25</td>
</tr>
<tr>
<td>300</td>
<td>50</td>
</tr>
<tr>
<td>250</td>
<td>4 days annealing</td>
</tr>
</tbody>
</table>

“Rad-hard” pixels
- Col 2x1 RadHard
- Col 5x1 RadHard
- Col 7x1 RadHard

“Normal” pixels
- Col 9x1 RadHard
- Col 30x1 Normal
- Col 33x1 Normal
Summary

- First prototypes of HV2FEI4 chip fully working
  - Compatible with both pixel (AC & DC) readout, strip-readout
  - Very promising results so far:
    - demonstration of sub-pixel encoding (CCPD) and position encoding (virtual strip)
    - first prototype sensor (specifically non-radhard) alive after $10^{16} \text{ n}_{eq}/\text{cm}^2$ !!
    - second version (HV2FEI4_v2) with improved radiation hardness

- HV-CMOS appears as a very promising technology for future particle tracking detectors in the HL-LHC
  - low-cost commercial technology, high-availability
    - no bump-bonding needed !!
  - low-mass (thin) sensors, low-power, high SNR (even at room temperature)
  - rad-hard, improved spatial resolution

- Next steps:
  - more radiation-hardness studies
  - prototypes for ATLAS pixel and strip detector modules