HEP 2013
Stockholm
18-24 July 2013

Contribution ID: **295** Type: **Talk presentation**

Radiation-hard Active Pixel Detectors based on HV-CMOS Technology for HL-LHC Detector Upgrades

Friday 19 July 2013 11:15 (15 minutes)

State-of-the-art particle physics detectors at colliders contain a pixel detector as heart of their particle tracker to cope with the large density of particle tracks near the interaction point. For radiation damage reasons, mostly hybrid detectors were used which comprise a silicon pixel sensor fabricated on high-resistivity FZ silicon and a bump-bonded readout chip in deep sub-micron technology. The requirement for bump-bonding and mechanical demands constrained the pixel pitch/size to larger than ˜50-100µm and also led to elevated costs which prevented the instrumentation of larger areas with pixel detectors. This is an issue in particular for HL-LHC upgrades of the existing trackers where the areas instrumented with pixel detectors will be significantly larger due to the higher occupancy at elevated luminosities.

Deep-submicron HV CMOS processes feature moderate bulk resistivity and HV capability and are therefore good candidates for drift-based radiation-hard monolithic active pixel sensors (MAPS). It is possible to apply up to 100V of bias voltage leading to a depletion depth of ˜10-20 um. Thanks to the high electric field, charge collection is fast and nearly insensitive to radiation-induced trapping. Due to the still rather high dopant concentration, almost no radiation effect is expected to the depletion voltage.

We explore the concept of using such a HV CMOS process to produce a drop-in replacement for traditional radiation hard silicon sensors. Such active sensors contain only simple circuits to amplify and either discriminate or condition the basic pulses created by charged particles. A traditional readout chip is still needed to receive and organize the data from the active sensor and handle high level functionality such as trigger management. The devices are tested with the ATLAS FE-I4 pixel readout chip and the the ATLAS ABCN and the LHCb Beetle strip readout chips. Either strip-like or pixel-like readout can be selected on the same device.

While a readout chip is still needed (unlike the case of an ideal MAPS device that contains all sensing and processing functionality in one), the active sensor approach offers many advantages: such sensors can be fabricated in a fully commercial CMOS process without need for special substrates or processing and will therefore cost less than traditional diode sensors, they can be thinned to the limit of the collection layer resulting in much lower mass, they require relatively low bias voltage, and they can operate at room temperature or with only moderate cooling after irradiation. In addition, they can contain sub-pixels with smaller pitch than the readout chip and improve the spatial resolution compared to standard sensors by encoding the hit sub-pixels in the signal sent to the readout chip. From a practical perspective, maintaining the traditional separation between sensing and processing functions lowers development cost and makes use of existing infrastructure. Active sensors can also be seen as a first step towards 3D-integrated electronics in which the analogue tier contains the sensor.

To explore the performance and radiation hardness of active sensors, the HV2FEI4 ASIC was produced in the AMS H18 process. It is compatible with the pixel and strip readout chips mentioned above and features a matrix of 60 by 24 pixels with a pixel cell size of 33 by 125 um. Thanks to relying on active circuits, capacitive coupling to the pixel readout chip is feasible and is explored with HV2FEI4 chips glued to FE-I4s. The option to replace the expensive and time-consuming bump-bonding by gluing would significantly lower the cost of future large-scale Pixel Detector upgrades and enable the instrumentation of larger areas with pixel detectors. For comparison, bump-bonding the HV2FEI4 with gold stud-bumps is still possible.

The HV2FEI4 pixels are combined to match the readout multiplicity of the respective chips: for the pixel readout, three HV-CMOS pixels are multiplexed onto one FE-I4 pixel such that the hit pixels are encoded by the pulse height. In this way, the position resolution of the HV-CMOS sensor can be significantly better than the granularity of the readout chip suggests. For the strip readout, the pixel cells are combined to form virtual

strips. Here, the z-position of the hit is encoded via the discriminator's pulse height and can be evaluated by analogue strip readout electronics like the Beetle chip.

The presentation will give an overview of the characterization results of the HV2FEI4 chip and highlight first experience with both pixel and strip readout. In addition, the status of the irradiation programme will be summarized and future prospects will be discussed.

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Session Classification: Detector R&D and data handling

Track Classification: Detector R&D and data handling