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DEPFET
Active Pixel Detector

Federal Ministry
of Education
and Research

DEPFET
Active pixel sensors for future e^+e^- experiments

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University of Bonn

On behalf of the DEPFET Collaboration

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Outline

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- DEPFET for future colliders
  - SuperKEKB and ILC
- DEPFET system
  - Sensor development
  - ASICs
- Latest results
  - Lab and beam tests

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Future vertex detectors

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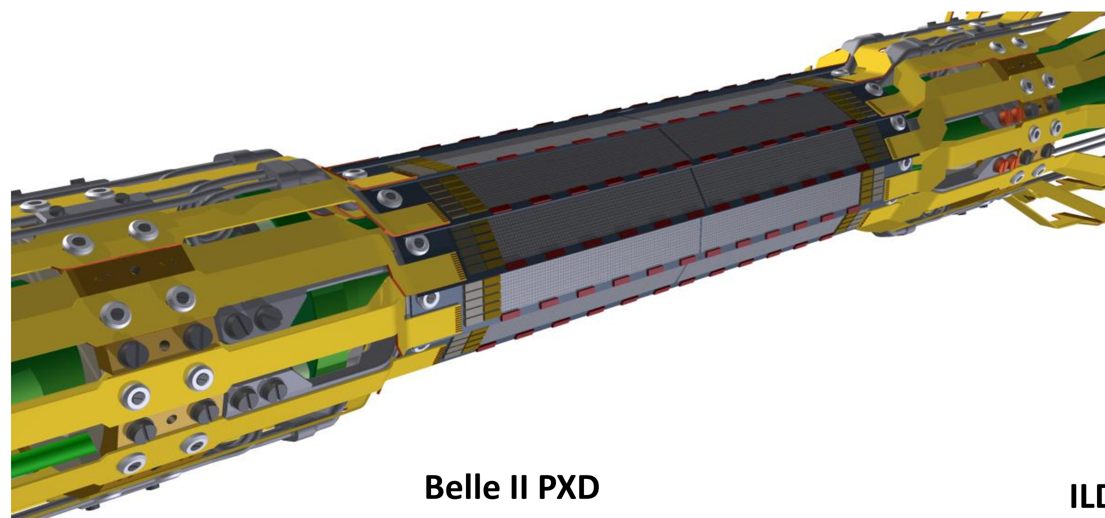
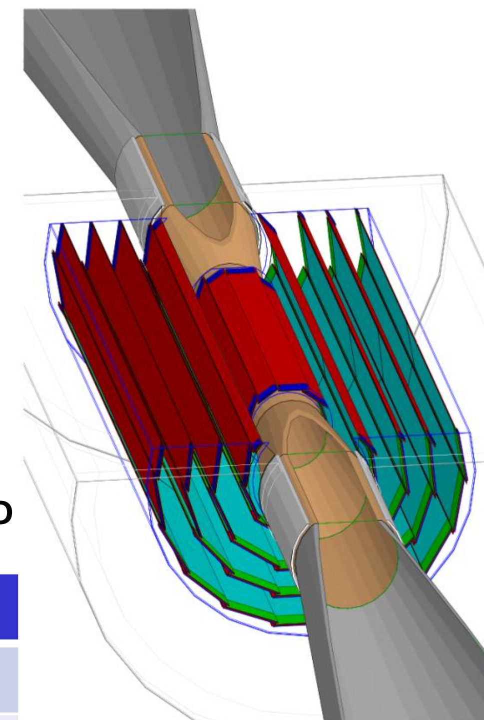
The Belle II Collaboration decided on DEPFET as baseline for the pixel detector



Belle II PXD



ILD 5-layer VXD

	Belle II	ILD LOI 5-layer layout	
Radii	14, 22	15, 26, 38, 49, 60	mm
Ladder length	90 (L1), 122 (L2)	123 (L1), 250 (L2-L5)	mm
Sensitive width	12.5 (L1-L2)	13 (L1), 22 (L2-L5)	mm
Number of ladders	8, 12	8, 8, 12, 16, 20	
Pixel size	50x50 (L1), 50x75 (L2)	25x25 (L1-L5)	μm^2
Frame rate	50	20 (L1), 4 (L2-L5)	kHz

The Belle II PXD DEPFET ladders: *almost* prototypes for L1 and L2 of ILD

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ILC detector concepts and Belle II

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- Both detectors have very similar requirements

	Belle II	ILC
Occupancy	0.4 hits/μm^2/s	0.13 hits/μm^2/s
Radiation	2 Mrad/year	< 100 krad/year
	$2 \cdot 10^{12}$ 1 MeV n_{eq} per year	10^{11} 1 MeV n_{eq} per year
Duty cycle	1	1/200
Frame time	20 μs	25-100 μs
Momentum range	Low momentum (< 1 GeV)	All momenta
Acceptance	17°-155°	6°-174°
Material budget	0.21% X_0 per layer	0.12% X_0 per layer
Resolution	10 μm (50x75 μm^2)	3 μm (20x20 μm^2)

→ Belle II presents more severe challenges than ILC in many different aspects

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DEPFET – DEpleted Field Effect Transistor

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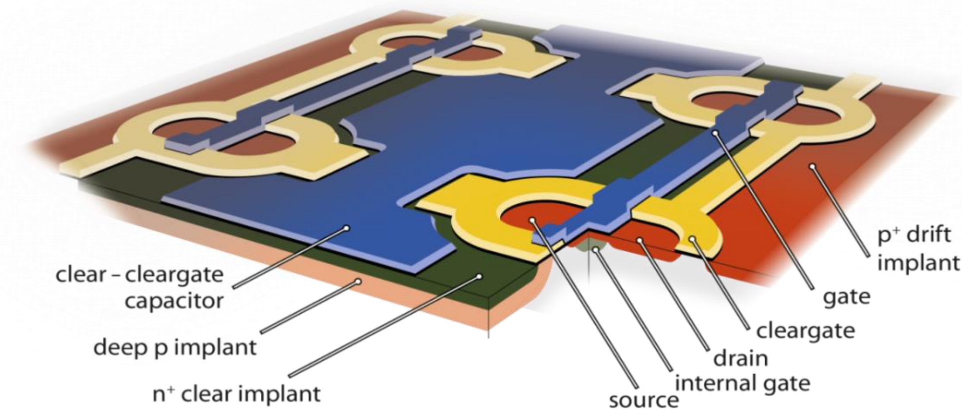
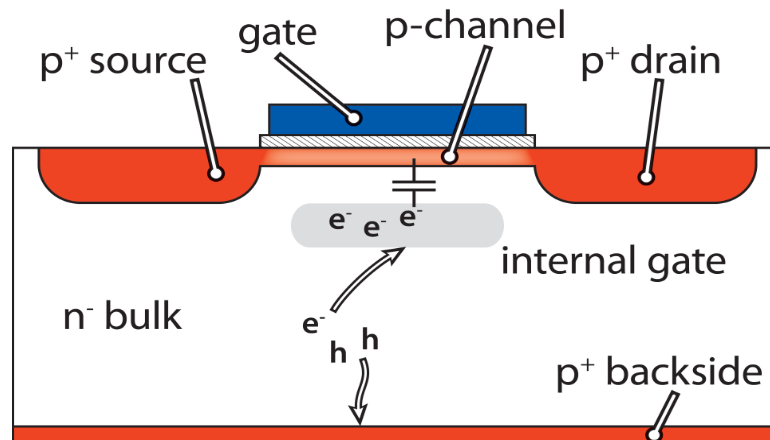
- Concept: amplifying transistors in a fully depleted bulk
- Internal gate forms potential minimum for e^-
- Stored charge modulates the channel current
- Small intrinsic noise
- Sensitive off-state, no power consumption
- Internal amplification g_q~0.3 – 1.0 nA/e^-





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DEPFET pixel array

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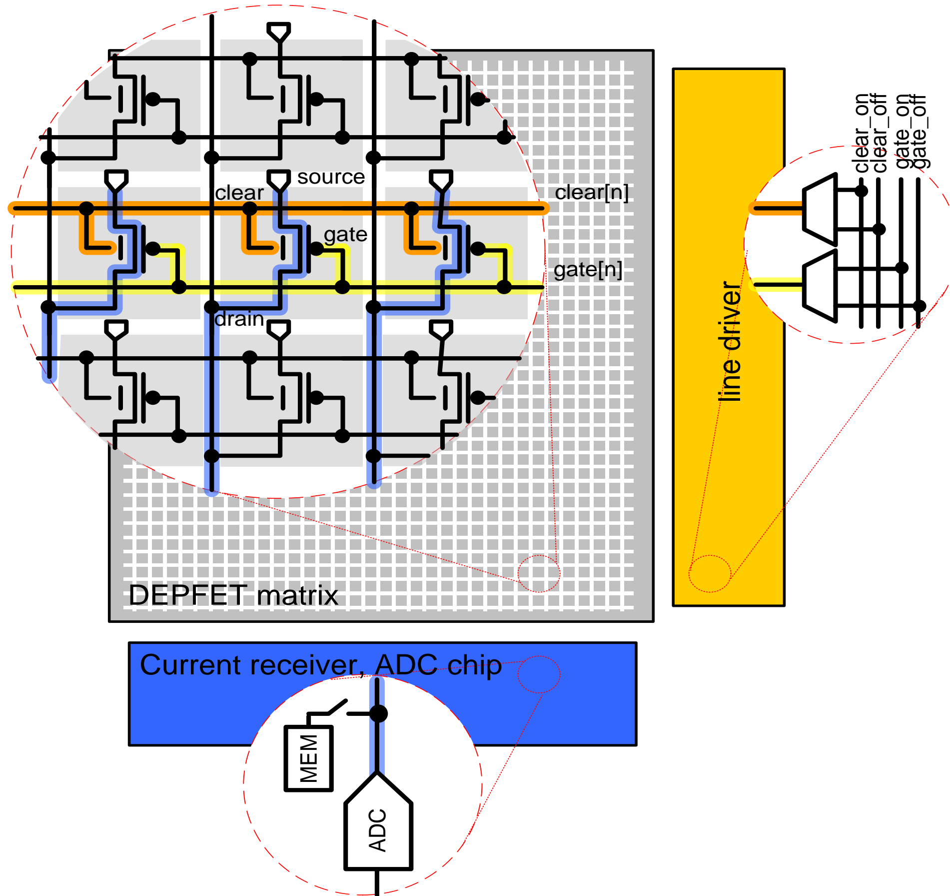
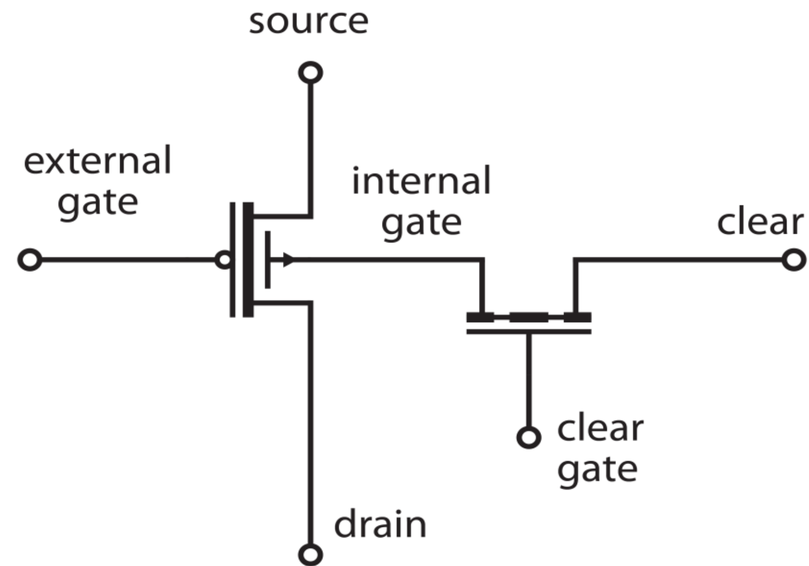


- Pixels are arranged in a matrix
- Row wise readout
- Gate, clear lines need Switcher steering chip
- Long drain readout lines to keep material out of the acceptance region



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The DEPFET ladder

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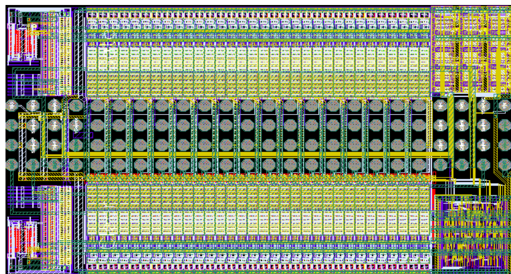
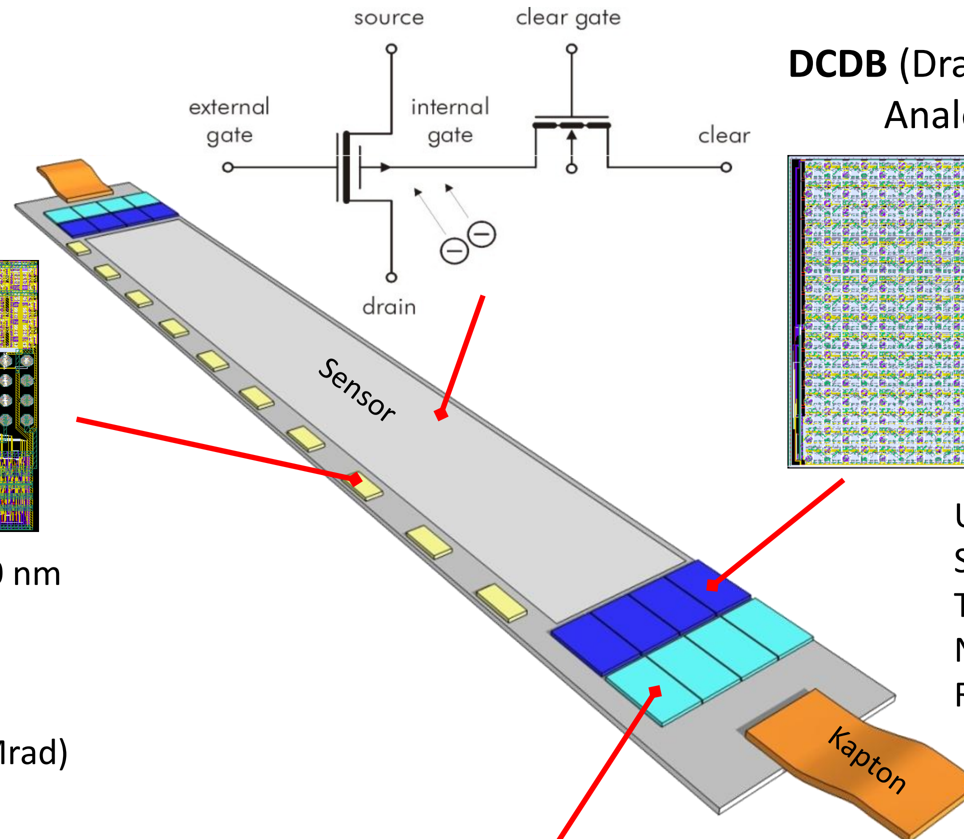
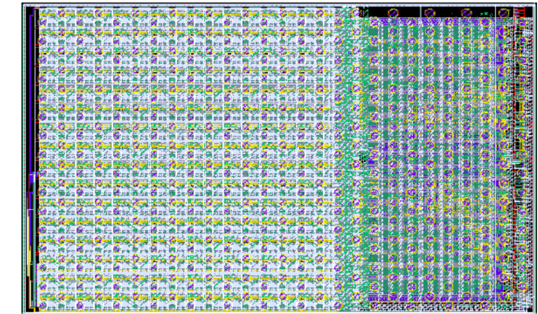
SwitcherB
Row control



AMS/IBM HVCMOS 180 nm
Size 3.6 × 1.5 mm²
Gate and Clear signal
Fast HV ramp for Clear
Rad. Hard proved (36 Mrad)

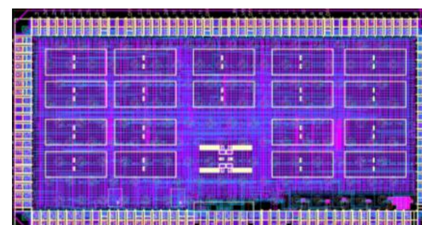


DCDB (Drain Current Digitizer)
Analog frontend



UMC 180 nm
Size 5.0 × 3.2 mm²
TIA and ADC
Noise 35 nA @ 100 ns/row
Rad. Hard proved (20 Mrad)

DHP (Data Handling Processor)
First data compression



IBM CMOS 90 nm (TSMC 65 nm)
Size 4.0 × 3.2 mm²
Stores raw data and pedestals
Common mode and pedestal correction
Data reduction (zero suppression)
Timing signal generation
Rad. Hard proved (100 Mrad)

The DEPFET ladder

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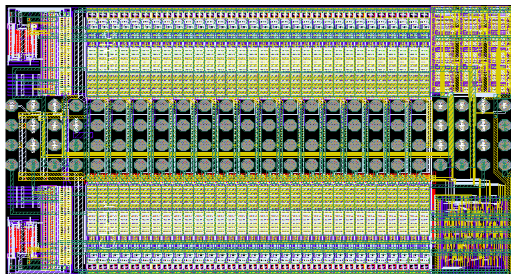
The full-size close to final versions of the ASICs are designed, produced and found to work

SwitcherB
Row control



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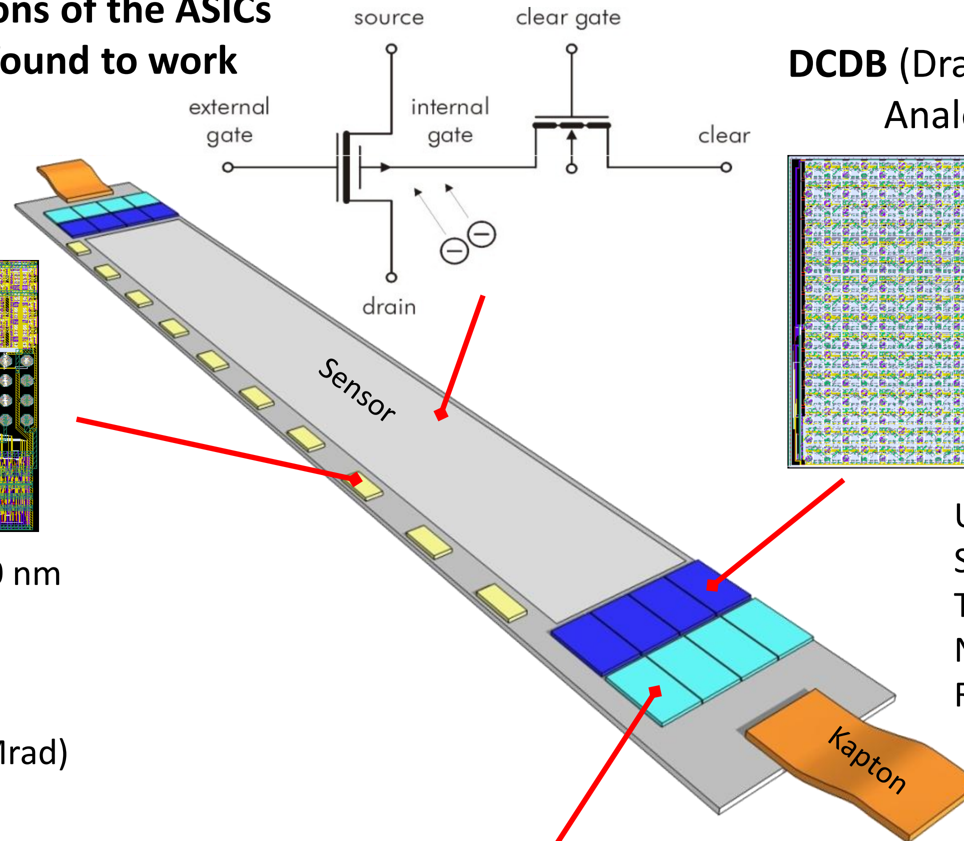

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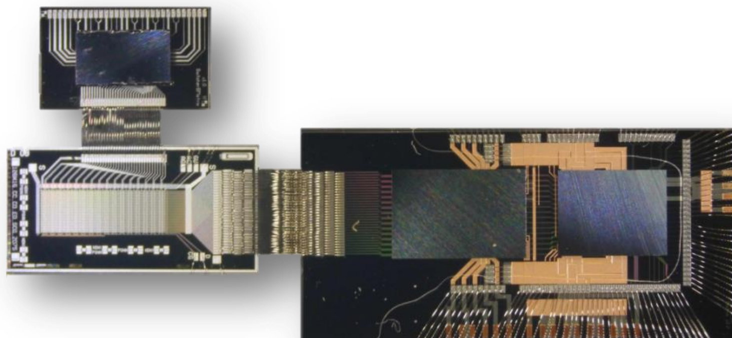

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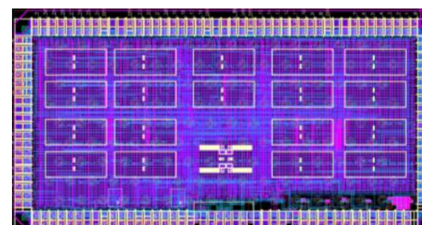

IBM CMOS 90 nm (TSMC 65 nm)
Size 4.0 × 3.2 mm²
Stores raw data and pedestals
Common mode and pedestal correction
Data reduction (zero suppression)
Timing signal generation
Rad. Hard proved (100 Mrad)

Thin DEPFET sensors

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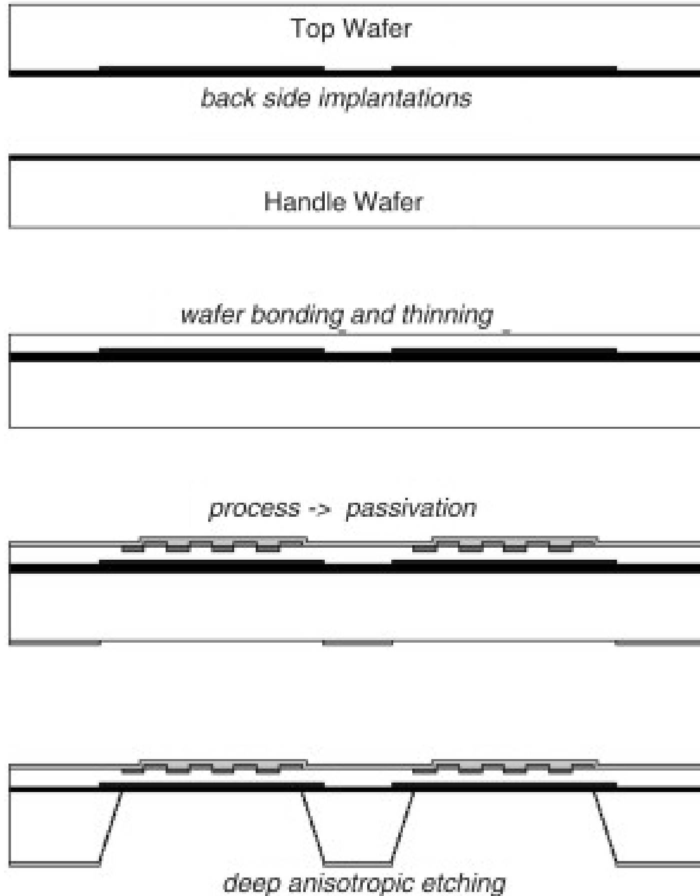
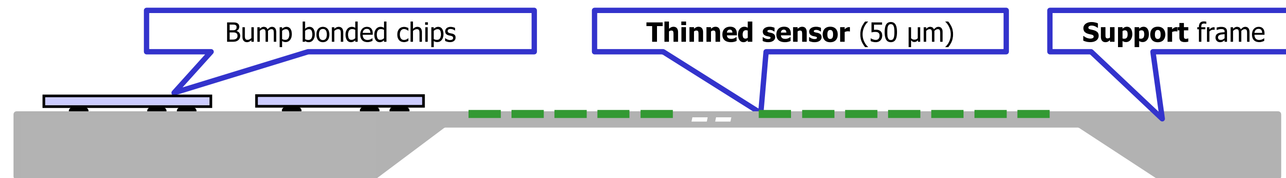
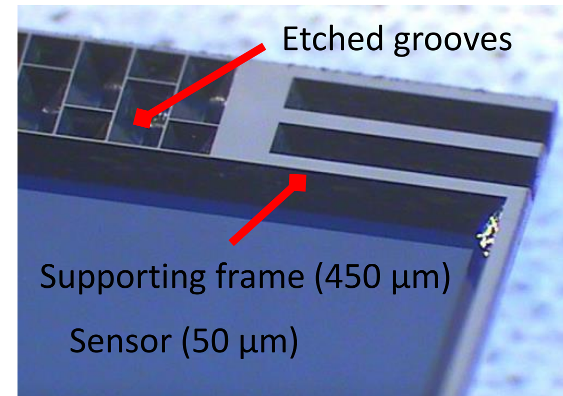
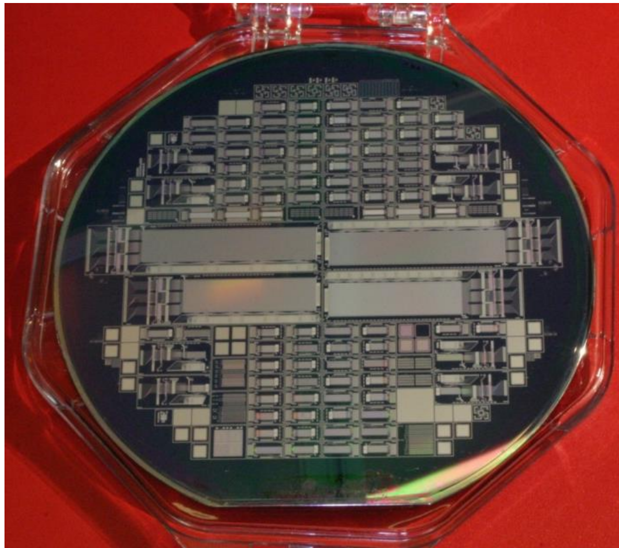
Use anisotropic etching on bonded wafers to create a thin, self-supporting sensor
→ One material: uniform and small thermal expansion





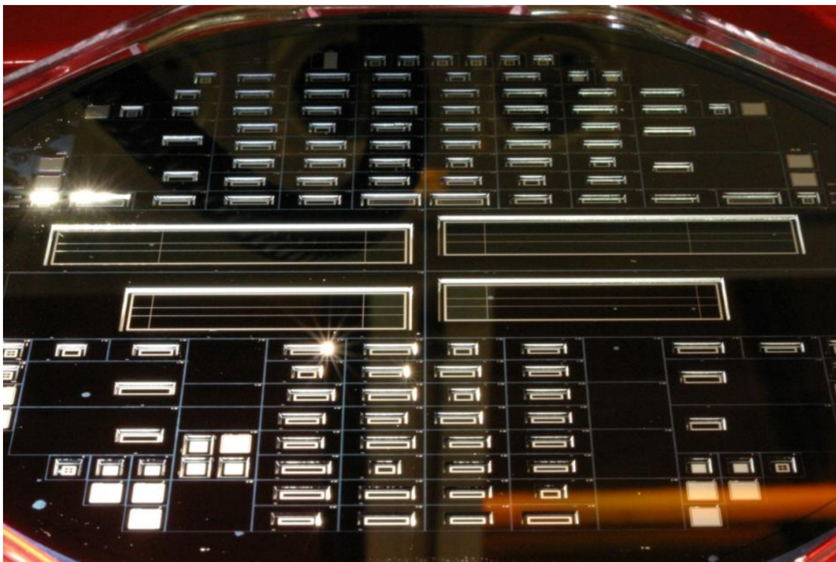


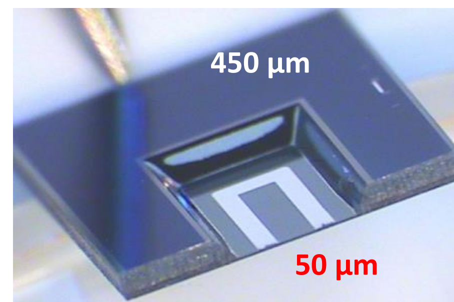
PXD6 DEPFET latest prototype production



8 SOI wafers with 50 µm thin sensors (400 µm handle)

- Small test matrices to test different pixel sizes (50-200 µm)
- Design variations: short gate lengths, clear structures, drift
- Full size sensors –half ladders for prototyping
- Technology variations on the wafer level





90 steps fabrication process:

9 Implantations
19 Lithographies
2 Poly-layers
2 Alu-layers
1 Copper layer
Back side processing

First 50 µm thin DEPFET sensors produced!

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Hybrid 5.0 – Concept demonstrator

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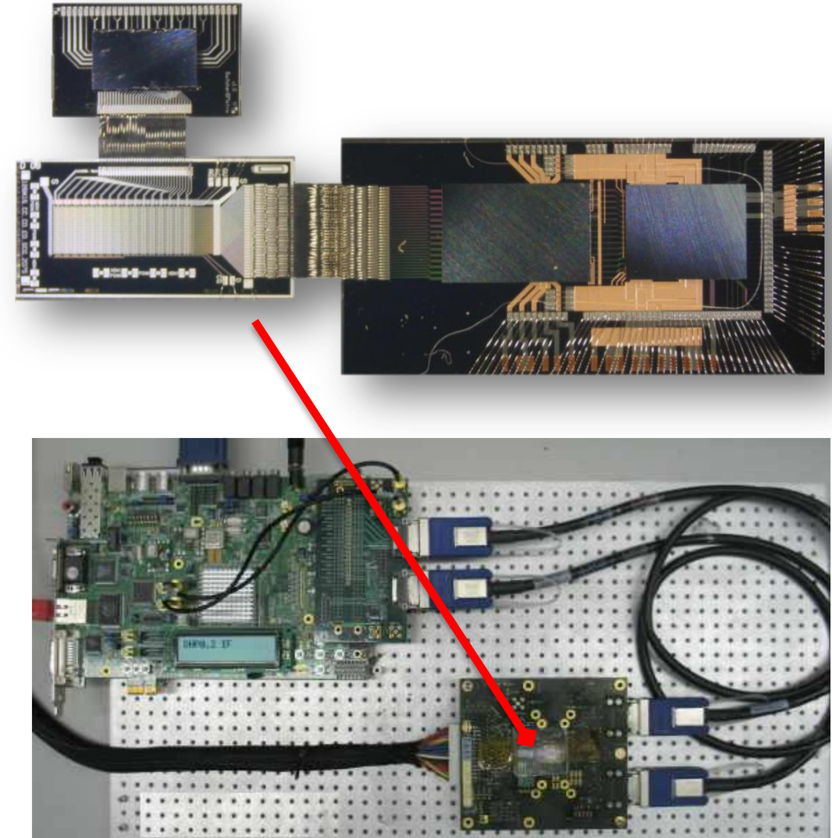
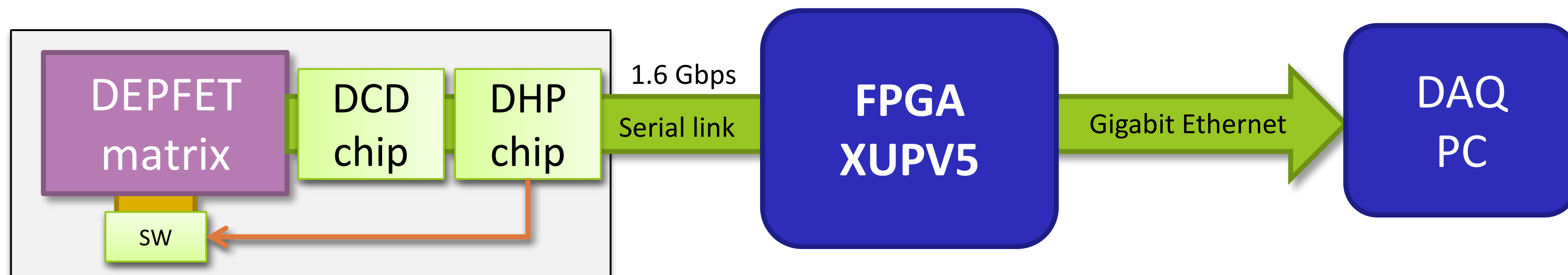
- Zero suppressed readout with the minimum necessary amount of components:
  - One Switcher-B
  - One DCDBv2
  - One DHP 0.2
  - Small thin matrix: Belle II SD PXD6 type, 16x128 pixels, 50x75 µm^2 pitch
- Frame rate: 300 kHz (small matrix)





Laboratory tests: DEPFET sensor

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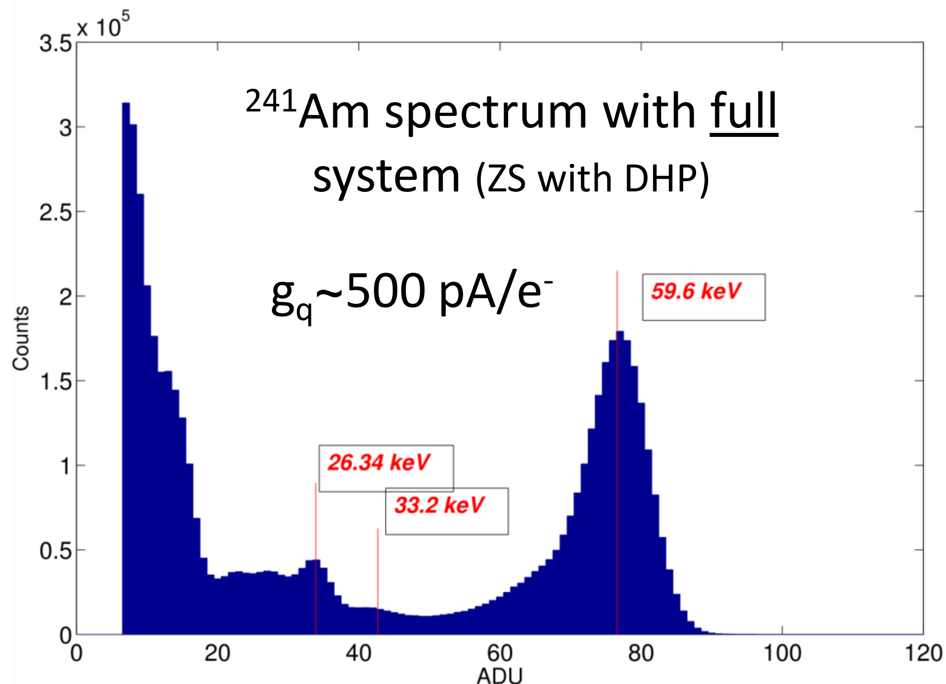
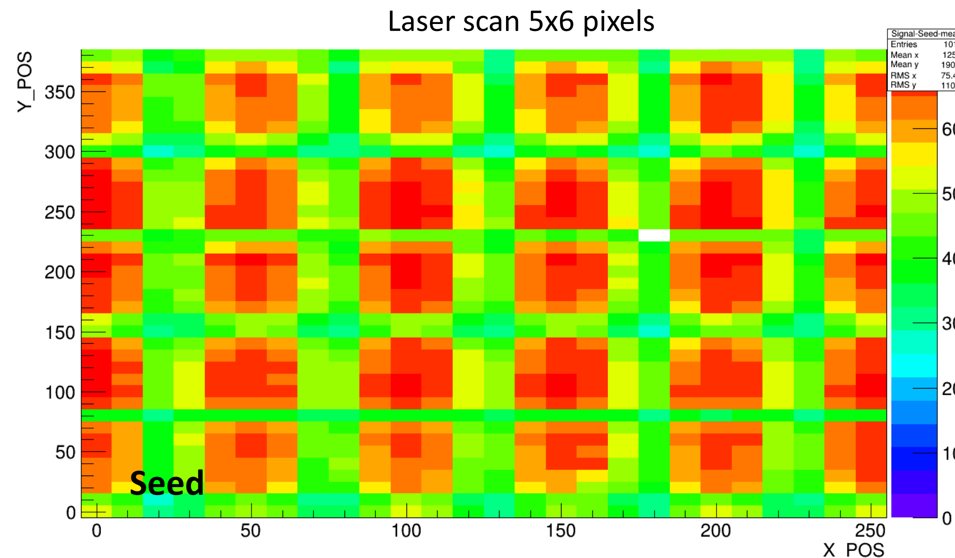
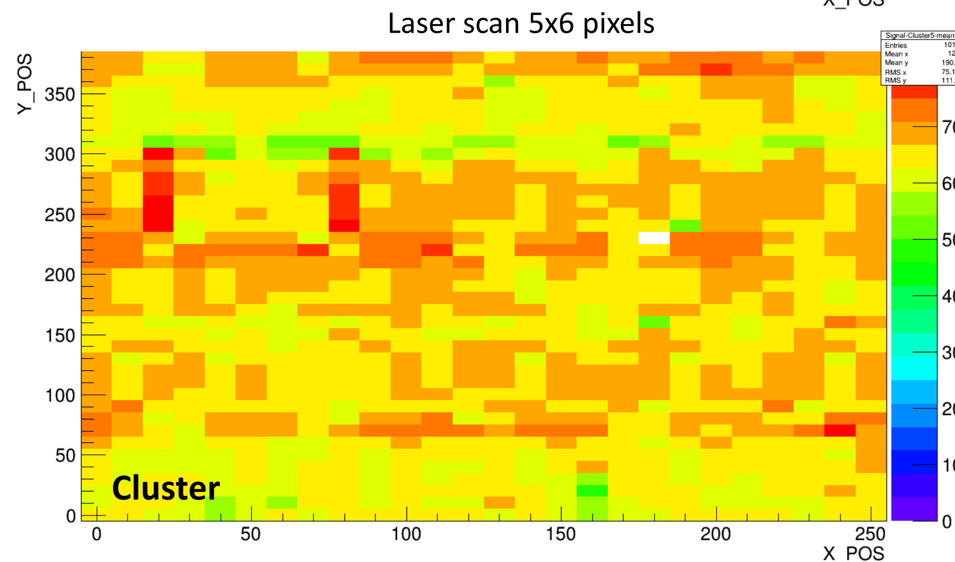
- Biasing optimization (HV, ClearGate, Drift)
- Laser scan
  - Charge collection homogeneity
  - In pixel studies
- Radioactive source
  - System calibration







Homogeneous charge collection

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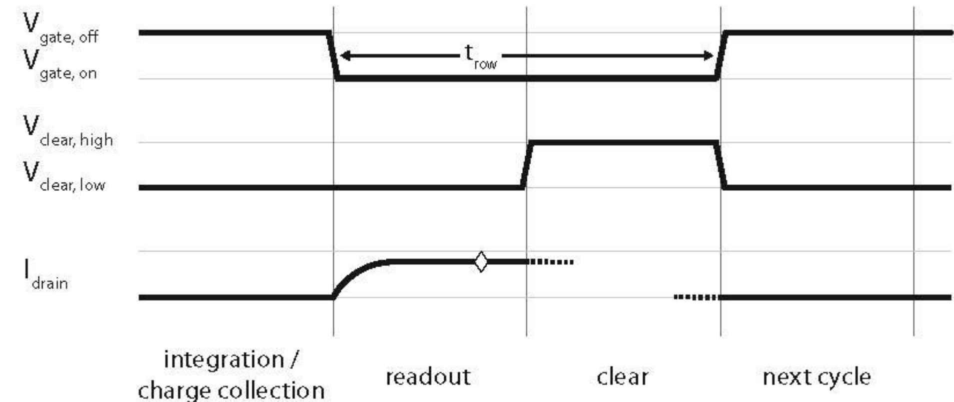
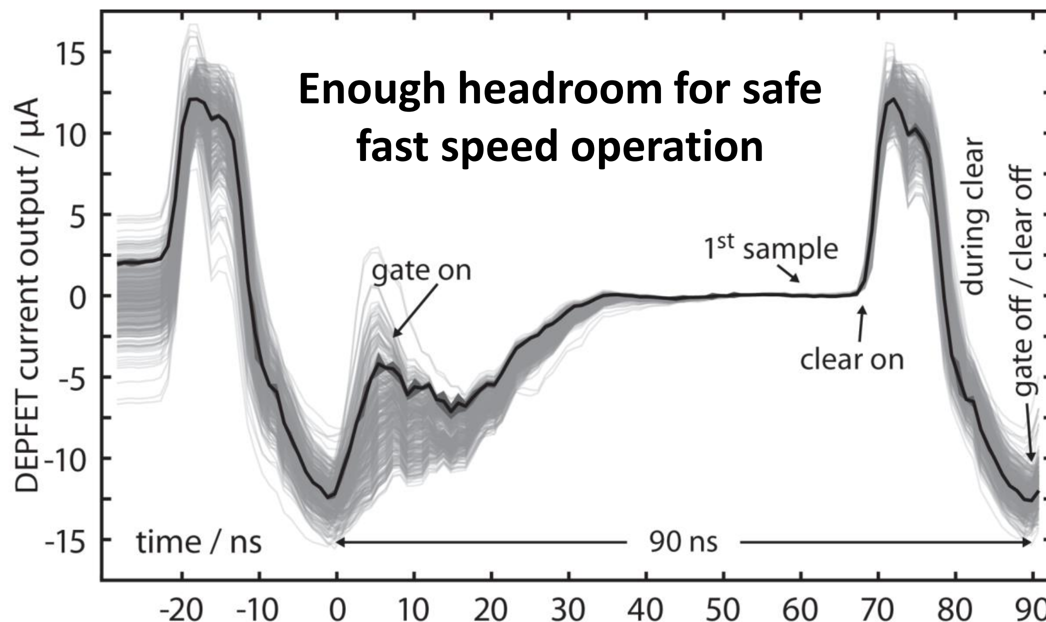
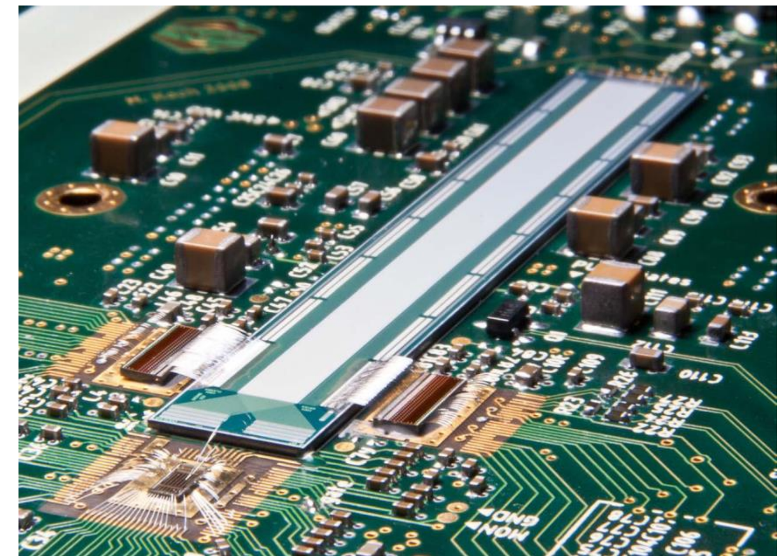
Laboratory tests: DCD

- DCD dynamic measurements
  Readout speed with single sampling
- Belle II PXD frame readout: 20 µs
  (50 KHz frame rate)
- Read-clear cycle: 100 ns
  (768 rows, 4 fold readout)







Long drain lines ~ 60 pF parasitic capacitance

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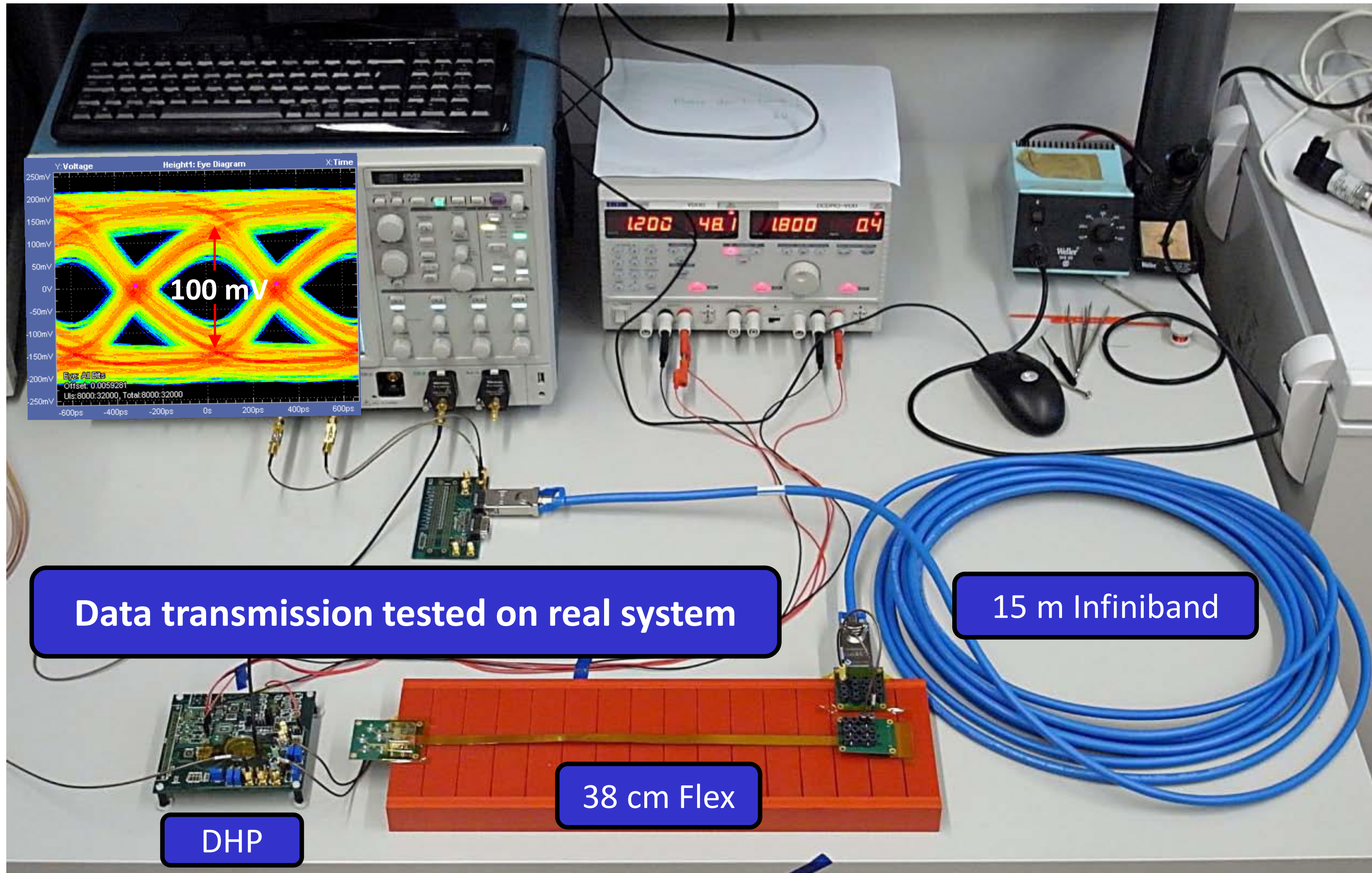
Laboratory tests: DHP serial link



+ pre-emphasis

Irradiated (100 Mrad) DHPT 0.1, can drive 15 m of Infiniband cable

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Beam tests

- DEPFET PXD6 extensively tested over the last campaigns
  - 120 GeV pions at CERN-SPS
  - 1-5 GeV electrons at DESY

- Sensor properties
  - Charge collection homogeneity, operating points, efficiency, angular scans
  - Various pixel sizes, gate lengths, clear structures, drift regions and pixel designs

- System related aspects
  - Power supply prototypes
  - DHH and ONSEN readout

Here, just an appetizer

Beam tests

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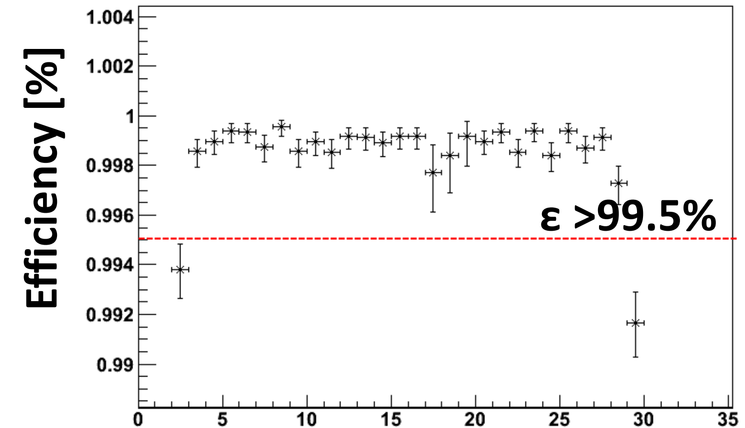
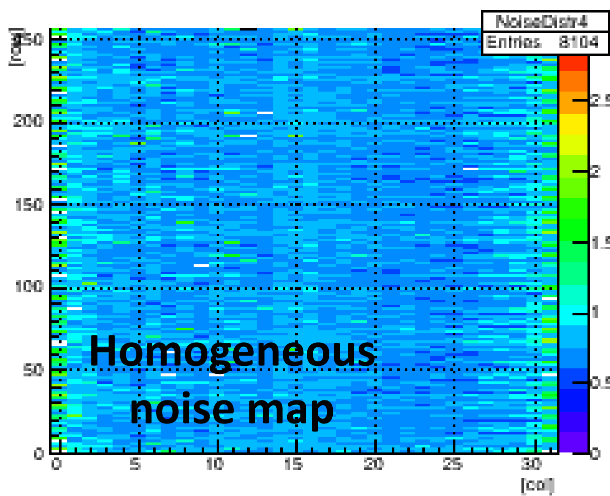
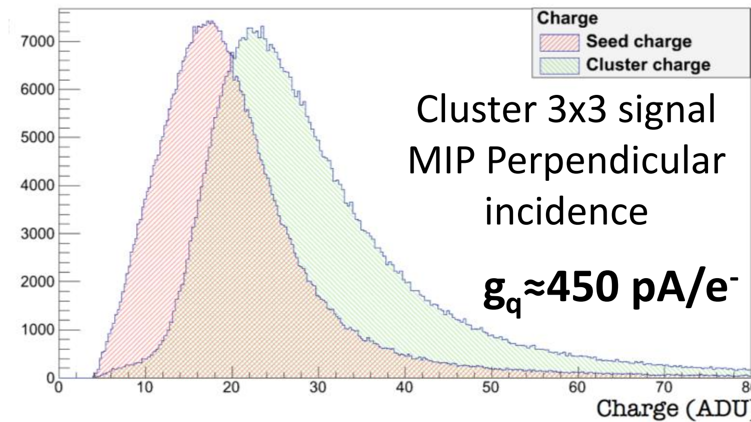
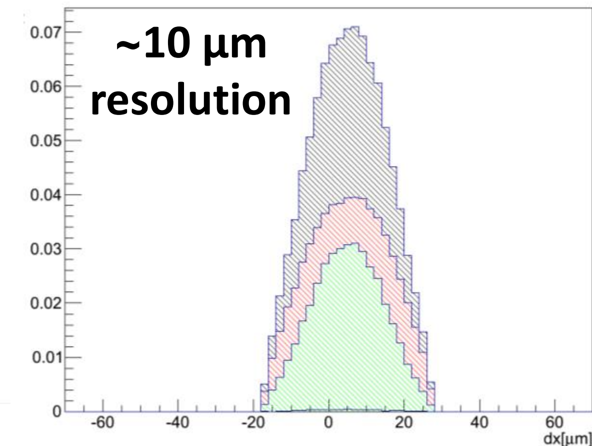
PXD6 Belle II design
Thin **50** µm sensor
Pitch 50x75 µm²
Targeted speed readout
Belle II prototype power supply









Hybrid (Gate length)	Pitch [µm²]	g_q [pA/e⁻]	Residuals [µm]
H.4.1.04 (6 µm)	50x50	275	~ 12 (Perpendicular incidence)
H.4.1.15 (5 µm)	50x75	600	~ 17 (Perpendicular incidence)

Electric MultiChip Module (E-MCM)

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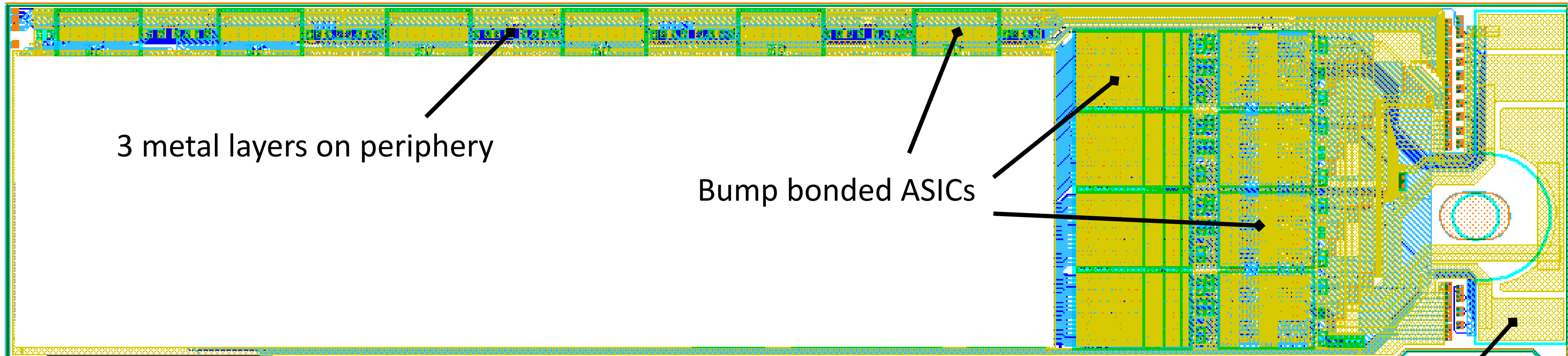
E-MCM: Everything but the DEPFET

Electrically active prototype of a half ladder



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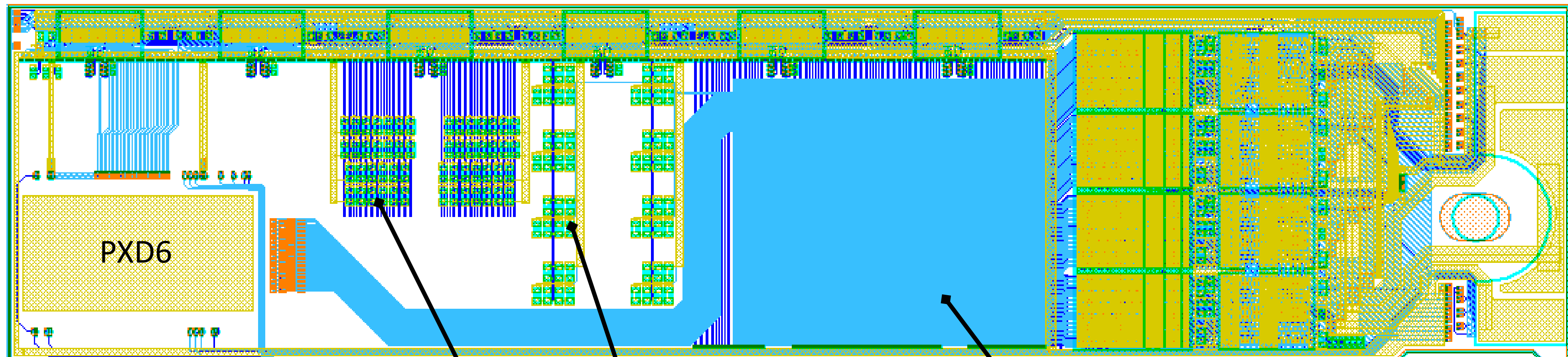

- Metal system as close as possible to final → Electrical information
- Commissioning: Flip chip, discrete components and kapton attachment

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Electric MultiChip Module (E-MCM)

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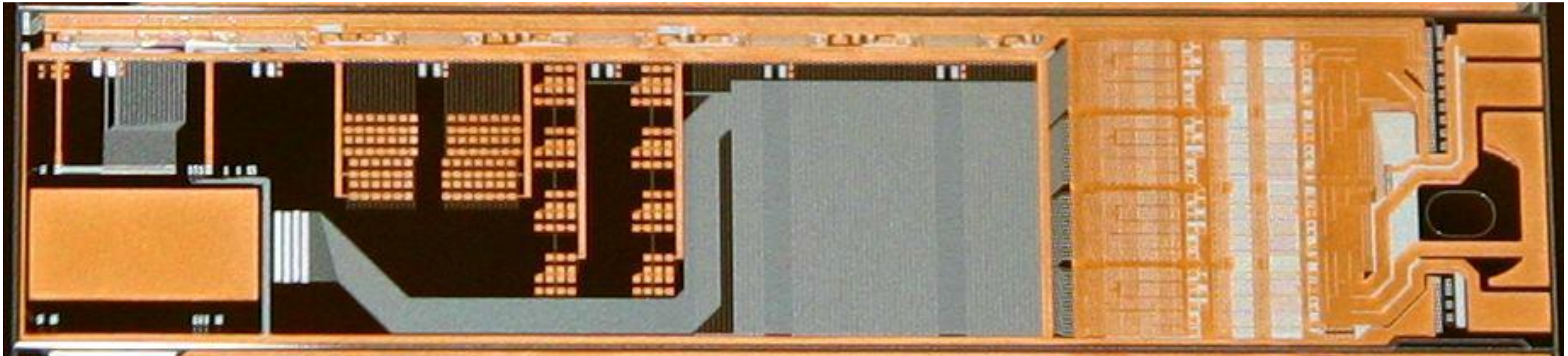
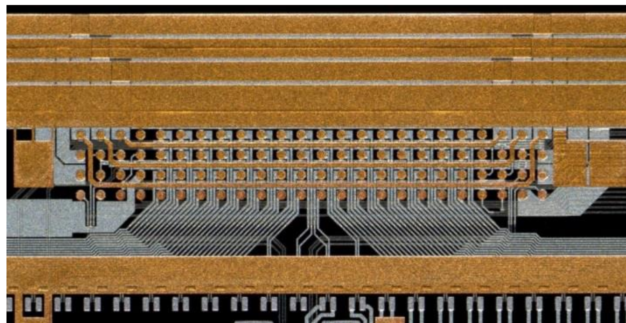
E-MCM in reality

→ **Modules produced, tested and flip chipped**





Detail of the Switcher landing area

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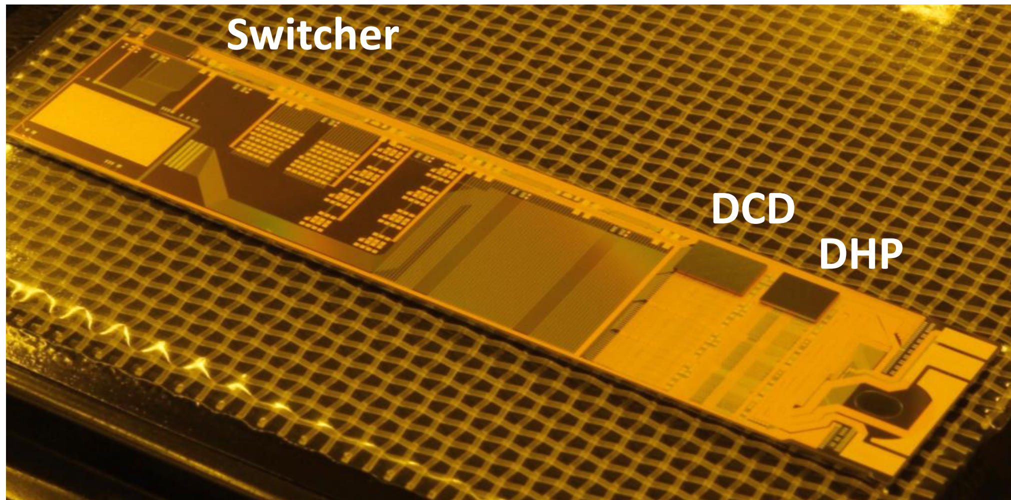
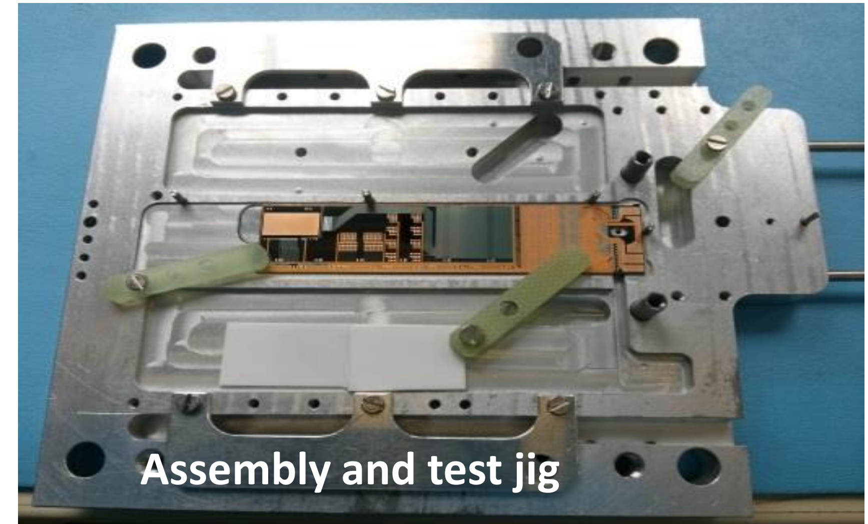
EMCM as today





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Summary

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- The DEPFET Collaboration is developing ultra-transparent pixel sensors with integrated amplification

- The good performance of the DEPFET detector system in terms of SNR, spatial resolution, readout speed is demonstrated

- The Belle II PXD boosted the development of DEPFET detectors
  → Direct benefit towards the ILC-VXD project (ILD-VXD layer concept '*engineered*')

- Building a real system: Every detail (although not covered here) is being considered
  → Cooling, mechanics, DAQ, …

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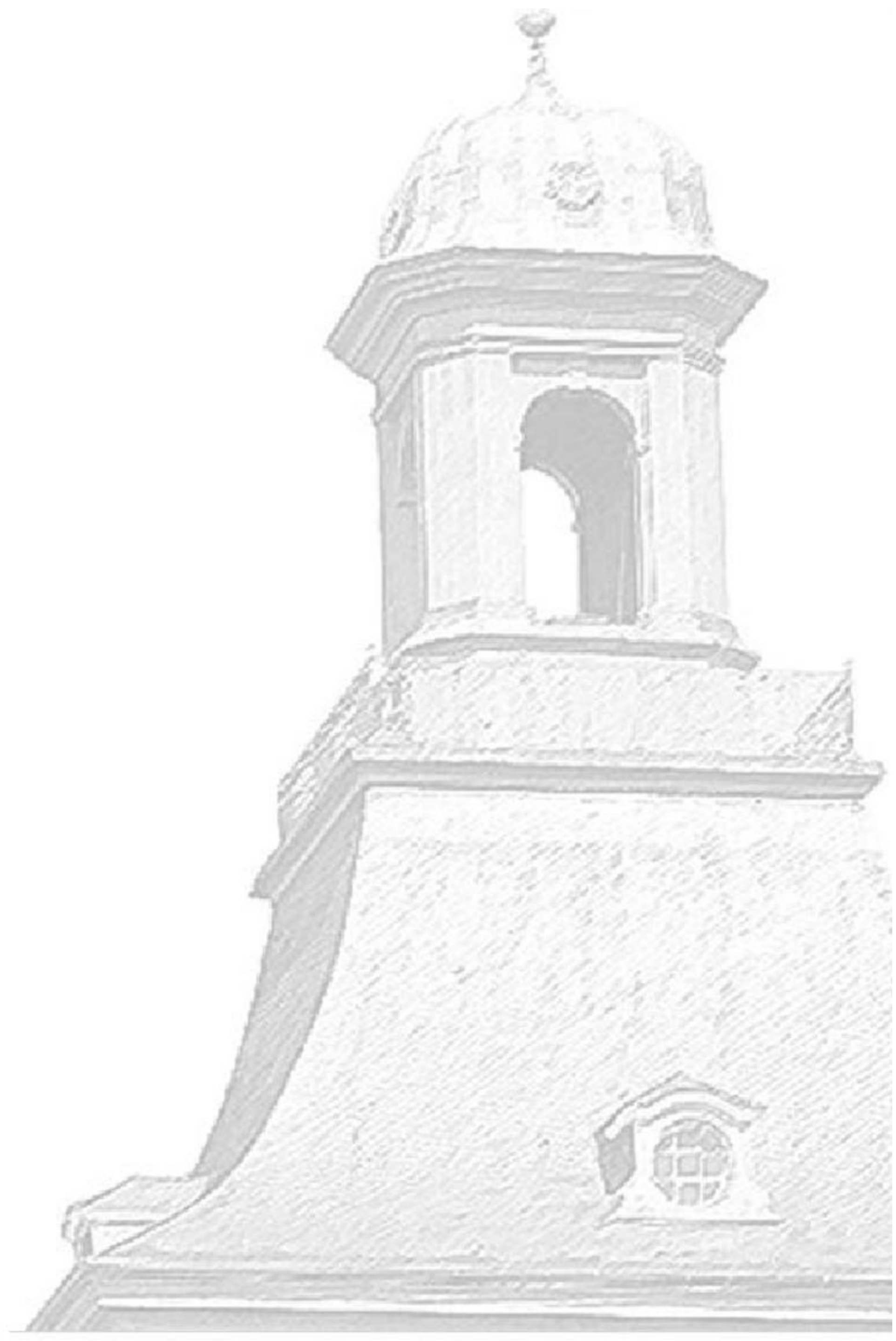
DEPFET

Active Pixel Detector



Thank you

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