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Queen Mary University of London

First Results from Cherwell, a Monolithic Active Pixel Sensor for Particle Physics

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University of BRISTOL

Science & Technology Facilities Council Rutherford Appleton Laboratory

UNIVERSITY OF BIRMINGHAM

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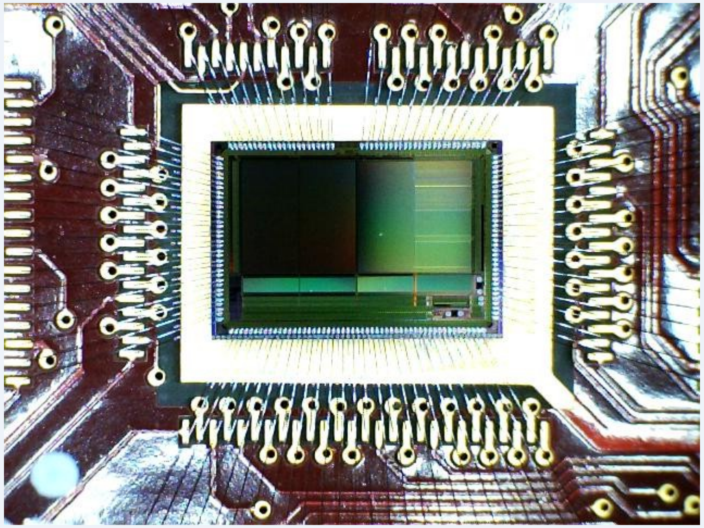
Overview

- **What is an INMAPS device?**
- **The Cherwell chip**
- **Characterisation of chip**
- **Test beam**
  - Correlation Plots
  - Clustering Analysis
  - Efficiency Measurements
- **Future Plans**
- **Summary**



What is an INMAPS Device?

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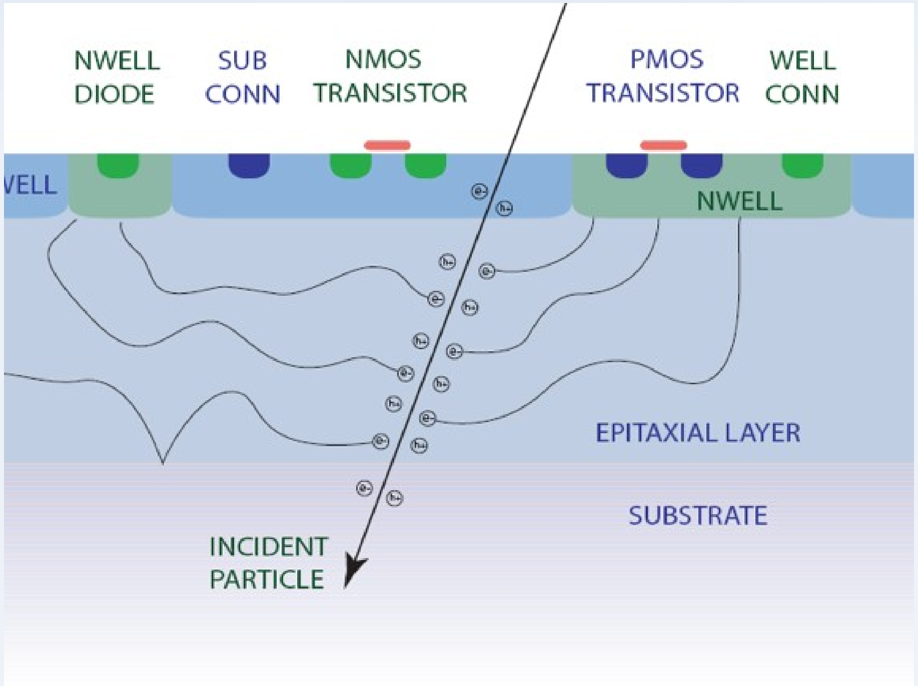
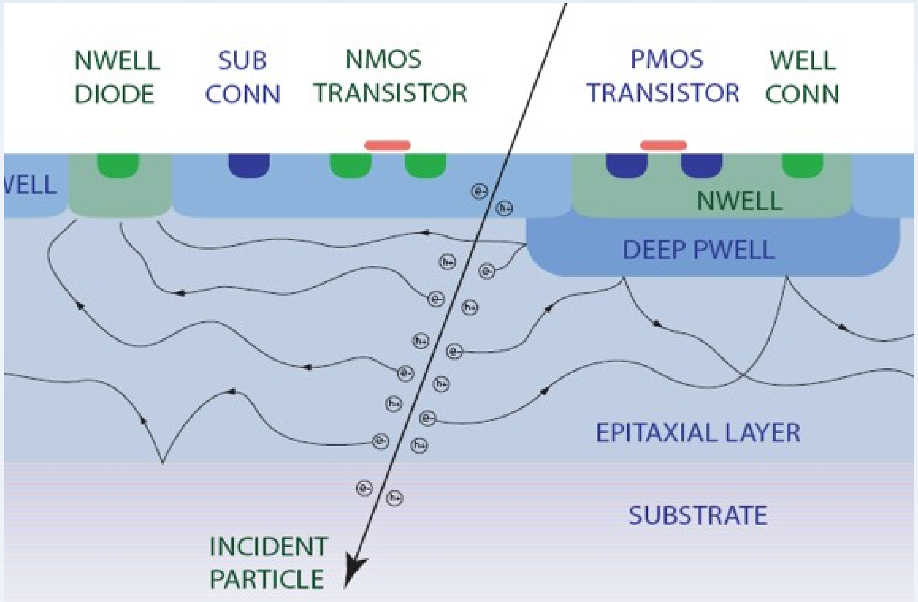
Standard CMOS MAPS



CMOS INMAPS



(Previously TowerJazz 0.18μm process)

- PMOS n-well competes with n-well diode resulting in inefficient regions of a pixel.

- **Added deep P implant.**
  - ➔ Deep p-well shields n-well.
  - Channels charge back into the epitaxial layer.
  - ➔ Increased charge collection efficiency (~ 100%) over whole pixel.

High Resisitivity Epitaxial Layer

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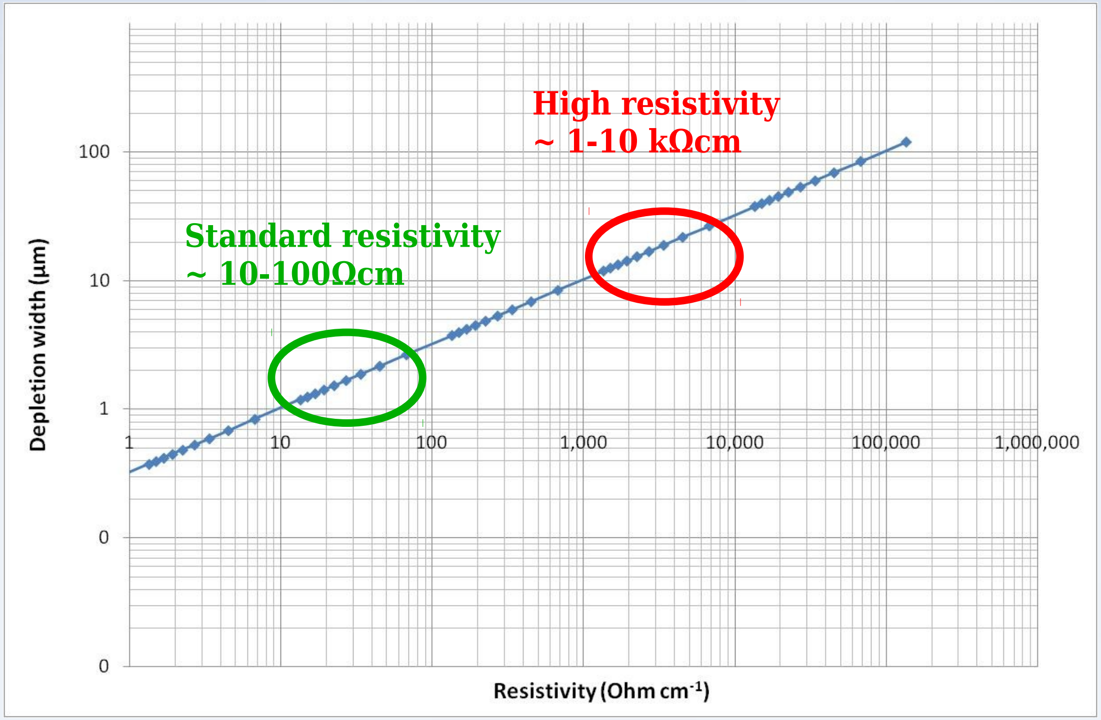
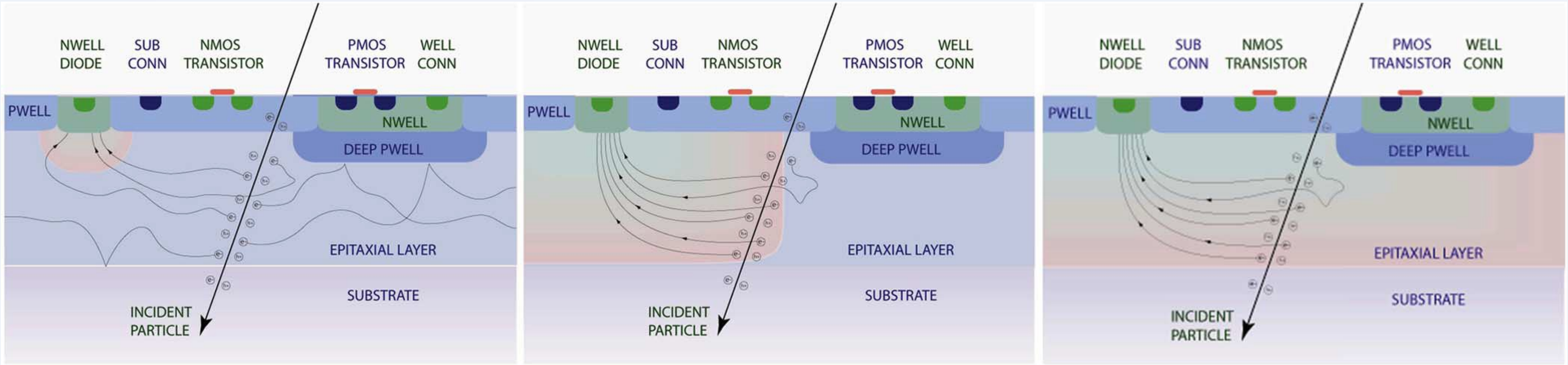


Traditional MAPS

- **Charge collection by diffusion in epitaxial layer.**
  - Slow.
  - Radiation-soft.

High res epi-layer

- **Potential benefits:**
  - Faster charge collection.
  - Reduced charge spread.
  - Increased radiation hardness.



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4 Transistor Technology

<u>3T CMOS</u>

Simple architecture: a diode, reset transistor, source follower transistor and row select transistor.

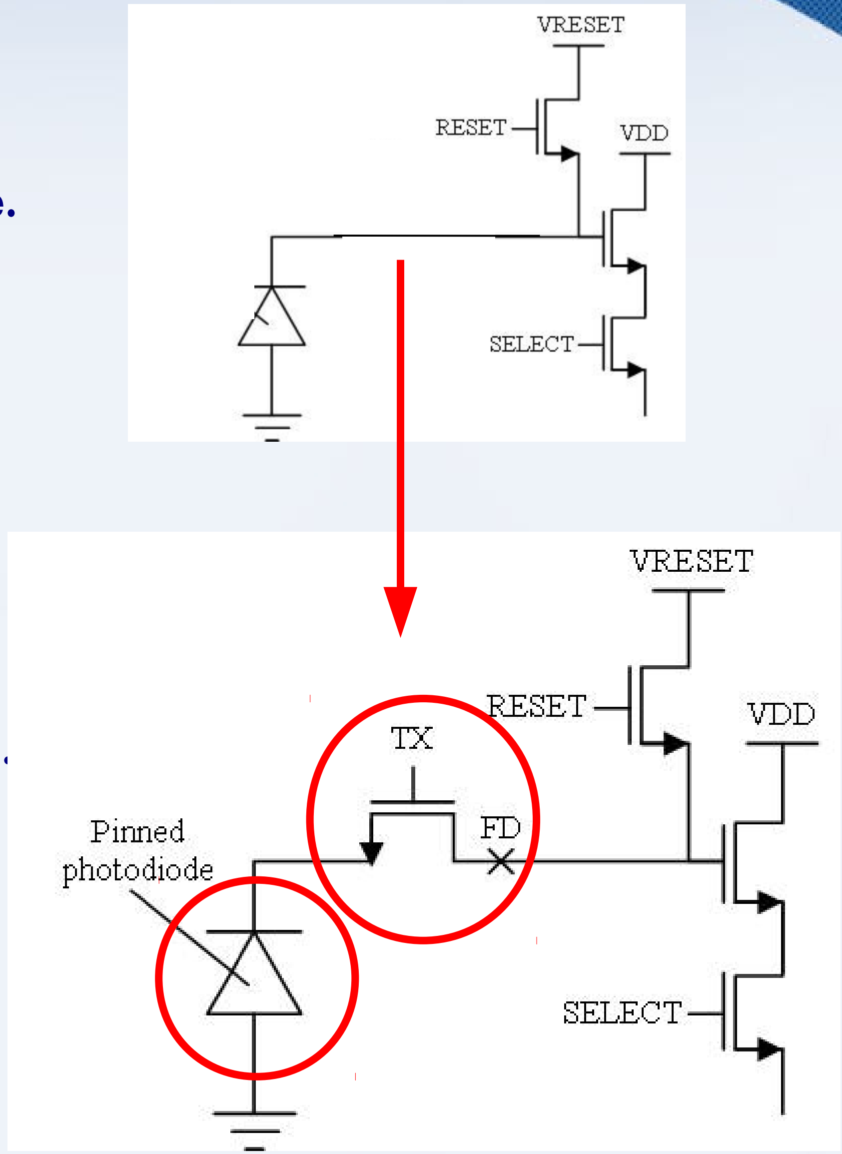
Readout and charge collection node are the same.

<u>4T CMOS</u>

3 additional elements:

1) Floating diffusion node (FD),
2) Transfer gate (TX),
3) Pinned photodiode (instead of normal diode).

Readout and charge collection at different points.



Benefits:

Low noise.
In pixel correlated double sampling.
High conversion gain.

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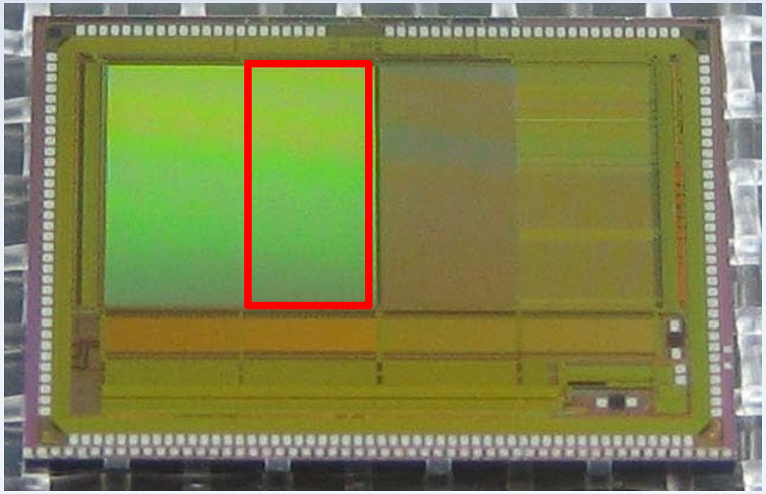
The Cherwell Chip



DECAL-50

- (50 x 50)µm pixels in 48x24 pixel array.
- 1 ADC per column at end of column.

Divided into quadrants of distinct pixel designs.

Each half of chip has different applications:

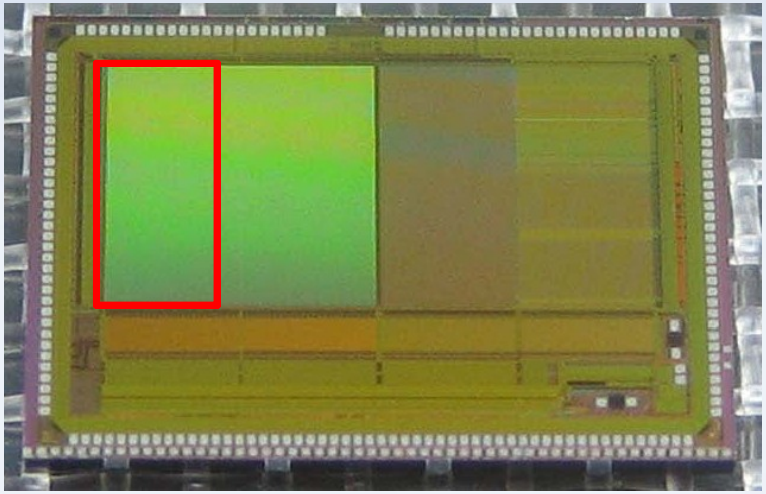
Calorimetry

- **DECAL-50**
- DECAL-25

Vertexing

- Strixel
- Reference Pixels

The Cherwell Chip



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Calorimetry

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- **DECAL-25**

Vertexing

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DECAL-25

- (25 x 25)µm pixels in 96x48 pixel array.
- 1 ADC per column at end of column.
- Circuitry to group 4 of these together to make a virtual 50×50µm pixel.

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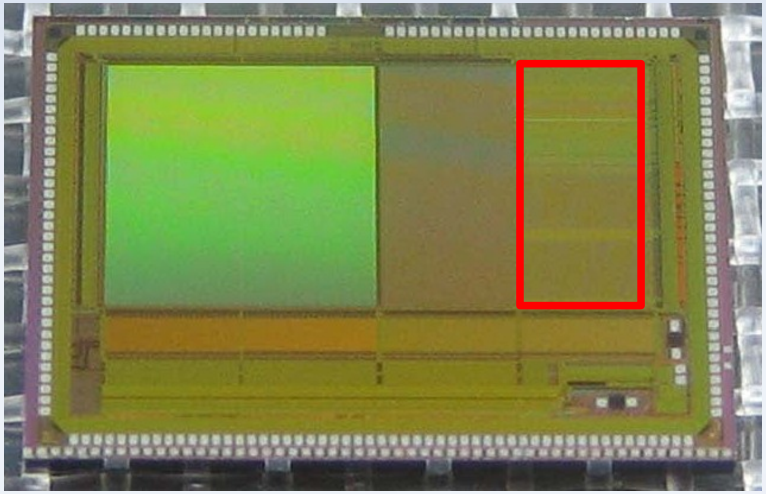
The Cherwell Chip



Divided into quadrants of distinct pixel designs.

Each half of chip has different applications:

Strixel

- (25 x 25)µm pixels in 96x48 pixel array.
- ADC embedded in pixel.
  - Eliminates end-column electronics.
  - Increases active area of the chip.

Calorimetry

- DECAL-25
- DECAL-50

Vertexing

- **Strixel**
- Reference Pixels

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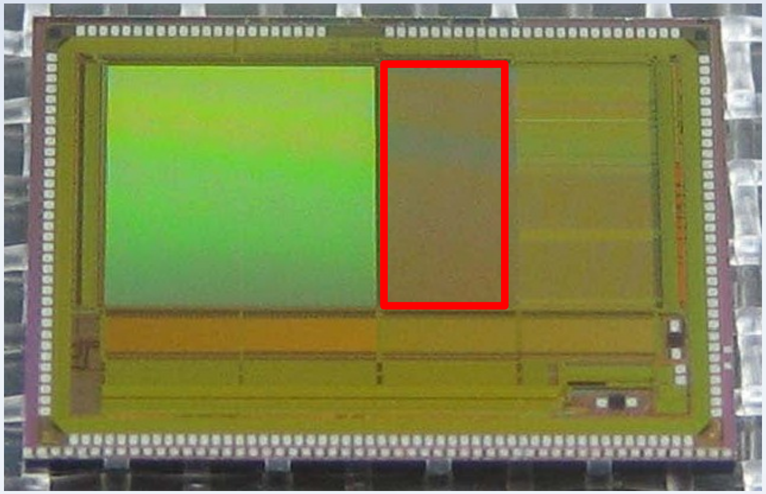
The Cherwell Chip



(Reference) Pixels

- (25 x 25)µm pixels in 96x48 pixel array.
- Test impact of deep p-well on 4T structures.
- **Baseline design: focus of today's talk.**

Divided into quadrants of distinct pixel designs.

Each half of chip has different applications:

Calorimetry

- DECAL-25
- DECAL-50

Vertexing

- **Strixel**
- **Reference Pixels**

Characterisation of chip

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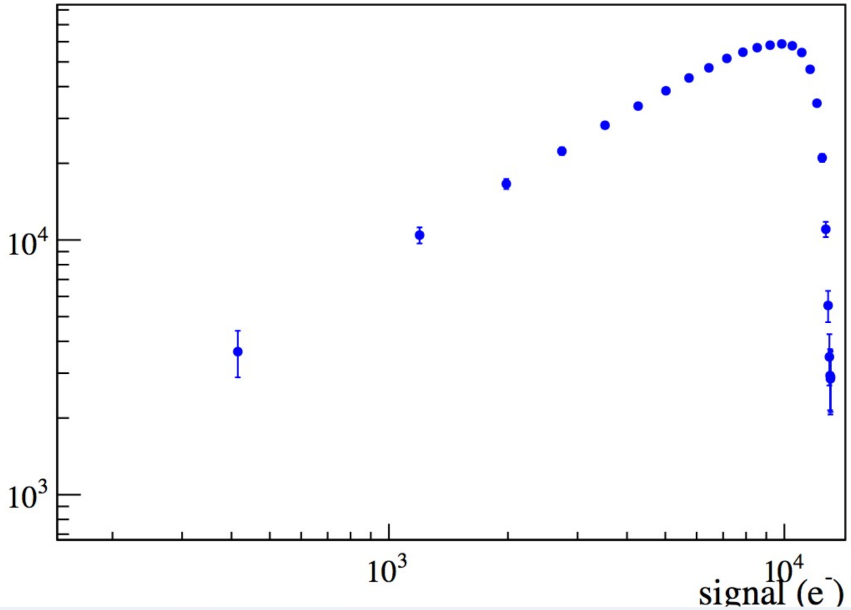
Lab tests to understand performance of chip:

Photon Transfer Curve

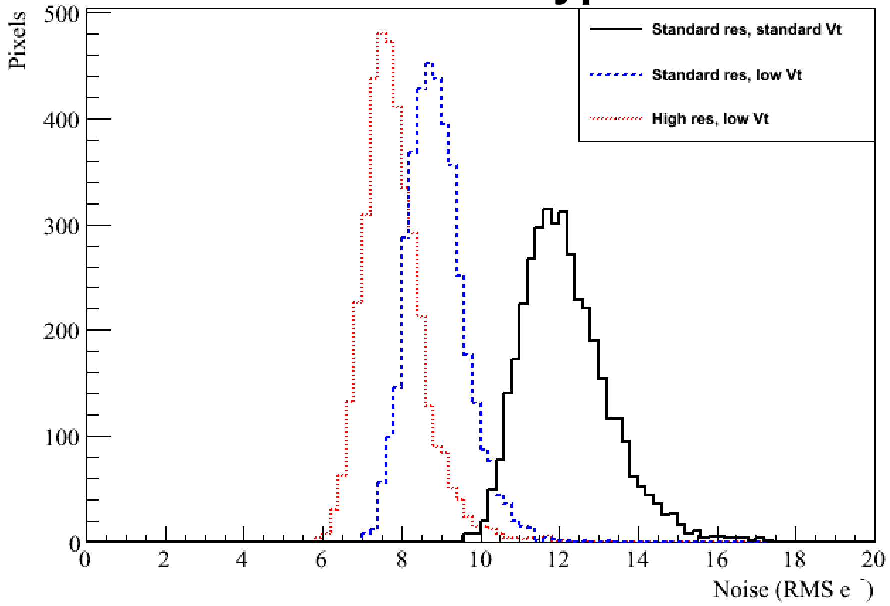


PTC performed using IR illumination.

Linear full well ≈ 11500 e⁻
Maximum full well ≈ 14700 e⁻

In agreement with previous measurements made using Fe-55 source.

Noise for each sensor type



- Noise uniform across sensor.
- Width and mean of noise decreases for higher res epi and low Vt implant as expected.

Mean Noise ≈ 8-12 e⁻ RMS
Gain ≈ 0.17 ADCs/e⁻

Test Beam

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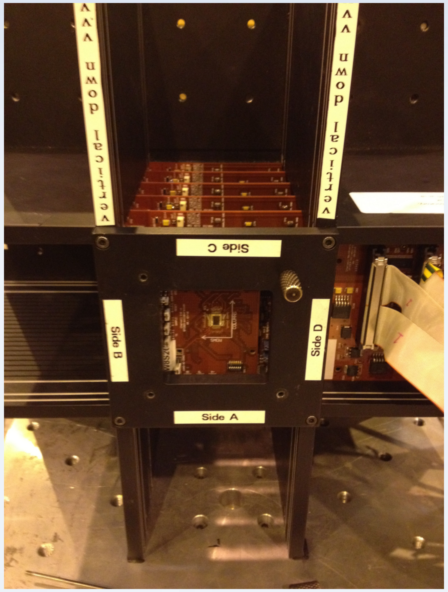
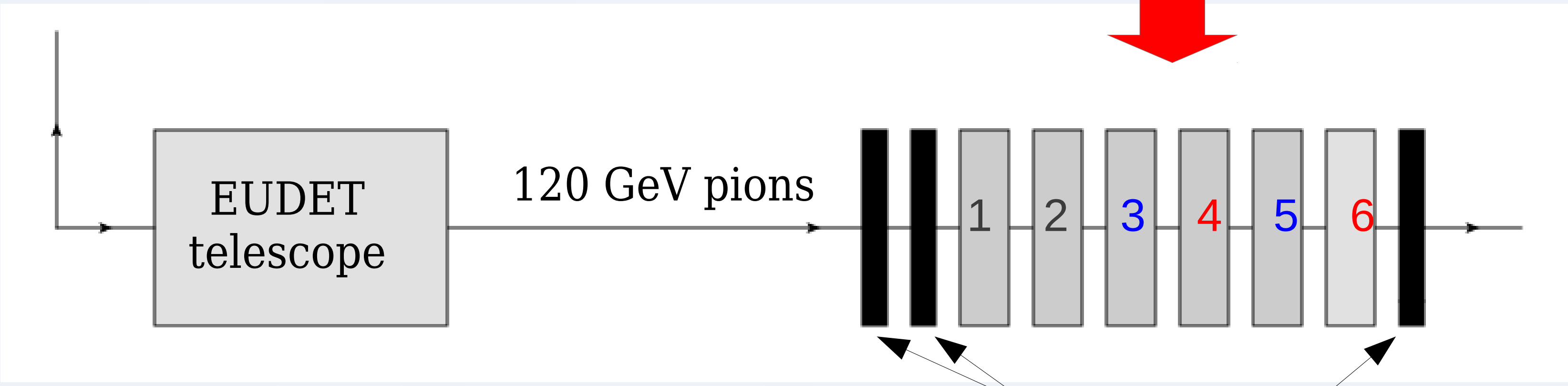
T4 beamline at H6 at CERN, Nov 2012

6 sensor Cherwell stack:

- 2 Standard wafers with low noise Vt implant for the source-drain
- 2 Standard wafers with standard noise Vt implant for the source-drain
- 2 High-resistivity wafers with low noise Vt implant for the source-drain



Aims: to understand resolution, charge sharing and efficiency of Cherwell.



Scintillators
Triple-coincidence trigger

Correlation Plots

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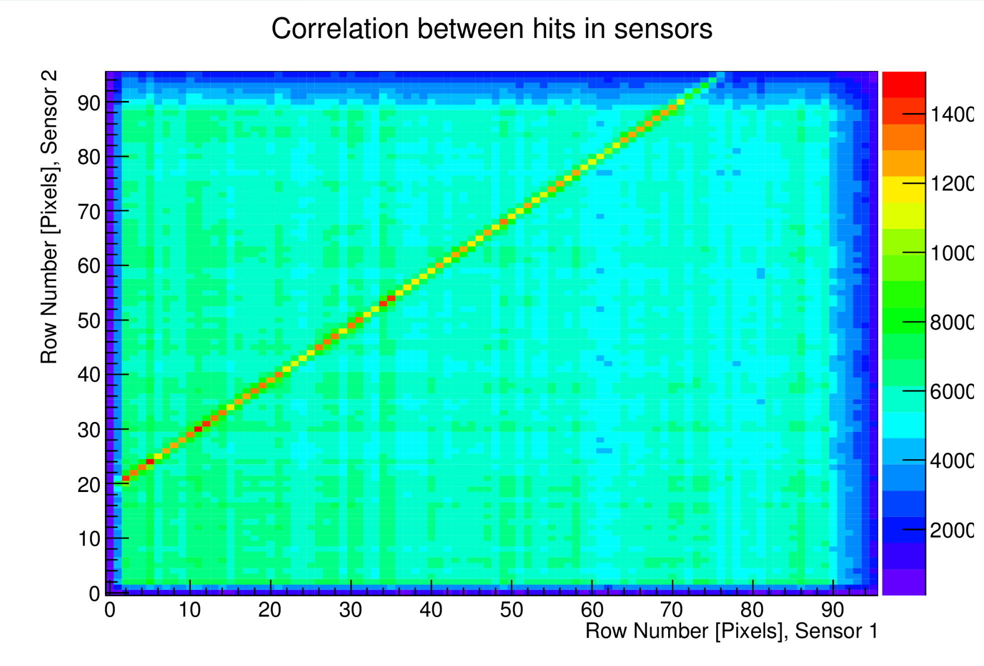
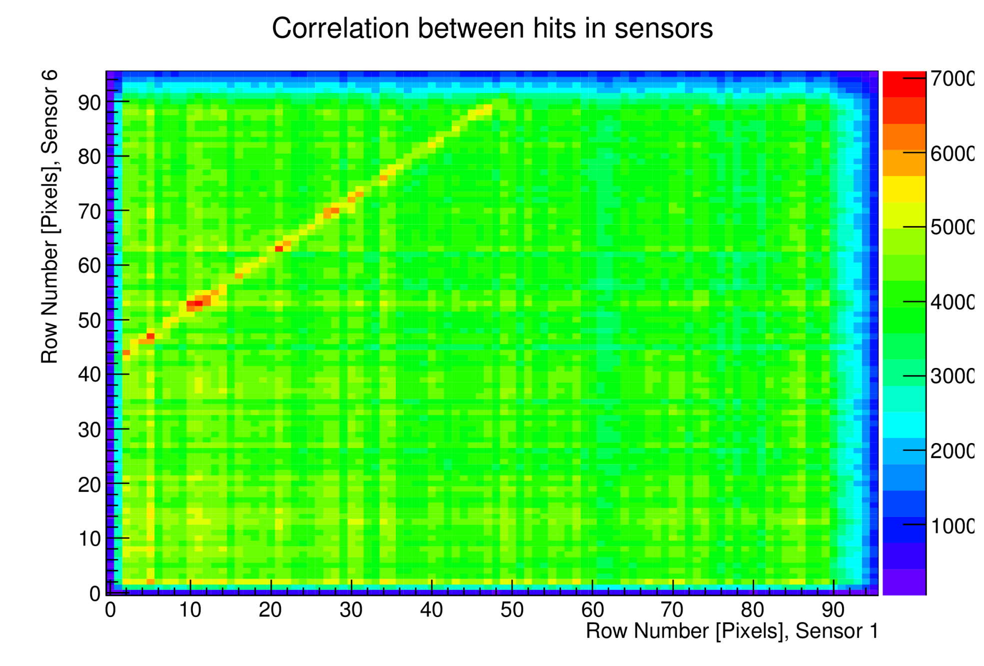
For 1 run of ~60,000 triggers:





Correlation plots show that we see particles crossing the entire detector and are used to align the sensors.

Clustering Analysis

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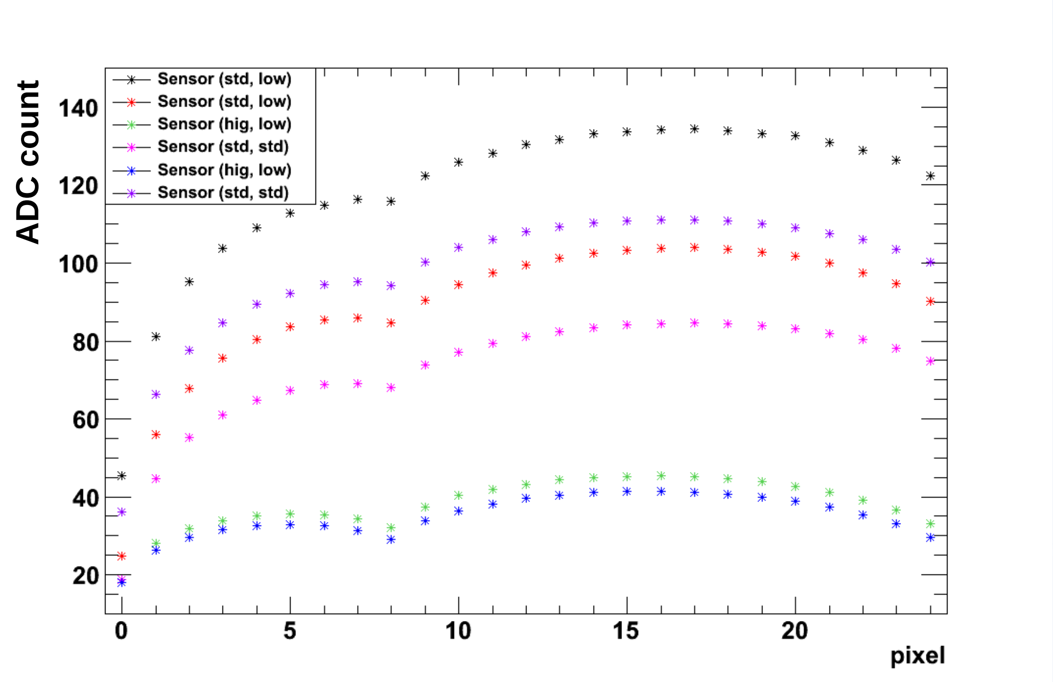
Making clusters

- **Seed** pixel threshold 5σ.
- Check surrounding pixels.
- **Neighbour** inclusion 3σ.
- Weight position according to signal Σ (hits*position)/Σ(hits).



Size of clusters

- Seagull plot shows total signal if:
  a) 3x3 pixel matrix included.
  b) 5x5 pixel matrix included.

- Charge is spread between more pixels in standard resistivity sensors .

Clustering Analysis

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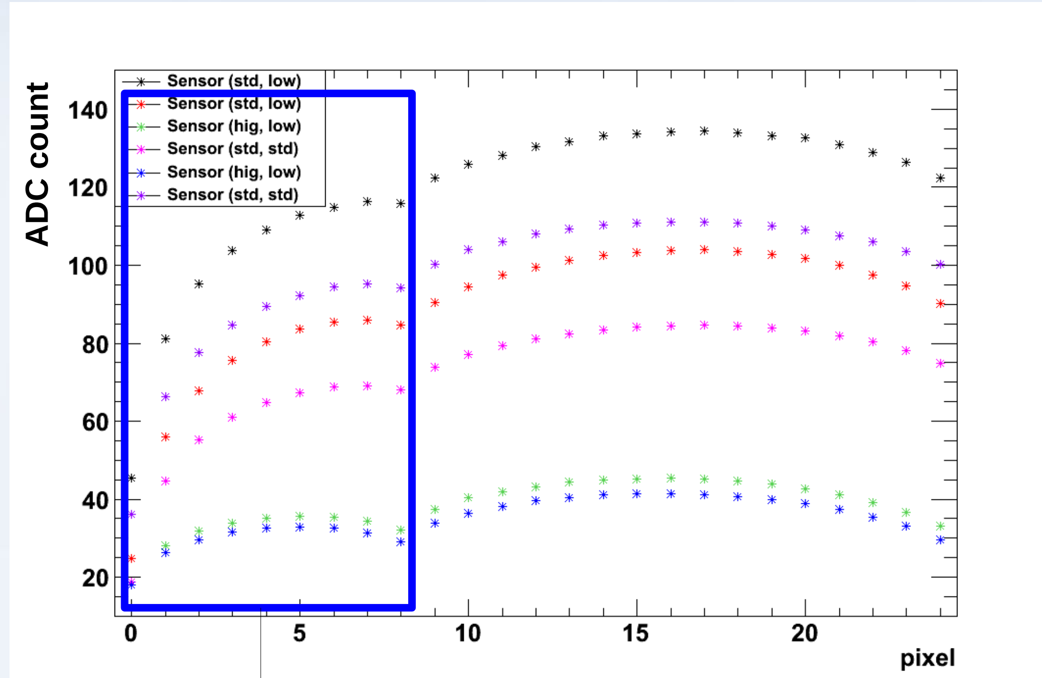
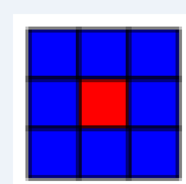


3x3 pixel matrix



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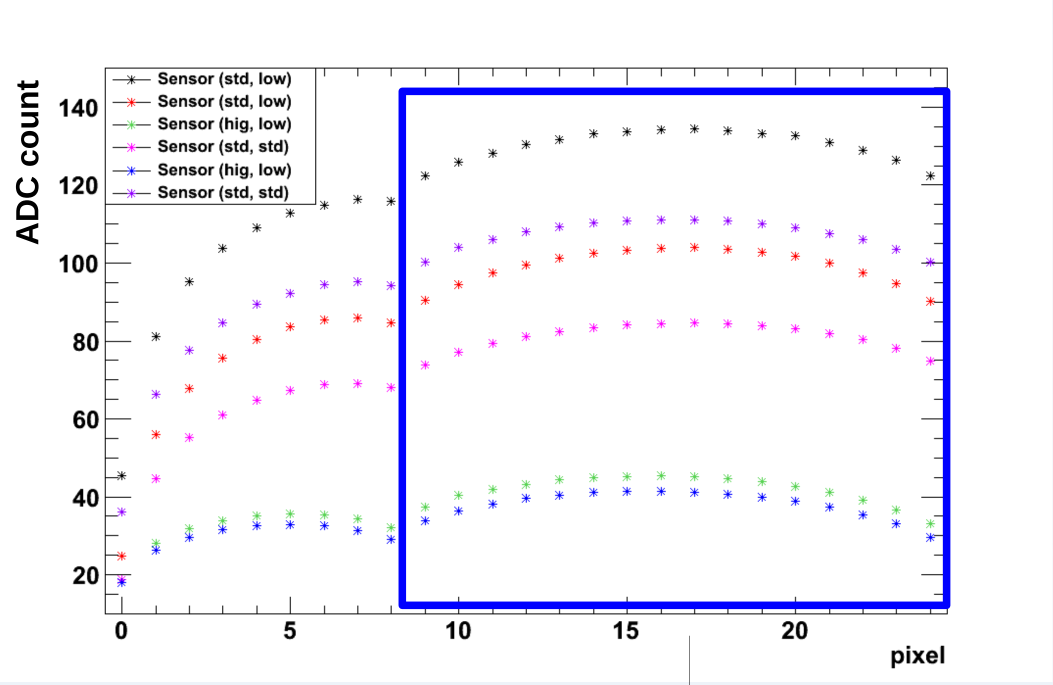

Size of clusters

- Seagull plot shows total signal if:
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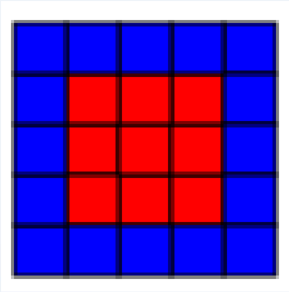
5x5 pixel matrix



Clusters limited to 3x3 matrix as no more information gained from including additional 16 pixels.

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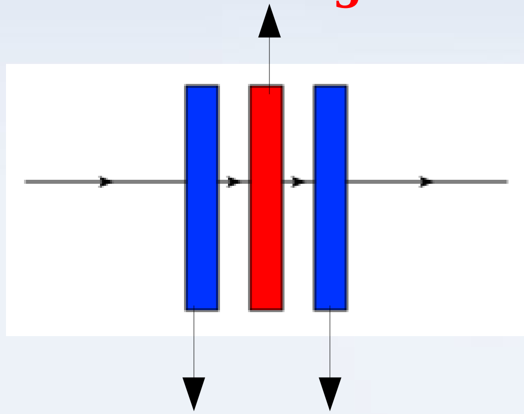
Efficiency Measurements

Sensor being tested



Reference sensors used as double coincidence trigger

$$\text{Efficiency} = \frac{\text{Number of clusters in all 3 sensors}}{\text{Number of clusters in 2 reference sensors}}$$

Preliminary results shown for one run of 58562 triggers:

Standard res, standard Vt:	**99.73%**
Standard res, low Vt:	**99.77%**
High res, low Vt:	**99.89%**

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Future Plans

- Cherwell 1 is first iteration.
- **Cherwell 2** as final device:
  - Similar design to Cherwell 1 strixel.
  - Pixels to be optimised for possible use in ALICE Inner Tracking System.
  - Chip has been fabricated.
  - Results below based on a 128-pixel strixel.

Different timings

	ALICE CDR Inner	ALICE CDR Outer	Pixel 1.8 Stimulus 1	Pixel 1.8 Stimulus 2
Power dissipation	0.3 W/cm^2	0.3 W/cm^2	0.0111 W/cm^2	0.0173 W/cm^2
Temporal + KTC Noise	-	-	17.13 e-	15.36 e-
Readout time	< 30 μs	< 30 μs	21.76 μs	21.76 μs
Pixel size	< (30 x 50) μm	< 70μm	(25x25) μm	(25 x 25) μm

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Summary

- Analysis ongoing but results are looking good.
  - Particles detected through whole sensor stack.
  - Efficiencies are high for all sensors.
  - Hit resolutions to be finalised.
  - Plans to test Strixel and DECAL at DESY test beam soon.

- Cherwell 2 has been designed and fabricated for possible use in ALICE ITS.
  - Performance tests to be carried out shortly.