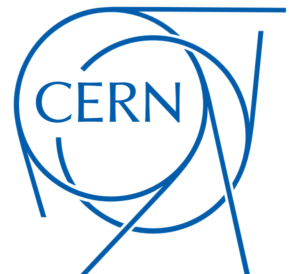
Status of pixel detector R&D for future Linear Colliders

EPSHEP 2013

July 19, 2013
Stockholm

Dominik Dannheim (CERN)
for the ILC and CLIC detector studies



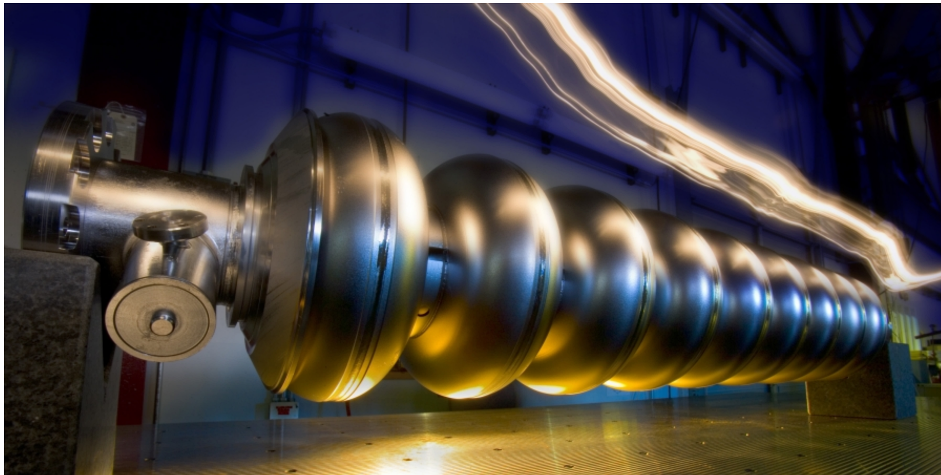
Outline

- Linear Collider concepts: ILC and CLIC
- Vertex-detector requirements
- Detector concepts
- Readout technologies
- Powering, cooling and mechanics

ILC and CLIC

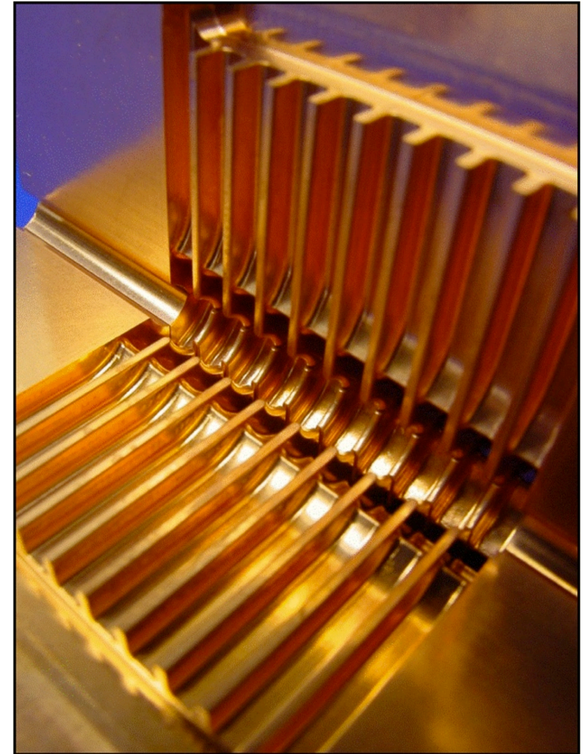
- linear e^+e^- colliders
- luminosities: few 10^{34} $cm^{-2}s^{-1}$
- length: up to ~48 km

ILC



•superconducting RF cavities (like XFEL)
•gradient 32 MV/m
•$\sqrt{s} \leq 500$ GeV (1 TeV upgrade option)
•focus on ≤ 500 GeV, physics studies for 1 TeV

CLIC



•2-beam acceleration scheme operated at room temperature
•gradient 100 MV/m
•$\sqrt{s}$ up to 3 TeV
•physics + detector studies for 350 GeV - 3 TeV

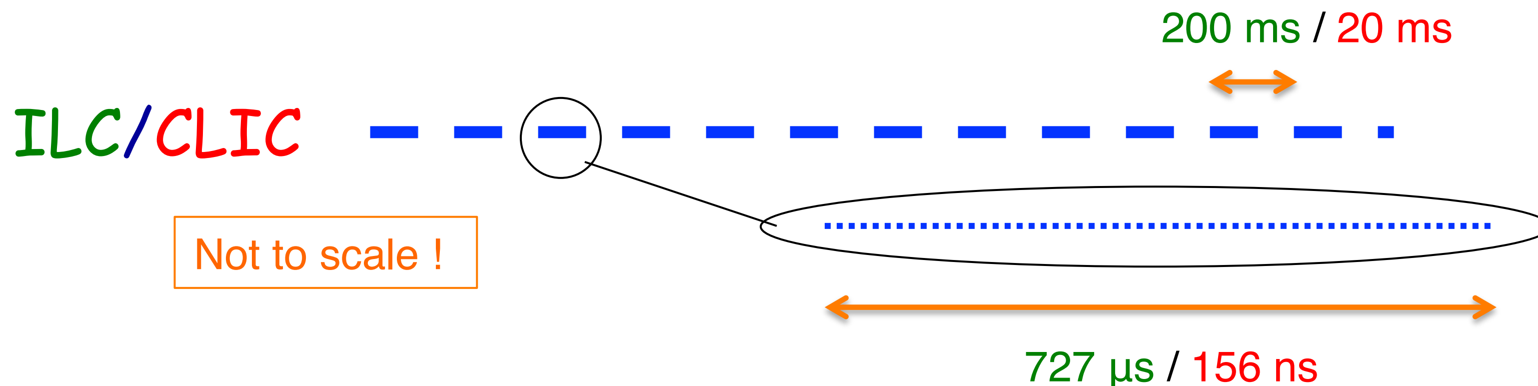
ILC and CLIC machine environment

	ILC at 500 GeV	CLIC at 3 TeV
L ($cm^{-2}s^{-1}$)	$2x10^{34}$	$6{\times}10^{34}$
BX separation	554 ns	0.5 ns
#BX / train	1312	312
Train duration	727 µs	156 ns
Train repetition rate	5 Hz	50 Hz
Duty cycle	0.36%	0.00078%
σ_x / σ_y (nm)	474 / 6	≈ 45 / 1
σ_z (µm)	300	44

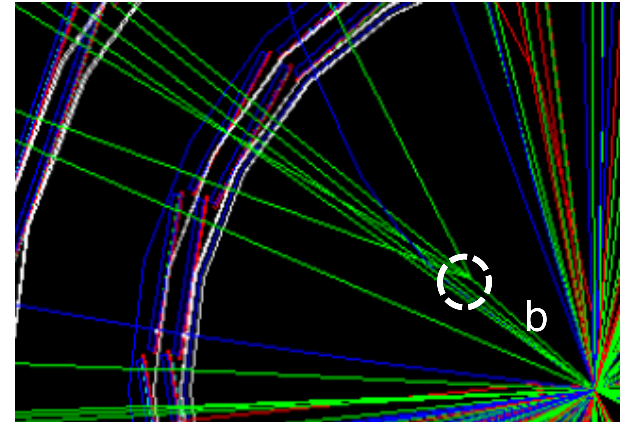
ILC ESD-2012/2 / CLIC CDR

drives timing requirements for detectors

very small beam sizes
→ high rates of e^+e^- and hadronic backgrounds



Vertex-detector requirements



- efficient tagging of heavy quarks through precise determination of displaced vertices:

$$\sigma(d_0) = \sqrt{a^2 + b^2 \cdot \mathrm{GeV}^2/(p^2 \sin^3\theta)}$$

a~5 μm, b~10-15 μm

→ good single point resolution: σ_{SP}~3 μm
  → small pixels <~25x25 μm², analog readout

→ low material budget: X ≲ 0.1-0.2% X_0 / layer
  → corresponds to ~100-200 μm Si, including supports, cables, cooling
  → low-power ASICs (~50 mW/cm²) + gas-flow cooling

- 20-200 ms gaps between bunch trains → trigger-less readout, pulsed powering
- B = 4-5 T → Lorentz angle becomes important

- few % maximum occupancy from beam-induced backgrounds
- moderate radiation exposure (~10^4 below LHC!):
  - NIEL: < 10^{11} n_{eq}/cm²/y
  - TID: < 1 kGy / year

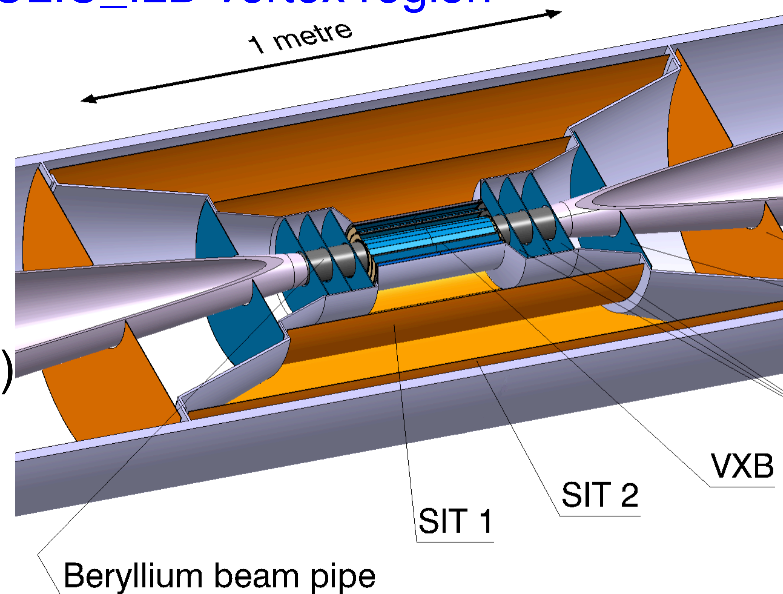
- for CLIC: Time stamping with ~10 ns accuracy, to reject background
  → high-resistivity sensors, fast readout

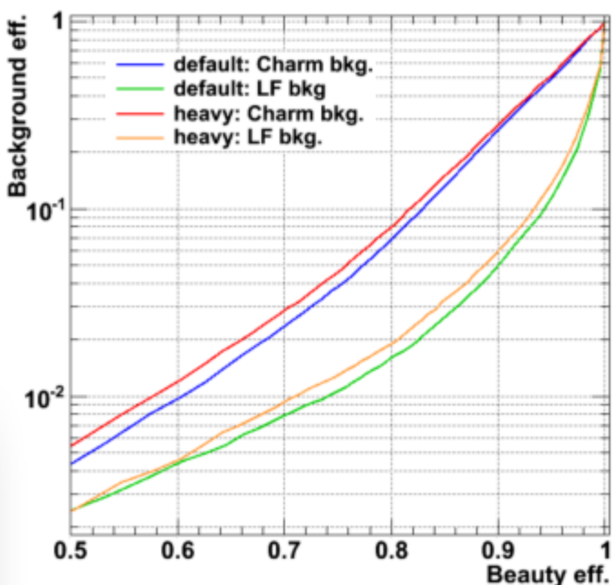
Vertex-detector concepts for ILC + CLIC

ILD & SiD detector concepts:

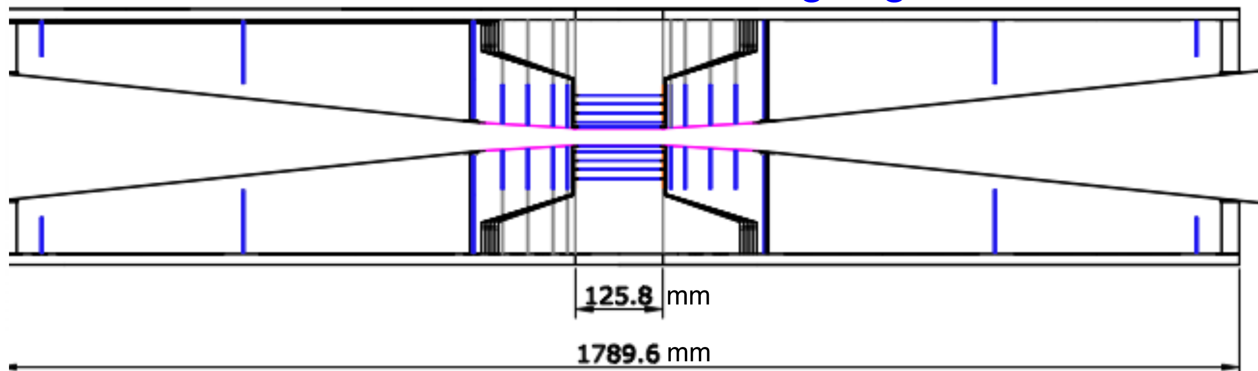
- systematic optimization of geometries:
  - background occupancies
  - detector performance
- barrel/endcap geometry
- 3 double layers or 5 single layers
- R_i between 14 mm (SiD) and 29 mm (CLIC_ILD)
- beam pipes with conical sections

CLIC_ILD vertex region





SiD vertex and forward tracking region

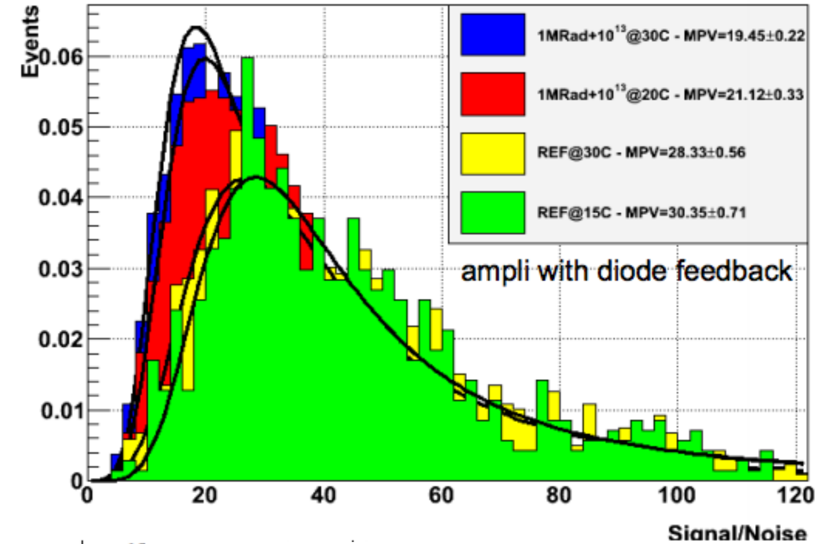


Integrated r/o technology: MAPS

Monolithic Active Pixel Sensor (MAPS):

- integrated CMOS technology
- low-resistivity substrate, charge collection mainly through diffusion

MIMOSA 32ter



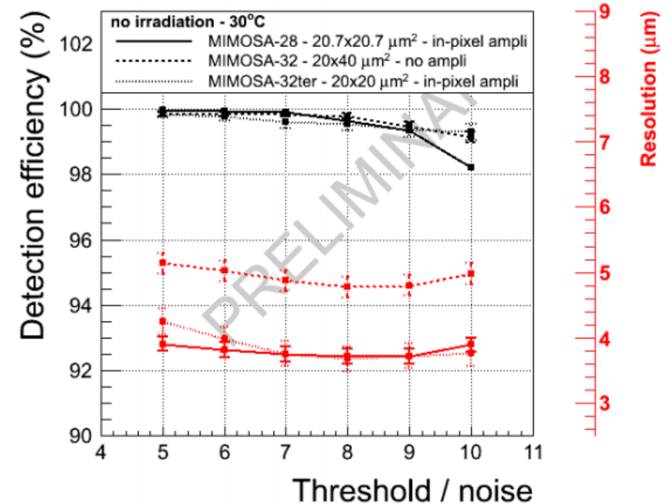
Example: evolution of MIMOSA chip family (IPHC)

- **MIMOSA 26/28**:
  - 0.35 µm process
  - 50 µm sensor thickness, ~20 µm pitch
  - 14 µm epitaxial layer, >0.4 kΩcm
  - binary r/o in 100-200 µs (rolling shutter)
  - used in EUTelescope and STAR experiment
- **MIMOSA 32/34:**
  - 0.18 µm Tower-Jazz CIS process:

    higher integration → faster/smarter
  - 18-40 µm epitaxial layer, 1-6 kΩcm
- **MIMOSA 32ter**: like MIMOSA 32, but in addition:
  - in-pixel amplification & CDS
  - improved radiation tolerance

Proposal for ILC ($\sqrt{s}$=500 GeV) vertex detector:

- precision layer with 3 µm resolution, 50 µs r/o time
- timing layer with 6 µm resolution, 10 µs r/o time
- outer layers with 4 µm resolution, 100 µs r/o time

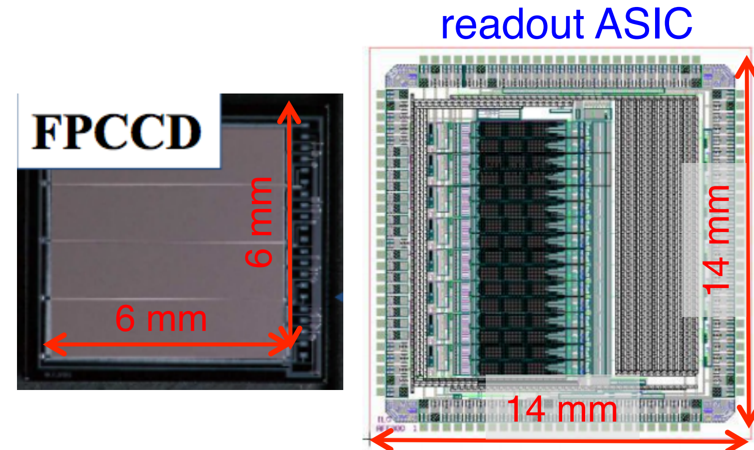


→ talk on CMOS pixel sensors by Isabelle Ripp

Integrated r/o technology: FPCCD

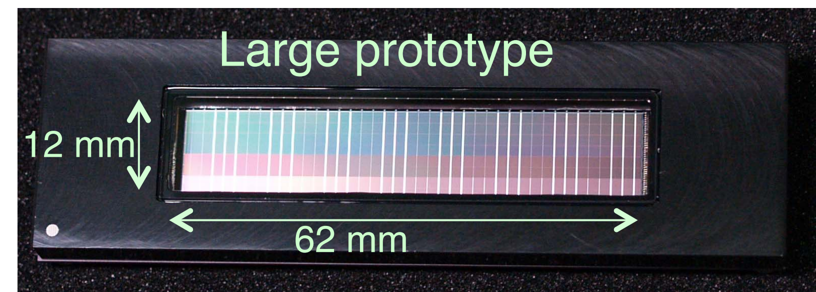
Fine Pixel Charge-Coupled Device:

- 5-10 µm pixel pitch (10^{10} px for ILD VTX!)
- ~15 µm depletion zone,
  to enhance drift + limit diffusion
- integrate over ILC bunch trains,
  r/o during gaps ~ 10 MPx/s
  → no time stamping, background
  rejection by pattern recognition



- operation at -40 °C in cryostat
  (2-phase CO_2 cooling system)
  to ensure radiation tolerance,
  limit power consumption (~10 mW/ch)
  and increase r/o speed

- small and large prototypes built:
  6x6 mm² and 6.2x1.2 cm²
  50 µm thin wafer
  6, 8, 12 µm pixel pitch



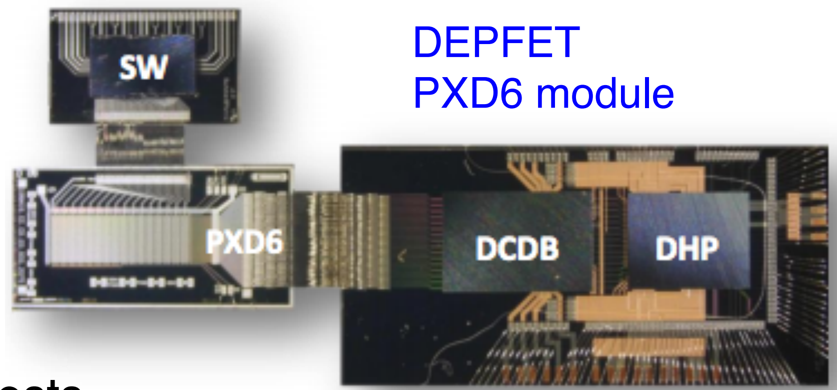
Other integrated r/o technologies

Depleted Field Effect Transistor (DEPFET):

- depleted layer under FET, potential minimum in channel → charge accumulation
- monolithic sensor, but r/o separate

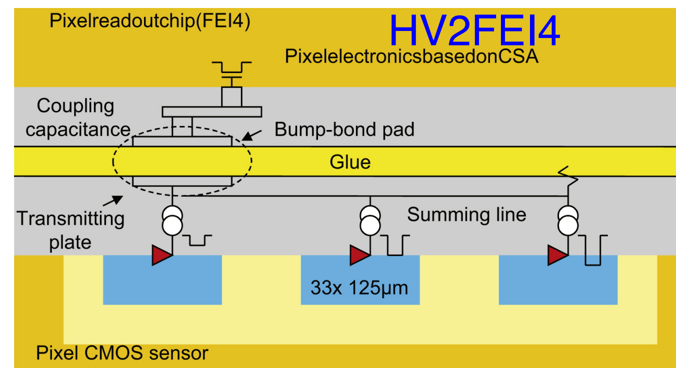
→ thin (~50 µm), small pixels (~25x25 µm²)

- readout with ~20-100 µs frame time
- Belle II baseline technology
- ladder prototype built (PXD6, 50 µm), beam tests
- talk by Carlos Marinas in this session



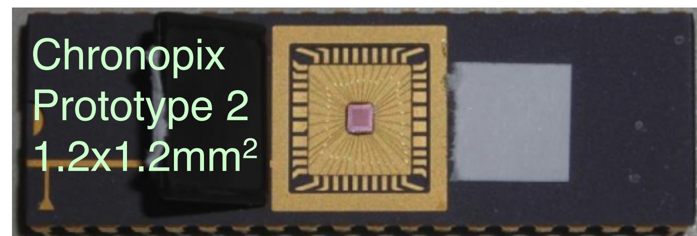
HV-CMOS MAPS:

- Deep-Sub-Micron High-Voltage CMOS process: Vbias~100 V → depletion layer ~10-20 µm
- integrated sensors with fast signal collection
- hybrid option: Capacitive Coupled Pixel Det. (CCPD)
- talk by Sergio Gonzalez Sevilla in this session



Chronopix:

- monolithic CMOS pixel sensor with time stamping
- prototype in IBM 90 nm process, 25 µm pixels
- challenges: cross-talk and large sensor capacitance



Hybrid r/o technology: CLICPix

- **65 nm CMOS hybrid r/o chip**, targeted to CLIC vertex detectors
- based on **Timepix/Medipix** chip family, synergy with HL-LHC pixel r/o projects (**RD 53** collaboration on 65 nm r/o)

- **demonstrator chip** produced with fully functional 64 x 64 pixel matrix
- **25 µm** pixel pitch
- simultaneous **4-bit time (TOA) and energy (TOT)** measurement per pixel

→ front-end **time slicing < 10 ns**

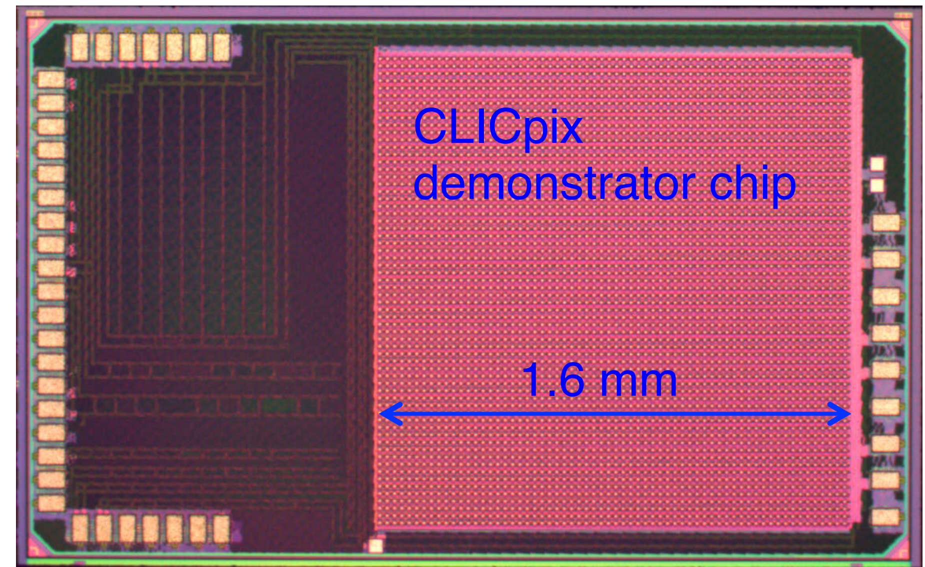
- selectable **compression** logic: pixel, cluster + column-based

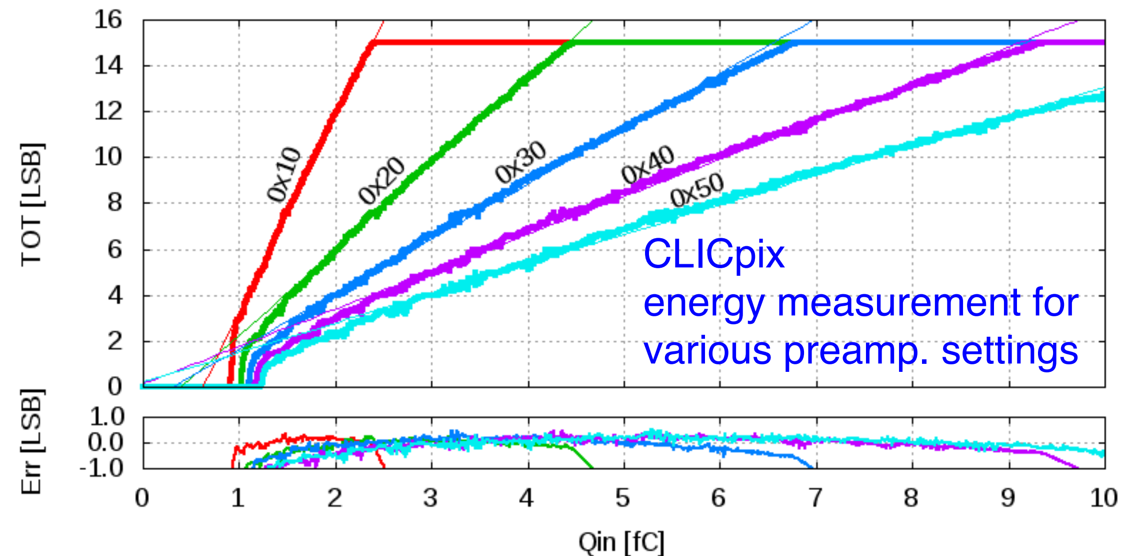
→ full chip r/o in less than 800 µs (at 10% occup., 320 MHz r/o clk)

- **power pulsing scheme**

→ P_{avg} < 50 mW/cm²

- **r/o tests** on prototypes:
  - chip fully functional
  - measurements confirm simulations





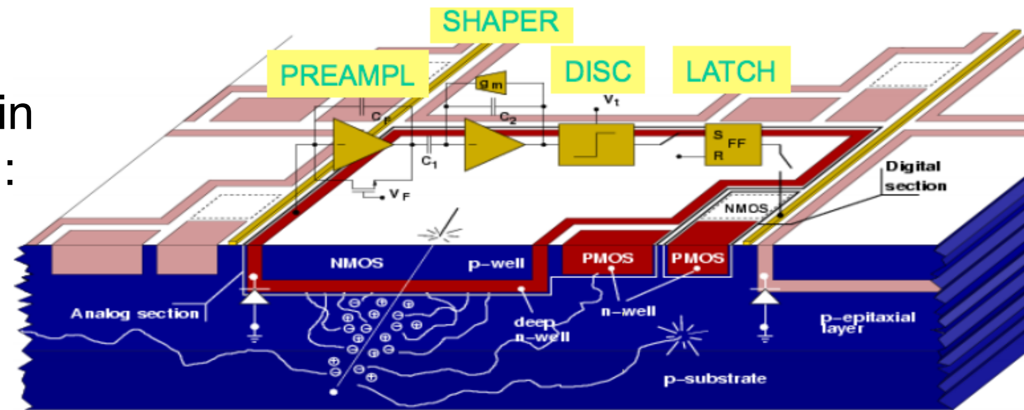
3D r/o technology: Deep N-well CMOS

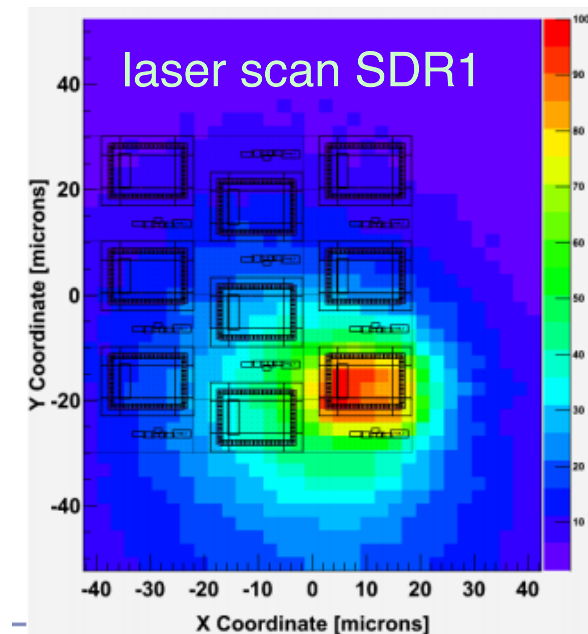
3D Deep N-well CMOS:

- functionality of hybrid pixel detector in monolithic devices by 3D integration: sparsification, time stamping
- charge-to-voltage conversion in charge preamp
- can extend collecting n-well electrode to increase fill factor + efficiency
- multi-project-wafer run through Tezzaron:
  - many technical problems, 3y turnaround
  - now fully functional 3D chips produced (SDR1)
  - 2 tiers, 20x20 μm^2 pixels in 240x256 matrix
  - analog frontend measurements:
    700 mV/fC, 40 e$^-$ ENC, 5 μW/px
  - lab + test-beam measurements, irrad. (1 Mrad)
- originally developed for Super-B
- exploring design with ~200 ns per-pixel time stamps

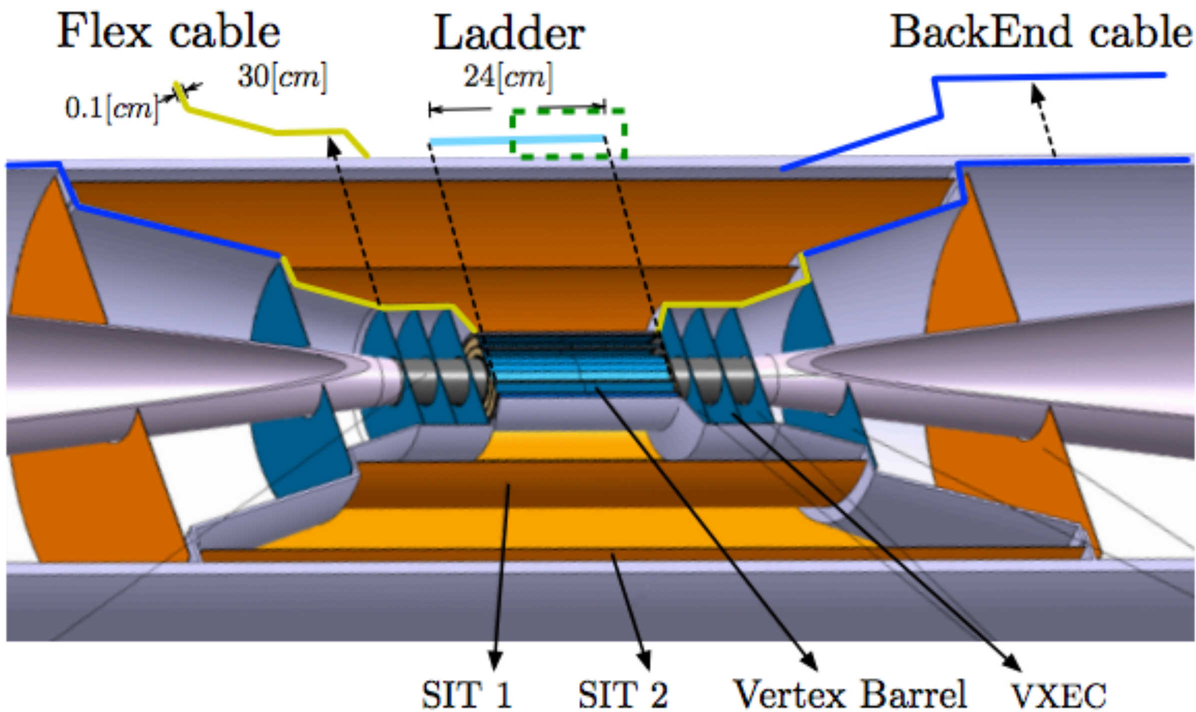
→ sub bunch-crossing time stamp for ILC

→ further performance improvement needed for CLIC (~10 ns time stamping)





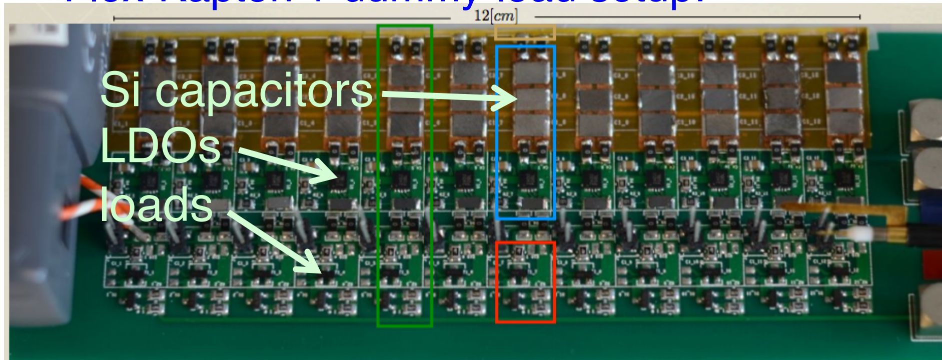
Power-pulsing and power-delivery

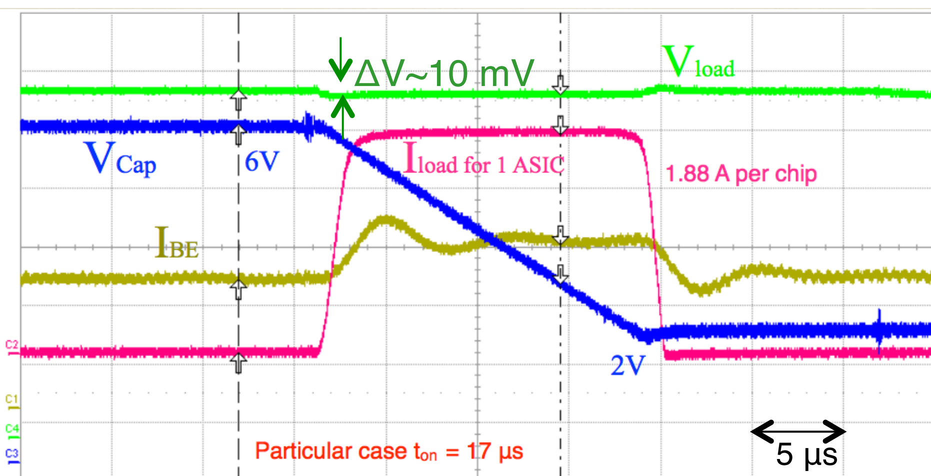


Power-delivery + pulsing

- low-mass Al-Kapton cables
- power pulsing with local energy storage and voltage regulation
- prototype for analog powering of CLICpix ladder:
  - I_{ladder}~20-60 mA; 10 mW/cm^2
  - voltage stability: ΔV~10 mV
  - 0.064% X_0 material contrib.
  - can be reduced to ~0.03% X_0

Flex-Kapton + dummy-load setup:





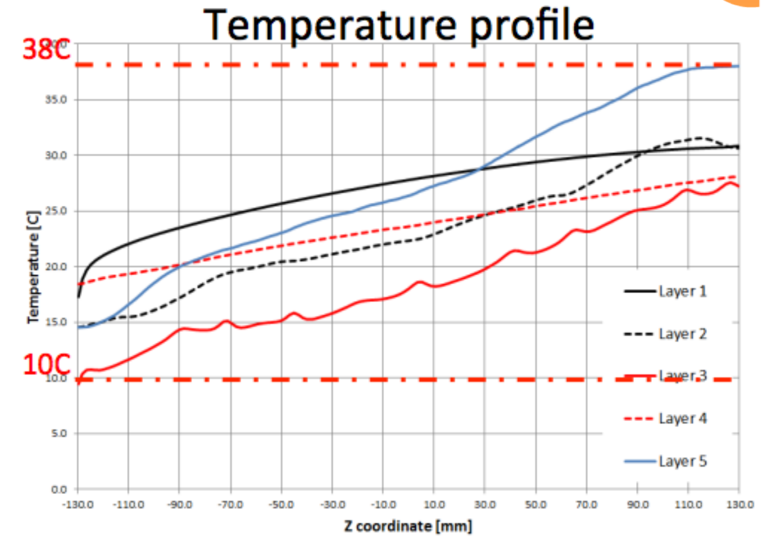
Cooling and mechanical integration

Cooling studies for CLIC vertex detector

- ~500 W power dissipation in CLIC vertex area
- spiral disks allow air flow through detector
- ANSYS finite element simulation

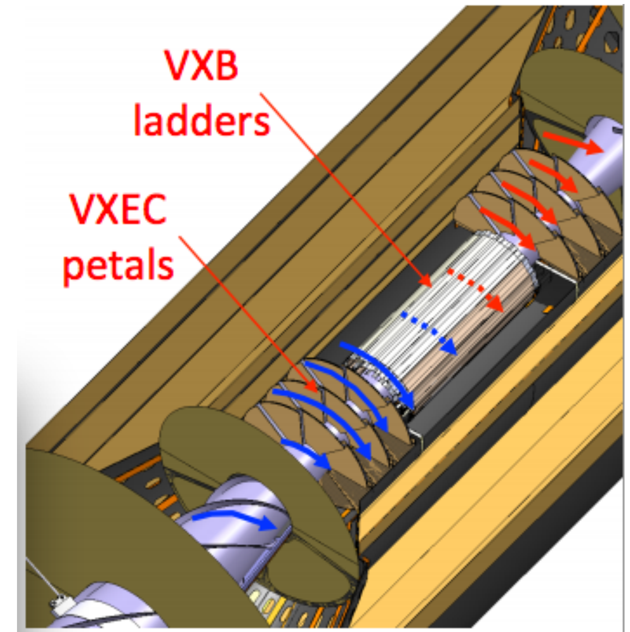
→ air cooling seems feasible!

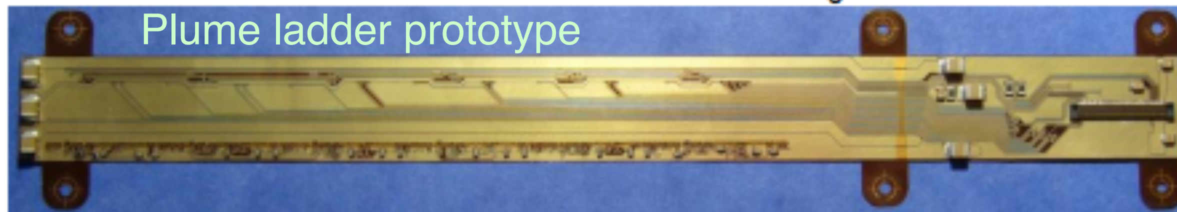
- ~10 m/s flow velocity, 20 g/s mass flow
- simulations to be validated in mock-up (temperature, vibrations)



Low-mass ladder design for ILD

- PLUME collaboration:
  - double-sided ladders with MIMOSA detectors
  - achieved $0.6\%X_0$ / ladder
  - new version with $0.35\%X_0$ in production





Summary

- machine environment + physics requirements at linear colliders pose challenging demands on vertex-detector systems
- detector concepts under development to meet those demands
- examples for active R&D on:
  - sensors + readout:
    - ILC: mainly fully integrated technologies
    - CLIC: hybrid or 3D technologies with fast time stamping
  - power delivery / power pulsing
  - cooling and mechanical integration
- synergy with other detector development projects

more details: ECFA Linear Collider Workshop 2013 VTX+TRK session

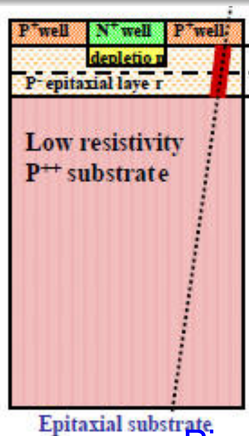
https://ilcagenda.linearcollider.org/sessionDisplay.py?sessionId=9&confId=5840

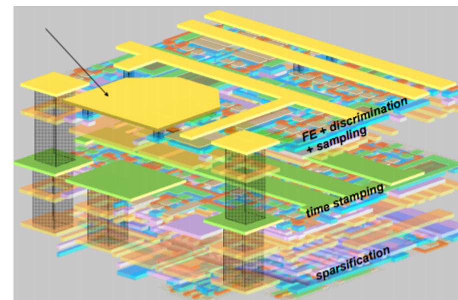
Thank you to the MIMOSA, FPCCD, DEPFET, HVCMOS, Chronopix , 3D and PLUME groups!

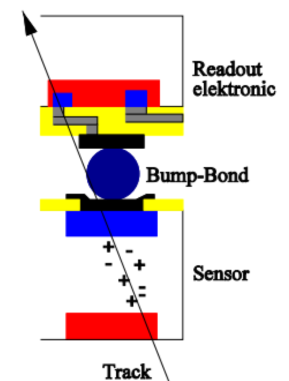
Additional material

Pixel-detector technologies

	Monolithic CMOS	3D-integrated	Hybrid pixel
Examples	DEPFET, FPCCD, MAPS, HV-CMOS	SOI, MIT-LL, Tezzaron, Ziptronix	Timepix3/CLICpix
Technology	Specialised HEP processes, r/o and sensors integrated	Customized niche industry processes, high density interconnects btw. tiers	Industry standard processes for readout; depleted high-res. planar or 3D sensors
Interconnect	Not needed	SLID, Micro bump bonding, Cu pillars	
granularity	down to 5 µm pixel size		~25 µm pixel size
Material budget	~50 µm total thickness achieveable		~50 µm sensor + ~50 µm r/o
Depletion layer	partial	partial or full	full → large+fast signals
timing	Coarse (integrating sensor)	Coarse or fast, depending on implementation	Fast sparsified readout, ~ns time slicing possible
R&D examples	ILC, ALICE, RHIC	ILC, HL-LHC	CLIC, ATLAS-IBL, HL-LHC

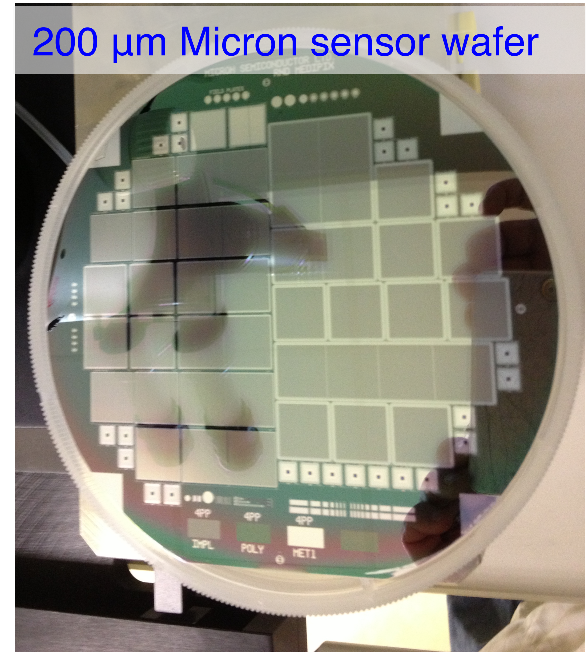


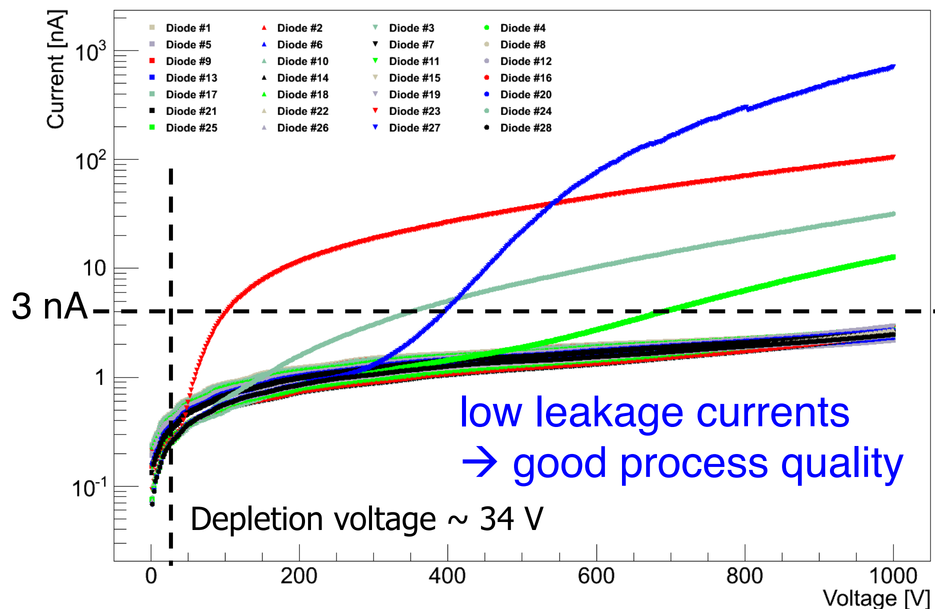


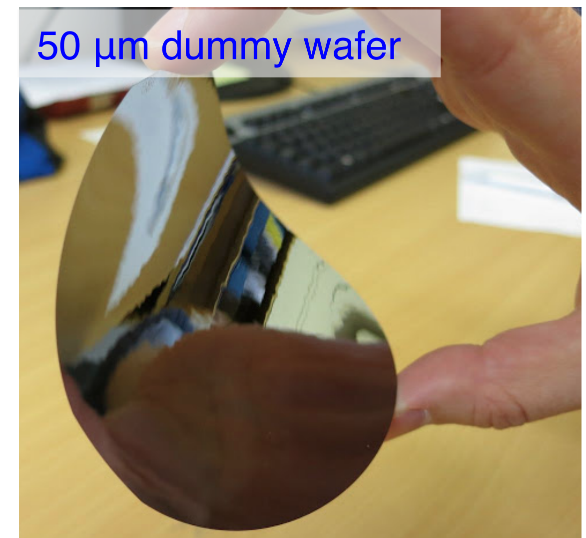


Hybrid r/o technology: thin sensors

- wafer production at Micron: sensors with 55 µm² Timepix footprint
  - Demonstrate feasibility of ultra-thin sensors and assemblies
  - Sensors delivered: 100, 150, 200, and 300 µm thickness
  - electrical characterization of sensor wafers
  - Test beams with Timepix assemblies in August 2013
- sensors matching 25 µm² CLICpix footprint (end 2013)
- mechanical tests with 50 µm dummy sensors
- ultimate goal: 50 µm thick sensors + 50 µm thick ASICs
- low-mass interconnects (TSV, µ bump + Cu pillar bonding)







Medipix/Timepix hybrid r/o chip family

Chip	Year	Process	Pitch [μm^2]	Pixel operation modes	r/o mode	Main applications
Timepix	2006	250 nm IBM CMOS	55x55	∫TOT or ToA or γ counting	Sequential (full frame)	HEP (TPC)
Medipix3RX	2012	130 nm IBM CMOS	55x55	γ counting	Sequential (full frame)	Medical
Timepix3	2013	130 nm IBM CMOS	55x55	TOT + ToA, γ counting + ∫TOT	Data driven	HEP, Medical
Smallpix	2013	130 nm IBM CMOS	~40x40	TOT + ToA, γ counting + ∫TOT	Sequential (data comp.)	HEP, Medical
CLICpix demonstrator	2013	65 nm TSMC	25x25	TOT + ToA	Sequential (data comp.)	Test chip with 64x64 pixel matrix
CLICpix	tbd	65 nm	25x25	TOT + ToA	Sequential (data comp.)	CLIC vertex detector

TOT: Time-Over-Threshold
→ Energy
ToA: Time-of-Arrival
→ Time stamping

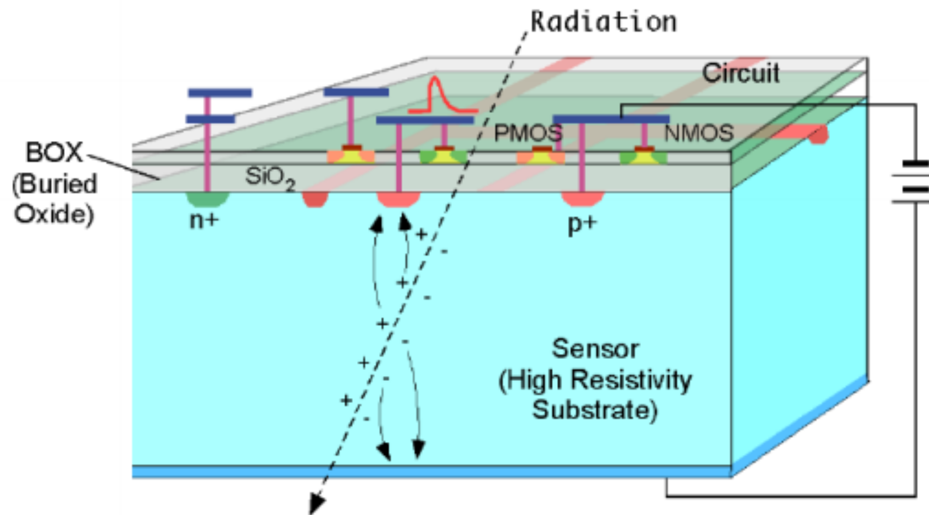
- Taking advantage of smaller feature sizes:
  - Increased functionality and/or
  - Reduced pixel size
  - Improved noise performance

3D r/o technology: SOI

Silicon On Insulator (SOI) technology

- CMOS sensor on SOI wafers
- Fully depleted High-Resistivity sensor
- Electronics on low resistivity wafer separated by BOX from sensing layer
- Allows for standard CMOS electronics
- Fast time stamping possible
- Complex pixel functionality
- Insulation from bulk

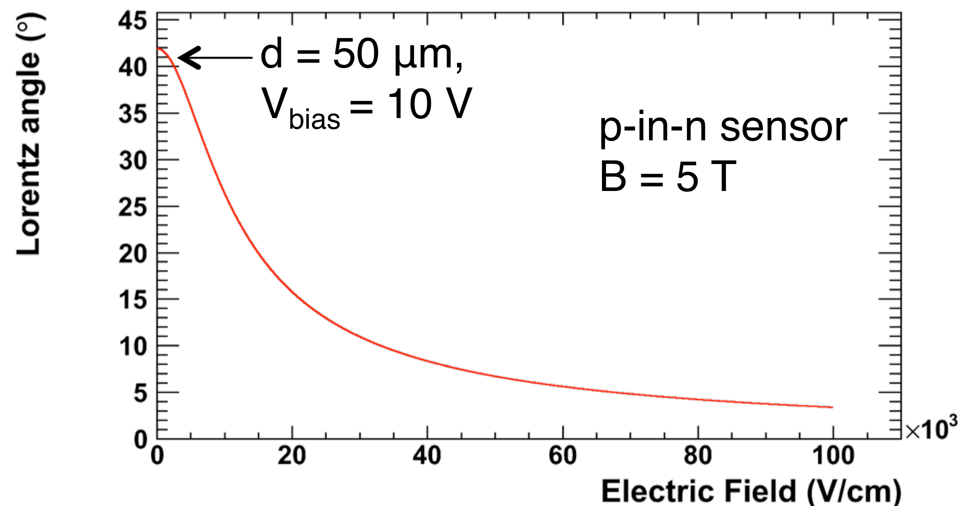
→low leakage current operation



Silicon device simulation with TCAD

Example:
Hybrid detector with Timepix readout

p-in-n sensor (10 kΩcm)
50 μm thickness → V_{dep}~1 V
55 μm readout pitch
V_{bias}=10 V → E~2000 V/cm
Magnetic field: 5 T
→ θ_L~40°



- Spread of charge cloud due to Lorentz-angle effect
- Effect more pronounced for e^-
- Can be partially compensated by rotation of sensors with Lorentz angle
- Over-depletion reduces effect

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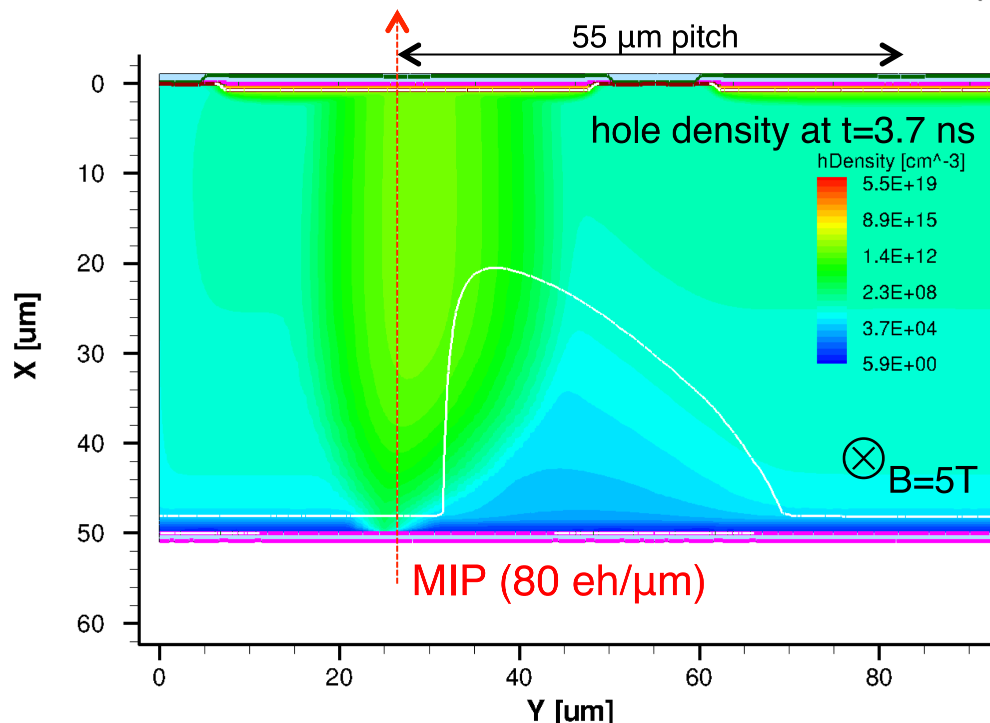


Signal rise time

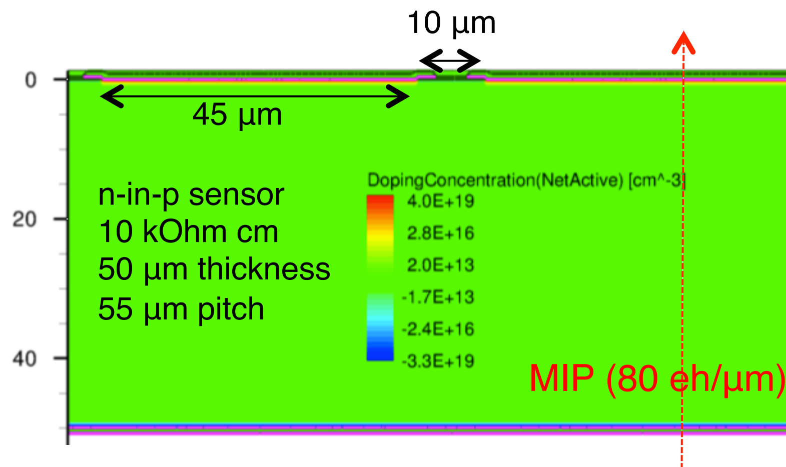
- Need time-stamping precision of ~10 ns, to suppress beam-induced backgrounds

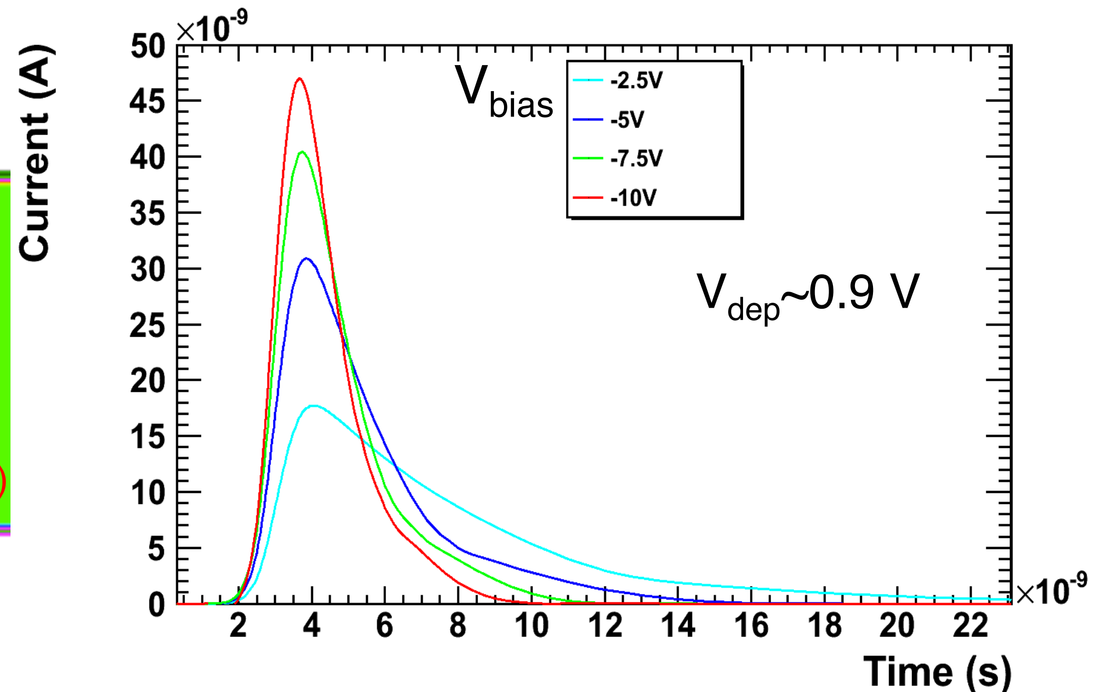
→ Peaking time in sensor should be <<10 ns, to optimize S/N and reduce effect of time walk

- electron collection faster than holes → favors n-in-p sensors

Example:

- 55 x 55 μm² pixels
- 50 μm thinned n-in-p sensor, ρ=10 kOhm cm
- ~2 ns peaking time with weak dependence on V_{bias}
- For higher V_{bias} better S/N expected after shaping, due to higher peak value; also less time walk due to reduced dispersion





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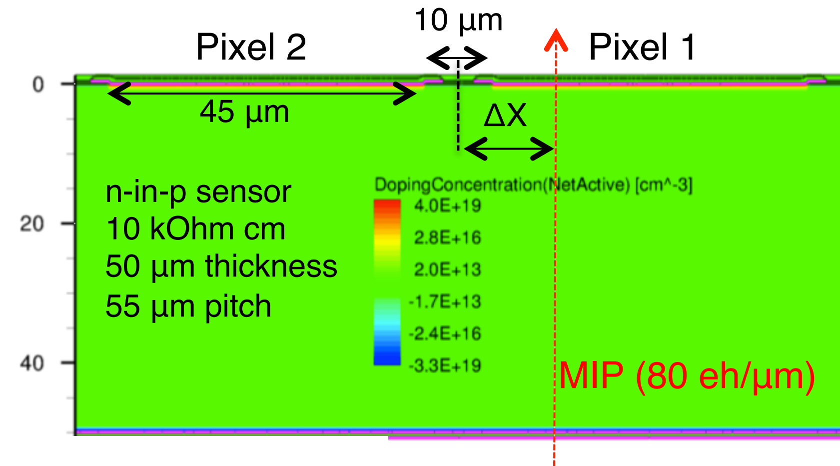
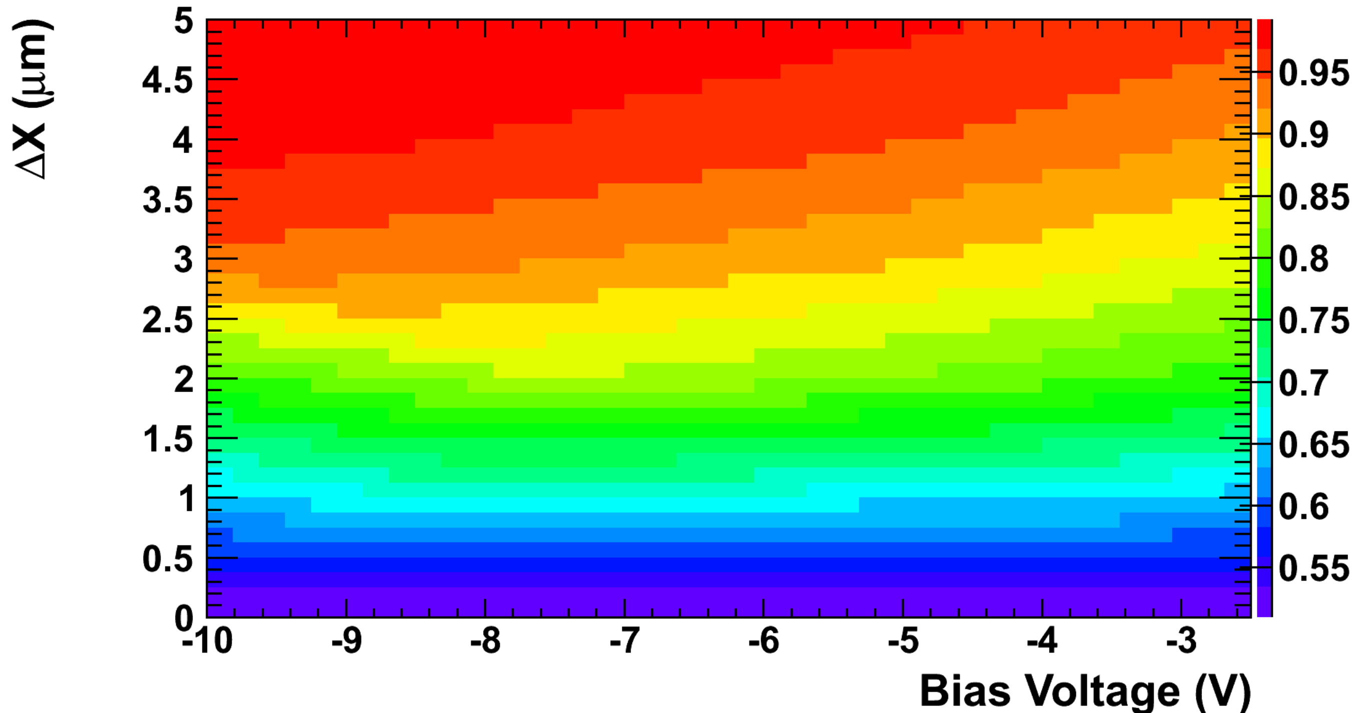
Charge sharing

- Charge spread in sensor leads to sharing of charge between neighboring pixels
- Over-depletion increases E-field, thereby reduces charge spread and charge sharing
- Charge sharing can improve resolution through interpolation (with analog readout)
- However: signals below threshold are lost





Fraction of total signal collected in pixel 1

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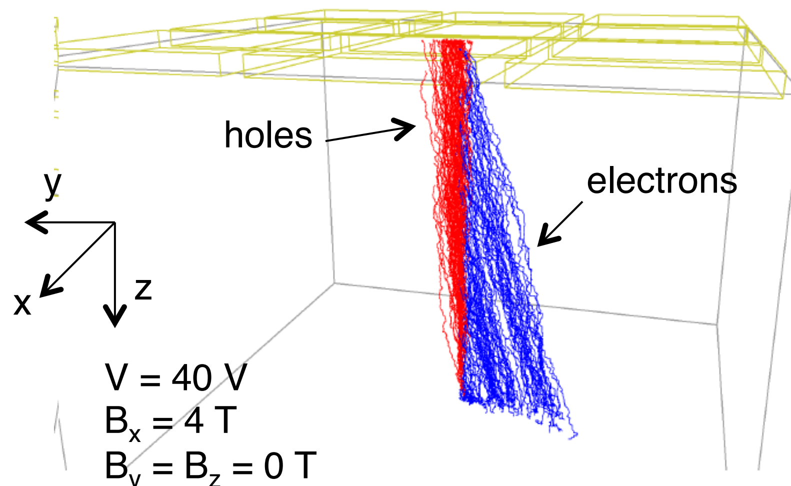
Monte-Carlo simulation of Charge Transport

- Simulate carrier drift in E+B field
- E-field from TCAD (previous slide)
- Takes into accout diffusion, mobility, trapping, repulsion

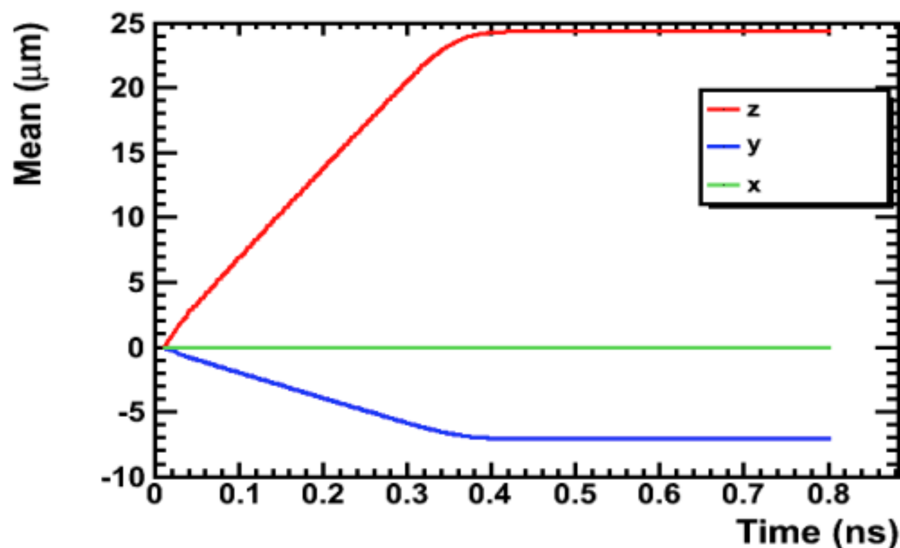
- Validation and simulation tuning in CERN SPS test-beam campaign (Timepix-based hybrid planar pixel sensor)

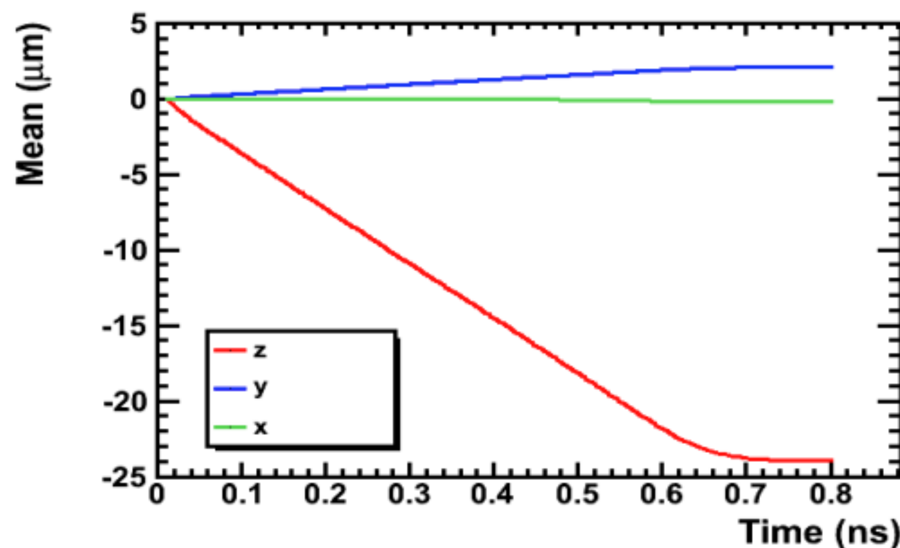
- Results will be implemented in Geant4-based full-detector simulation frameworks

Carrier drift in 50 μm thick fully depleted sensor:



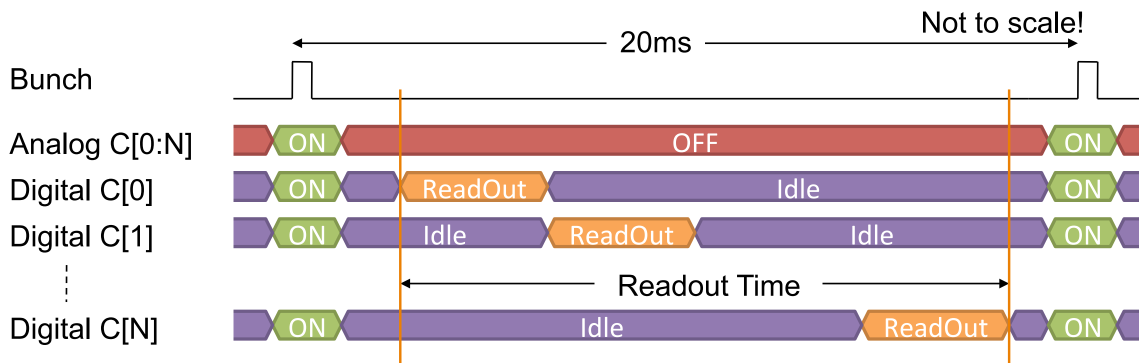
M. Benoit





CLICPix power-pulsing requirements

- Overall power budget (driven by air-flow cooling): P_{avg} ~ 50 mW / cm^2
- Estimation of power consumption for analog and digital blocks of CLICPix readout chip
- Based on measurements with 65 nm test-chip and projections from current Timepix
- Power pulsing with On/Idle/Off states, to reduce average power

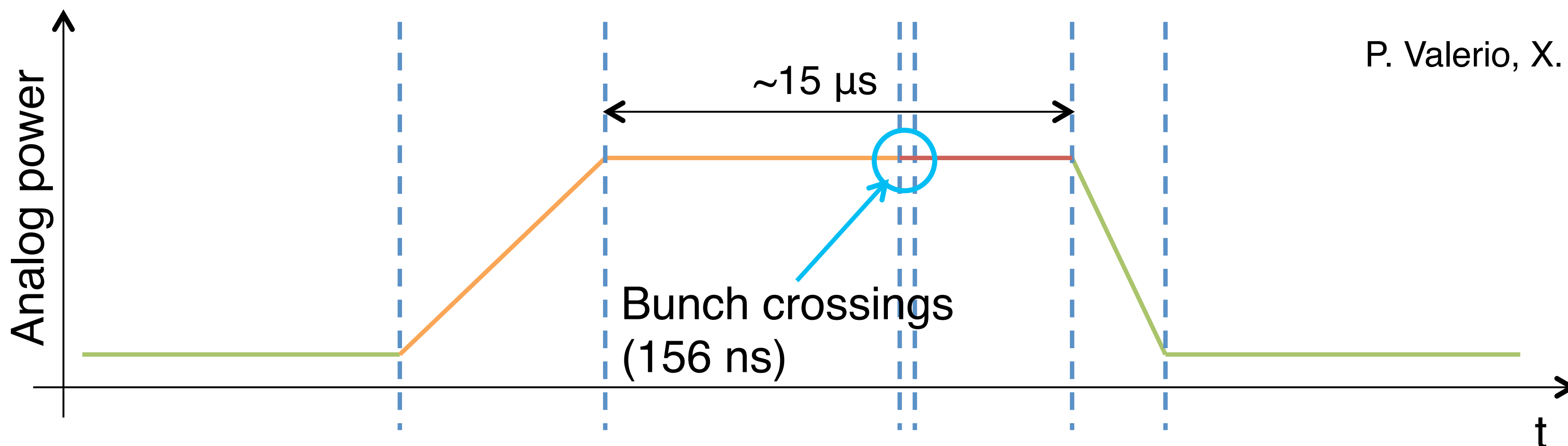


- Very small duty cycle for analog power
  → Favors local energy storage

Bunch Train (3.0 W/cm²)	
Pixel Analog	ON
Pixel Digital	ON
Periphery Analog	ON
Periphery Digital	ON
IO LVDS Pads	OFF

Chip Readout (360 mW/cm²)	
Pixel Analog	OFF
Pixel Digital	ON
Periphery Analog	OFF
Periphery Digital	ON
IO LVDS Pads	ON

Idle (7.8 mW/cm²)	
Pixel Analog	OFF
Pixel Digital	Idle
Periphery Analog	OFF
Periphery Digital	ON
IO LVDS Pads	OFF



P. Valerio, X. Llopart

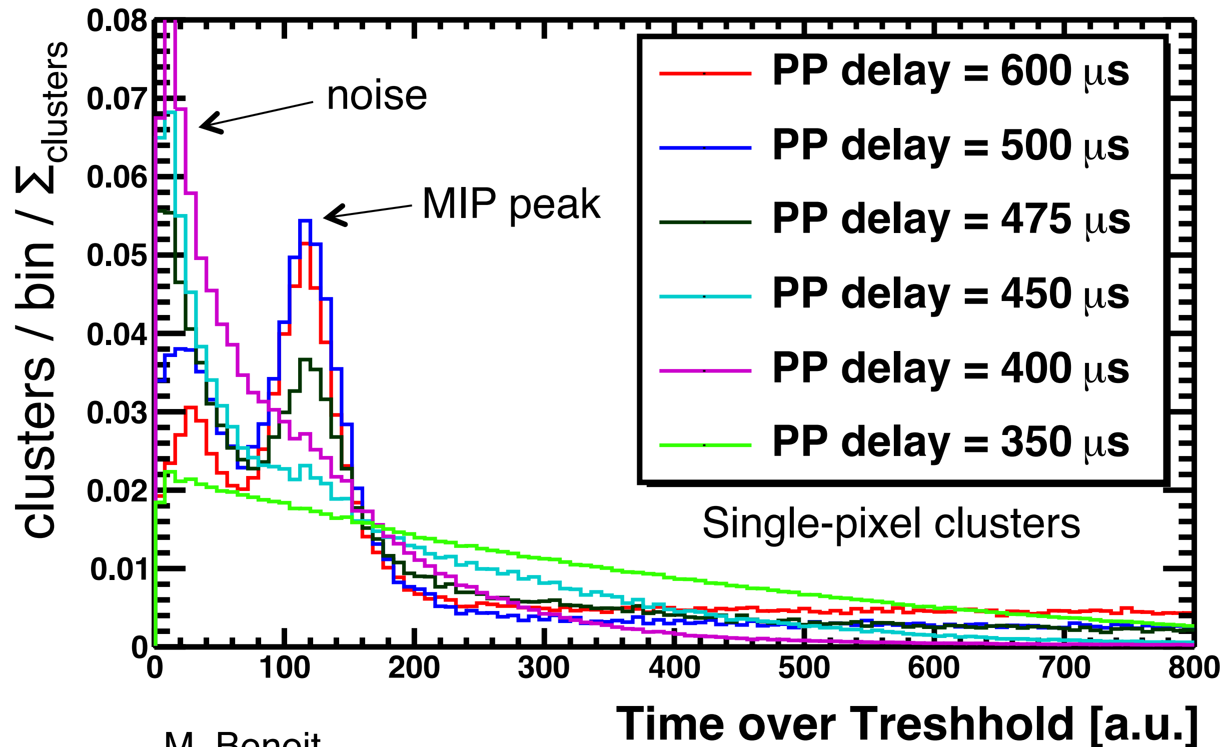
Power-pulsing in test beam

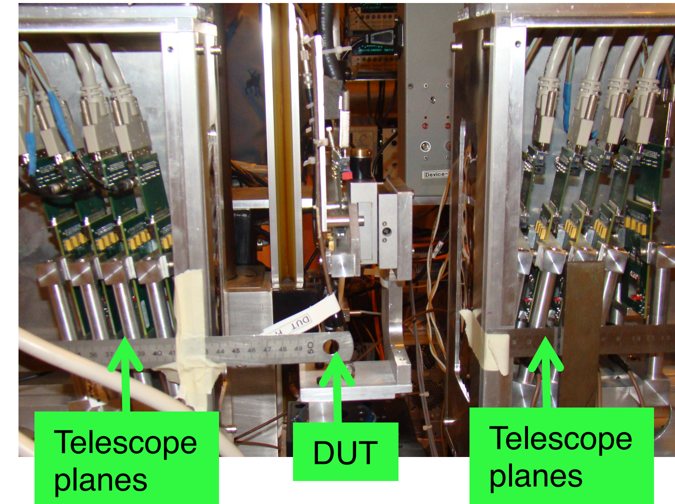
Power Pulsing with Timepix:

- Not designed for power pulsing, single bias line for all pixel rows
- But possibility to switch on/off all preamps through bias DAC

CERN SPS test-beam campaign in June 2012:

- Power pulsing of the Chip and operation in sync with LHCb/Timepix tracking telescope
- Shutter-based readout for 25 μs
- Adjustable delay between power-on and shutter-start times

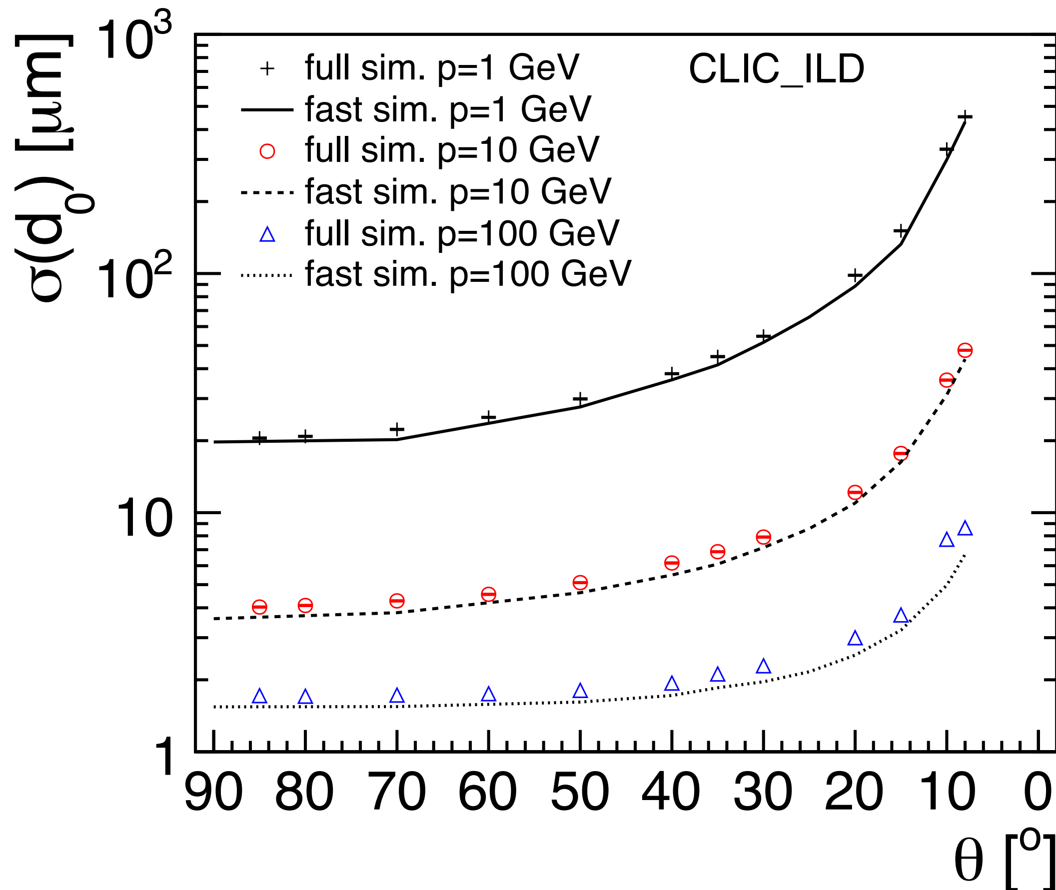




- Fully efficient after ~600 μs
- Similar results obtained with source in laboratory and in simulation

CLIC vertex-detector performance

d_0: distance of closest approach to interaction point in R-phi plane
→ d_0 resolution closely linked to heavy-flavor tagging performance
→ main benchmark parameter for vertex detector performance



- Simulation models reach required performance
- Sensitivity to changes in design parameters:
  - Single-point resolution
  - Distance to IP
  - Material budget

→ Parametric studies