TWEPP-08 Topical Workshop on Electronics for Particle Physics

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Book of Abstracts
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POSTERS SESSION / 101

14-bit and 2GS/s low-power digitizing boards for physics experiments

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The new Matacq14 board described in this paper has been designed to digitize 4 channels with 14 bits of resolution at 2 GS/s with an analog bandwidth of 345 MHz. It is not based on commercial ADCs which don’t reach these specifications, but on the low-power custom-designed analog circular memory called MATACQ. It can be triggered internally or externally, and several boards can easily be synchronized. It integrates USB, GPIB and 64-bit VME interfaces, permitting complying with most current acquisition systems. It can thus replace oscilloscopes for a lower cost in most applications where a much higher precision is needed.

**Summary:**

The trend in data acquisition systems for modern physics experiments is to digitize analog signals closer and closer to the detector. The digitization systems have followed the progress of commercial analog to digital converters. The state of the art for these devices is currently at the level of 500MHz for a 12-bit range. Faster ADCs, originally dedicated to military applications are also available, but their resolution is lower and they are much more expensive and power-consuming. Moreover, their packaging, cooling, and huge output data rates make them very difficult to implement.

The new Matacq14 board, described in this paper, has been designed to improve these performances by an order of magnitude. It houses 4 channels of 14-bit resolution digitizers sampling analog data in the range between 2 GS/s and 50MS/s with an analog bandwidth of 345 MHz. It is based on the custom-designed patented MATACQ chip that samples signal with a very high dynamic range in an analog circular memory of 2560 cells. Its innovative design permits reaching these performances, yet in an old fashioned pure CMOS technology, with a power consumption as small as 1W. Sampling precision is of the order of 15ps rms and trigger datation of 50ps rms. The boards can be triggered either by internal (individual threshold on inputs, auto-trigger, software trigger, ...) or external signals and several boards can easily be synchronized. An external clock can be used in order to synchronize the board with another system. The board integrates USB, GPIB and 64-bit VME interfaces which permits a maximum readout speed close to 1Kevent/s with the 4 channels read. Those various interfaces permit complying easily with most current acquisition systems. Several other read-out modes permitting reading only a limited set of cells or of channels are available for faster readout operation if necessary. Channels can also be grouped in order to extend the sampling depth (2 channels with 5120 of one channel with 10240 samples). A 1Mbit flash EEPROM permits storing all calibration and user data on-board. The usual power consumption is as low as 13W and remains below 20W even in the worst acquisition case. Because of its moderate cost and its design aimed at multi-channel operation, this board opens the fields of pulse shape discrimination, timing or charge measurement on very fast signals even in very high background environments. It can thus replace oscilloscopes for a lower cost in most applications where a much higher precision or a higher number of channels are needed.

Various evolutions of the MATACQ circular analog memory are under study, improving the sampling frequency, the sampling depth and the signal bandwidth. A patented continuous sampler will also be tested very soon. In parallel with high precision digitizing, those chips will open new doors into the domain of very high precision time measurements.

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Plenary Session 5 - Commissioning the LHC machine and interlocking with experiments / 151

3D IC Pixel Electronics, the next challenge

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Articles and advertisements related to 3D integrated circuits are now common in IC trade magazines. Numerous conferences and workshops are dedicated to developing the technologies needed for 3D ICs. Although HEP cannot drive the development of 3D technology, our community should be prepared to take advantage of the advances that are being made. In particular, there are new opportunities for pixel detectors in HEP that exploit the technologies being developed in industry for CMOS image sensors. This talk will present an overview of 3D technology, describe potential advantages for HEP, present results of the first 3D IC for HEP, and describe future plans in HEP to explore this technology. Looking to the future, 3D may be the next big challenge for HEP electronics designers.

**POSTERS SESSION / 111**

A GOL Based Optical Demo Link to Study System Issues for the ATLAS Inner Detector Readout Upgrade

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The GOL ASIC is a serializer chip developed by CERN based on 0.25 μm CMOS technology. The GOL operates with two data rates: 800 Mbps and 1.6 Gbps. This ASIC has been evaluated for the ATLAS Inner Detector readout upgrades for the SLHC. A demo link is being designed to read out test staves through fiber optics and study system issues in a giga-bit optical link. The results of the radiation evaluation and the demo-link will be reported.

**Summary:**

The GOL ASIC has been qualified and are used for detector readout systems in LHC experiments. We irradiated this ASIC with a 230 MeV proton beam for the ATLAS Inner Detector readout upgrade for the SLHC. TID effects were studied and SEE from the GOL was measured. Performance of the GOL before and after the irradiation tests was also compared. This is a part of an ATLAS R&D project for the SLHC. Based on the test results, we conclude that the GOL ASIC is suitable for the ATLAS Inner Detector readout upgrade for the SLHC.

Supported by US-ATLAS upgrade program, we are designing and constructing a GOL based optical demo link to read out the test stave through optical fiber. We intend to use this demo link to study optical link system level issues like the jitter in the link system, overall system reliability and the channel redundancy implementation, PCB area requirement and system power consumption, etc. In this demo link design, the GOL interface to the fiber is chosen to be the Versatile Link. A study about this interface is also needed. We will report the status and the latest test results with this demo link.

**Parallel session A1 - ASICs / 55**

A MAPS-based readout for Tera-Pixel electromagnetic calorimeter at the ILC

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The leading proposed technology for electromagnetic calorimeters for ILC detectors is a highly granular silicon-tungsten calorimeter. We have developed an active pixel sensor for such a calorimeter, which would have extremely fine granularity, allowing binary pixel readout. A first generation chip (TPAC1) has been fabricated, and this contains a 168x168 pixel array, consisting of 50x50 micron pixels. Each pixel has an integrated charge pre-amplifier and comparator. TPAC1 has been manufactured in the 0.18 micron CMOS INMAPS process which includes a deep p-well. We present recent results of the performance of the TPAC1 chip together with comparison to device-level simulations.

Summary:

The ILC physics program requires detectors with unprecedented jet energy resolution. To achieve this goal, the detectors will need highly granular calorimeters and, for the electromagnetic calorimeter, the use of a silicon-tungsten calorimeter has been favored. The granularity and readout requirements of such a calorimeter are closely interrelated. Detailed simulations show that a pixel size of 50x50 microns results in most pixels being only hit once per event. Thus we can employ a simple binary readout using a comparator instead of an analogue measurement. We have designed and fabricated such a CMOS Monolithic Active Pixel Sensor (MAPS) using a novel "INMAPS" process.

The first prototype chip (TPAC1) comprises 168x168 pixels with a total of over 8 million transistors. TPAC1 consists of 4 sub-arrays of 84x84 pixels implementing two distinct pixel architectures, with two variants of each. Each pixel contains four N-well diodes for charge collection, analogue front-end circuits for signal pulse shaping, a comparator for threshold discrimination, and digital logic for per-pixel threshold trim adjustment and pixel masking.

For readout, pixels are served by shared row-logic which stores the location and time-stamp of pixel hits in local SRAM, and was designed to target the 189 ns beam bunch crossing rate of the ILC. The sparse hit data are read out from the columns of logic in the quiet time between bunch trains.

The INMAPS process is a standard 0.18 micron CMOS image-sensor technology but includes a high energy deep p-well implant. A conventional MAPS design will allow charge absorption by any PMOS active devices in the pixel. Hence, the signal charge is shared between the N-well collection diodes and the rest of the circuit, dramatically reducing the efficiency of the pixel. By implanting the deep p-well in the regions of the pixel containing the PMOS active devices, charge deposited in the epitaxial layer is reflected and conserved for collection only at the exposed N-well collection diodes.

The charge collection performance of pixel test structures on the chip has been evaluated using a focused IR laser and clearly demonstrates the improvement achieved by the deep p-well implant. These results will be compared with device simulations. The performance of the main sensor pixels has been evaluated in terms of gain, noise and pixel uniformity. A Fe55 radioactive source is used to calibrate the pixel gain, and the laser is used to evaluate per-pixel gain uniformity. Further tests include cosmic rays, and alpha and beta radioactive sources. The status of the project, including latest results on the sensor performance, will be reported.

This is an exciting CMOS technology that offers a competitive alternative to the challenges of large-scale silicon detector systems both in performance and cost. The INMAPS process which has been developed under this program would also be applicable to a wide range of other applications.

Parallel session A1 - ASICs / 129
A Pixel Read-Out Architecture for the NA62 Gigatracker with on Pixel Time-To-Digital Conversion and Data Derandomization.

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The NA62 experiment will need hybrid pixel sensors with a size of 300 um x 300 um and a time resolution of 150 ps (rms). To meet the timing requirement an adequate strategy to compensate the discriminator time-walk must be implemented and an R&D effort investigating two different options is ongoing. In this presentation we describe the two different approaches. One is based on the use of a constant-fraction discriminator followed by an on-pixel TDC. The other one is based on the use of a Time-over-Threshold circuit followed by a TDC shared by a group of pixels.

The global architectures of both the front-end ASIC will be discussed.

Summary:

The aim of the proposed NA62 experiment at the CERN SPS is to study the very rare decay of the charged K meson into a pion and neutrino-antineutrino. One of the key components of NA62 will be the Gigatracker, which consists of three matrices of Si-pixel stations, each covering a sensitive area of 60 mm x 27 mm. The silicon sensor will be read-out by 10 front-end ASICs, each one with 45x40 read-out cells.

The Gigatracker should measure the particle trajectory with a space resolution of 100 um and a timing accuracy of 150 ps (rms). The latter is an unusual requirement for a traditional pixel detector and none of the existing systems has such a capability.

Two major issues has to be addressed to achieve the required time resolution: the compensation of the discriminator time-walk and the time measurement with such an high density of channels. Time-walk problem can be addressed either via a constant fraction discriminator (CFD) or a Time-over-Threshold (ToT) correction. While the first approach requires only one measurement per hit, it poses more challenges on the design of the comparator. The issue of precise time resolution with an high readout channel density can be dealt either with a per pixel, Time-to-Amplitude Converter based TDC or via a bank of DLL-based TDCs shared among pixels.

The TAC-based TDC solution requires more circuitry on the pixel area, thus potentially creating noise problems. Moreover, the pixel area will receive an high radiation dose and therefore it has to be designed in order to be radiation-tolerant in both total dose and SEU aspects.

On the other hand, the DLL-based TDC has to be much faster in order to keep the dead time under control because the TDC is shared among pixels. Ambiguities can arise if two pixels which belong to the same TDC are hit at the same time. Moreover, the TDC bank has to be placed at the end of the pixel column and therefore the signal carrying the time information has to be transmitted over a well calibrated transmission line in order not to degrade the timing information.

Preliminary investigations did not give a clear advantage of one solution over the others, therefore two prototypes will be designed in order to have an experimental comparison of the performances.

Parallel session A1 - ASICs / 104

A Pixel readout architecture for the NA62 Gigatracker based on End Of Column TDC

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We present the ASIC development of the readout electronics of the Gigatracker pixel detector of NA62. Gigatracker speed, noise and power performance are very challenging and 2 architectures,
are in phase of R&D demonstration to further select the best approach. Circuits configuration of the constant fraction discriminator with on pixel TDC and of the time-over-threshold discriminator with end-of-column DLL based TDC are presented and discussed. Spice simulations and layouts of the demonstrator circuits developed in 130 nm CMOS technology are presented and discussed.

Summary:
The NA62 Gigatracker pixel ASIC comprizes an array of 1800 pixel of 300 μm each and an End of Column logic on the periphery of the ASIC. The pixel array is structured into 40 columns of 45 pixel cells. The pixel circuit comprizes an ultra fast preamplifier and discriminator followed by a differential line driver designed to minimize both digital signal activity and power consumption. The End of Column logic comprizes differential line receivers, banks of TDC’s and readout FIFO’s that performs derandomisation and data pipeline before to send data off chip.

We present the design aspects of this challenging ASIC architecture, in particular design solutions that have been used to implement subnanosecond circuit in a low power architecture, and the integration of array of TDC’s in a front end ASIC, to date the first one implemented.

POSTERS SESSION / 51

A Prototype of Low Voltage Power Supply Using Piezoelectric Transformer

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A prototype of the low voltage power supply is implemented with a piezoelectric transformer provided by Tokin Corporation lately, where the piezoelectric transformer realizes ground isolation between the primary and the secondary. The low voltage power supply, integrating the piezoelectric transformer, produces the regulated output voltage of 1.5 V from the supply voltage around 48 V.

A carrier drives the piezoelectric transformer where the carrier is generated by a full bridge of FETs operated in a phase shift mode. The full-bridge phase shift switching realizes flexible control over the frequency and the amplitude of the carrier. The carrier is converted in amplitude by the transformer, and then rectified to be the output voltage of the power supply, which is fed back to the frequency and the amplitude of the carrier. The response of the output voltage is improved by the feedback.

The output voltage is stabilized by feedback. A feedback loop includes error amplifiers, FETs and a control IC for the full-bridge phase-shift switching. The control IC includes the circuitry necessary for the feedback, generating gate drive signals for FETs. The error amplifier detects the deviation of the output voltage from a reference voltage, supplying error signals to the control IC, The error signal changes the timing of the gate drive signals, thus modifying the amplitude of the carrier. The error signal also changes the switching frequency of the control IC, thus shifting the frequency of the carrier.

Summary:
A prototype of the low voltage power supply using the piezoelectric transformer is implemented, where the piezoelectric transformer was provided by Tokin Corporation lately. The transformer realizes the ground isolation between the primary and the secondary. The prototype is used to validate stabilization learned from extensive simulation and theoretical investigation.

The low voltage power supply includes the piezoelectric transformer. The piezoelectric transformer includes an internal resonance circuit. A carrier drives the piezoelectric transformer. The carrier supplied at the input of the transformer is converted in amplitude at the output, with the input to output voltage ratio of the amplitude being an amplitude ratio that shows a resonance as a function of the driving
frequency: the frequency of the carrier. Voltage conversion at the transformer depends on the driving frequency. The dependence is utilized for stabilization.

The carrier driving the piezoelectric transformer is generated by a full bridge of FETs operated in a phase shift mode. The full-bridge phase shift switching realizes flexible control over the frequency and the amplitude of the carrier. Thus the switching drives the piezoelectric transformer at a good efficiency. The carrier outputted by the transformer is rectified by a full bridge of diodes, which produces the output voltage of the power supply. The output voltage of the power supply is fed back to the frequency and the amplitude of the carrier, by which the response of the output voltage is improved.

The output voltage is stabilized by feedback. A feedback loop includes error amplifiers, FETs and a control IC for the full-bridge phase-shift switching. The control IC includes the circuitry necessary for the feedback, generating gate drive signals for FETs. The error amplifier detects the deviation of the output voltage from a reference voltage, supplying error signals to the control IC. The error signal changes the timing of the gate drive signals, thus modifying the amplitude of the carrier. The error signal also changes the switching frequency of the control IC, thus shifting the frequency of the carrier.

The power supply has been extensively simulated. Simulation is run for all sorts of feedback under the various conditions. Yet the circuit of the power supply used in simulation is different from the real circuit of the power supply for several reasons. One of the reasons is that simulation consumes time. The real circuit is simplified to the simulation circuit so that the simulation time can be shortened. It may happen that difference between the real and the simulation circuits becomes an issue.

In the simulation circuit, the piezoelectric transformer is represented by its equivalent circuit. The error amplifier is approximated by an ideal amplifier with low pass filters. FETs and other components are found to be modeled in SPICE libraries. So the simulation circuit is composed of standard SPICE models except for the control IC. The control IC includes various functions necessary for the phase shift switching. In the simulation circuit, the control IC is implemented by a mathematical model partially because the simulation of the control IC is time-consuming.

The mathematical model is designed to be functionally equivalent to the control IC, which can be tested with the prototype. The mathematical model can be compared with the SPICE model of the control IC, which will be soon at hand. Stabilization of the feedback so far learned can be tested, and the theoretical investigation can be validated.

**POSTERS SESSION / 86**

**A Radiation Tolerant Current Reference Circuit in a standard 0.13um CMOS Technology.**

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A Current-summing Bandgap reference circuit, has been developed in a 0.13um CMOS technology. The reference current has low sensitivity to temperature and power supply variations. In the design we utilize only CMOS structures (instead of diodes) and poly-silicon resistors. The combination of the natural properties of the thin gate oxide MOS transistors with gate-all-around layout, results in a circuit having a very low susceptibility to ionizing radiation. The output current varies in the range \(\pm 0.9\%\) when the circuit is being irradiated up to dose of 200 Mrad.

**Summary:**

Integrated circuits with current comparators, A/D and D/A converters and bias circuits generally require reference currents with low sensitivity to temperature and power supply variations. For high-energy physics experiments an additional requirement is to deliver a stable current even when operating in ionizing radiation environments. With the ongoing CMOS evolution, the gate-oxide thickness steadily decreases, resulting in an increased radiation tolerance of the MOS transistors. This, combined with special layout techniques, yields to
circuits with a high inherent robustness against X-rays and other ionizing radiation. In bandgap voltage/current references, the dominant radiation susceptibility is then no longer associated with the MOS transistors, but is dominated by the diodes.

For this reason in the present design we excluded diodes and used instead new structures called dynamic-threshold MOS transistors (DTMOST). DTMOST is made of a standard p-channel MOST by means of tying the gate-, drain-, and bulk terminals together, whereas the source terminal is left open. This two-terminal device demonstrates an exponential (diode-like) current-to-voltage characteristic when the voltage is lower than 250mV. This feature enables us to consider the DTMOST as a “low-voltage diode” and use it instead of ordinary diodes in standard bandgap circuits [1].

The present design has origins in current-summing bandgap reference circuit proposed by Banba [2]. This circuit delivers a stable current which can be used as a reference for current mirrors or can be converted into a stable voltage, if necessary.

The present circuit has four outputs providing currents of 2.5μA, 7.5μA, 16.5μA and 30μA.

The most important specifications are:
1) Power supply voltage is 1.0V...1.3V.
2) Output current-to-power supply voltage sensitivity is 10ppm/mV
3) Output current-to-the temperature sensitivity is
   100ppm/ K (when trimmed) in the range from 0C to 40C
   600ppm/ K (when untrimmed) in the range from 0C to 80C
4) Channel-to-channel spread of the absolute value of the output current is 7%.
5) Variation of the output current caused by ionizing radiation up to dose of 200 Mrad is +-0.9%.


Parallel session A2 - ASICs / 61

A Readout ASIC for CZT and Si Detectors

Author(s): Lawrence Jones
Co-author(s): Ian Lazarus; Mark Prydderch; Patrick Coleman-Smith; Paul Seller

Spectrometers that can identify the energy of gamma radiation and determine the source isotope have until recently used low temperature semiconductors. These require cooling which makes their portability difficult. A relatively new material, cadmium zinc telluride, is now available which operates at room temperature and can be used to measure the energy of gamma radiation. In a Compton camera configuration the direction of the radiation can also be determined. A read-out ASIC has been developed which detects the ionised charge in such a system and processes this before outputting to a data acquisition system. ASIC test results will be presented.

Summary:

A portable gamma camera has been developed which can detect both the position and isotope of material emitting gamma radiation. As part of this, a layered and pixellated cadmium zinc telluride (CZT) detector has been designed. Battery powered, the detector requires low power, and low noise read-out electronics to detect and process the ionised charge before it can be developed into an image.

The read-out ASIC has 100 channels. A preamplifier detects the ionised charge and integrates this into a voltage, the rise time of which can be used as a measurement of the depth of the ionising event within the detector. A differentiator and comparator measure this rise time and store it for later read-out. The comparator is also used to generate a time stamp of when the event occurred. A CR-RC filter shapes the voltage into a pulse which is easily processed by a peak hold circuit. The resulting amplitude is proportional to the energy of the ionising event in the detector. A comparator with a user defined threshold selects the energy level above which data will be digitised and read out. For every event above
this energy, the chip converts the voltage held on the peak hold circuit into a 12 bit digital form, and reads this out together with the pixel address, time stamp, and rise time. Data from neighbouring pixels are also read out as part of the same event. The energy range for which the ASIC has been designed is 2MeV for CZT with 1keV resolution.

Read-out from the chip is 1 bit serial and data driven. The data transfer speed is 32MHz and a data packet consists of 34 bits. Consecutive data packets will be output without a break in the data.

Reference voltages and bias currents are internally generated to simplify external circuitry, and the user can modify the default settings using an I2C compatible interface which accesses the internal registers. The shaping is programmable between 500ns and 7.5us and the preamplifier has two gain settings optimised for CZT or Si detectors.

The ASIC has been designed and manufactured on an AMS 0.35μm process. Testing is ongoing and results will be presented.

**POSTERS SESSION / 90**

**A dual scale 1mW full flash ADC for the ILC vertex detector**

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The resolution needed in the CMOS sensors of the ILC vertex detector implies a digitization of each pixel by a small, 4-5 bits, dedicated ADC.

The ADC characteristics, given by the constraints of the pixel matrix and its read out are for one ADC per column: 10 MS, 25 micron width and about 1mW consumption, thank to the fact that this power could be turn off 99 % of the time.

To fit these requirements, several architectures were designed in different laboratories.

This paper describes the results of the LPC Clermont Ferrand R&D which is a two scale, 20 MS,1mW, 47 μm width, full flash ADC sharing two columns.

**Summary:**

The resolution needed in the CMOS sensors of the ILC vertex detector implies a digitization of each pixel by a small, 4-5 bits, dedicated ADC. The CMOS sensor chip MIMOSA designed at IPHC Strasbourg, is line column organized and read out column by column at 10MHz to avoid dead time. The pitch between columns is 20 to 30micron for a column number of several hundreds to thousand. The available area for the ADC is then 20 to 30micron width by 1.2 mm length.

The ADC characteristics, given by these constraints, are, for one ADC per column, 10 MS, 25micron width, and about 1mW consumption, thank to the fact that its power could be turn off 99 % of the time.

To fit these requirements, several architectures were designed in different laboratories. This paper describes the results of LPC Clermont Ferrand R&D which is a two scale full flash ADC.

First, the choice of the flash architecture for these particular features is discussed, and the concept of a non regular interval between comparators is introduced. Compare to the others architecture, the flash ADC exhibits the fastest response time, a poor differential linearity, a high number of comparators, and a high consumption. In the particular goal of pixel digitization, the fast response time is an advantage, and a good differential linearity is not mandatory at all.

**POSTERS SESSION / 91**
A front end chip for the INNOTEP project including a 8 bits, 100 MS ADC.

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This paper describes the front end electronic developed for the IN2P3 INNOTEP project by the pole microelectronic Rhone Auvergne. (Collaboration LPC Clermont Ferrand and IPNL Lyon).

This circuit handles the signals coming from LSO crystals through photo detectors (APD, PM...), and has to provide energy and time measurement, with medium accuracy (8 bits) for the energy but very high accuracy (500 ps at least) for the time.

The electronic consist of a high gain charge amplifier, a fast shaper and a pipeline ADC.

Two versions of charge amplifier and shaper were realized and tested, the ADC is under development, its first version should be send to foundry in June.

This ADC is 4 stages, 2.5 bits per stage pipeline, with open loop track and hold and amplifiers.

It is design in SiGe 0.35µm technology.

Summary:
The signals delivered by APD’s are very small: 20 to 50 fC, and must be amplified and shaped with small time constants to allow a good time measurement.
The charge amplifier is then design in the classical way: a common mode folded cascode with high gain and a small feedback capacitor of 500 fF.
The gain achieves is only 1.5 mV/fC, not big enough to be directly digitized.
To overcome this problem, an extra gain of 10 is added in the shaper itself, to obtain a signal of 700 mV, capable to drive an ADC.
The time constant of this shaper must be short (20 ns) to allow a good time measurement, and then needs a high gain, high bandwidth amplifier.
The architecture and measured performances of these two components, including a noise measure, are detailed and discussed.
The second part of the paper concerns the 100 MHz ADC.
The architecture chosen is a 4 stage pipeline.
This architecture needs 6 comparators per stage, a track and hold, a 3 bits DAC and an amplifier with a good accuracy and a gain of 4.
Each design is fully differential and open loop, to try to minimize the kick back noise and the stability problems.
The choice to handle the signal as a current instead as a voltage in the comparison and subtraction stage as well as in the DAC is discussed, and simulation results are given.

POSTERS SESSION / 47

A multi-channel 24.4 ps bin size Time-to-Digital Converter for HEP applications

Author(s): Christian Mester

Co-author(s): Christian Paillard; Paulo Moreira

1 CERN

A multi-channel time-tagging Time-to-Digital Converter (TDC) ASIC with a resolution of 24.4 ps (bin size) has been implemented and submitted for fabrication in a 130 nm CMOS technology. An on-chip PLL is used to generate an internal timing reference from an external 40 MHz clock source.
The circuit is based on a 32 element Delay Locked Loop (DLL) which performs the time interpolation.
The 32 channel architecture of the TDC is suitable for both triggered and non-triggered applications.
The prototype contains test structures such as a substrate noise generator. The paper describes the circuit architecture and its principles of operation.
Summary:

A 32 channel time-tagging Time-to-Digital Converter (TDC) ASIC with a resolution of 24.4 ps (bin size) has been implemented and submitted for fabrication in a 130 nm CMOS technology.

This chip is the successor of a High Performance TDC (HPTDC), which has been implemented in a commercial 250 nm technology achieving a resolution of 100 ps based on a Delay Locked Loop (DLL). The HPTDC is used in a variety of applications, with the largest one in terms of number of channels being the time of flight detector in the ALICE experiment at CERN. An RC delay line performs an additional interpolation in order to reach the required resolution of 25 ps at the cost of reducing the number of channels to 8, instead of 32. Contrary to a DLL, which is self-calibrating, RC delay lines need offline calibration. To implement 160 000 channels with 25 ps bin size, 20 000 HPTDCs are necessary, while the new development (TDC130) would require only 5 000 parts.

In the TDC130, an on-chip Phase Locked Loop (PLL) is used to generate an internal timing reference with a period of 780 ps from an external 40 MHz clock source. In order to further increase the resolution, a 32 element DLL performs the time interpolation. The prototype contains a PLL, a DLL, registers for event timestamps of the 32 channels and a band-gap voltage reference for biasing circuits. All channels share one common DLL time base in order to minimize the power consumption. The measurement is relative to the 40 MHz external clock and the bin size is a binary fraction of a 25 ns period, simplifying the encoding of the measurement. Furthermore, a programmable noise generator with an independent clock source is included in order to evaluate the sensitivity of the circuit to substrate and power supply noise. As the TDC130 is targeted at high energy physics (HEP) applications, it supports a high rate of measurements (3 MHz per channel). The maximum hit rate on one channel does not depend on the activity on other channels, as, contrary to the HPTDC, the level 1 buffers are not shared amongst multiple channels.

In order to reduce the bandwidth required for readout, a mechanism to store all measurements, but to read out only those that are considered interesting and signalled by a trigger signal, is implemented. This technique is frequently used in HEP applications. In other applications, a trigger system might not be available and thus all data needs to be extracted, a mode of operation also supported by the TDC130. The architecture is thus suitable both for triggered and non-triggered applications.

The paper describes the circuit architecture and its principles of operation. Depending on the fabrication schedule measurement results might be available at the time of the conference.

POSTERS SESSION / 24

A prototype ASIC buck converter for LHC upgrades

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Given the larger number of channels and the need for reduced material budget in the SLHC trackers, alternatives to the present power distribution scheme have to be explored. In this context we are envisaging a new architecture based on custom switching converters able to work in the high radiation and high magnetic field environment of the experiments. A prototype of the converter has been designed and integrated in an ASIC. This includes the fundamental building blocks of a buck converter that can be used in later and more complete designs and even in different topologies. Design techniques, functional and radiation tests of the prototype will be discussed.

Summary:

The number of channels in SLHC trackers will increase and the front-end (FE) circuits will probably require larger supply currents at lower voltage. Since the efficiency of the present power distribution
scheme is around 50% due to the power lost on cables, any increase in the supply current will dramatically affect the efficiency. It is therefore necessary to evaluate alternative power distribution schemes. A promising approach consists in the distribution of power through a higher voltage bus (up to 24V) to DC-DC converters positioned close to the FE electronics. These locally convert the bus voltage to the low voltage needed by the FE, reducing the current in the bus by a factor close to the voltage conversion ratio, hence decreasing the power lost in the cables.

Since the converters should be placed as close as possible to the FE electronics to reduce the high current path, they need to work properly in the harsh environment of the experiments characterized by high level of radiation (up to hundreds of Mrd) and intense magnetic field (up to 4T). These constraints make commercial switching converters, using ferromagnetic materials saturating well below 4T and not rated for reliable radiation hardness, unusable for this purpose.

In this context we are developing a custom inductor-based switching converter where tolerance to radiation and magnetic field are specifically addressed. Radiation tolerance up to 200Mrd has been demonstrated on custom-modified layouts (results presented in TWEPP 2007) for a high voltage 0.35 um CMOS technology usually employed in automotive applications. Magnetic tolerance can be achieved using air core inductors that avoid magnetic core saturation, although at the price of introducing constraints in the design of the converter.

In this contribution, we present a prototype converter that has been developed in the selected 0.35 um technology. The prototype includes the fundamental building blocks of a buck converter that can be used in later and more complete designs and in different converter topologies. It contains the two power switches and the control circuit.

The dimension of the two switches is optimized to reduce the switching and conductive losses as much as possible. The resistance of each switch is 165mOhm and the gate capacitance is 2nF. The control circuit allows the converter to supply a constant voltage to the load even if the load current is varying. This local regulation capability is a very attractive feature of the power distribution scheme using converters, since it allows for providing the FE electronics with the appropriate power at any time with minimum losses. The control circuit topology used in this design is the voltage mode control.

Our prototype needs some external components that will be integrated in a later version of the converter. This was done in order to have more freedom for testing purposes, as it enables to vary the switching frequency, the compensation network to stabilize the feedback loop, the input and load voltage and the load current.

Design techniques used for the stability of the feedback loop will be presented and layout specificities will be discussed. The prototype shall be delivered in July and functional and radiation tests will therefore be available for the workshop and will be presented.

**A small portable test system for the TileCal Digitizer system**

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The TileCal hadron calorimeter in the ATLAS detector contains about 2000 digitizer boards, developed and maintained by Stockholm University. A rather complex test system has until now been used to verify the functionality of the boards. However, it was built almost 10 years ago and is now in itself difficult to maintain since it consists of several already obsolete parts. The development of a new simple, reliable and portable test system that could survive the digitizers was therefore initiated. Its components have been chosen to reduce the problem with obsolescence and to allow easy migration to new platforms.

**Summary:**

The new system is based on commercially available components, for easy upgrade and service. It consists of a Xilinx development board (ML506), equipped with a Small Form-factor Pluggable (SFP) module for optical transmission and reception, and a laptop (optional). The system is communicating with the digitizers by transmitting TTC signals and receiving G-Link signals back through the same SFP module, utilising a single gigabit transceiver in the Virtex-V FPGA. The FPGA can easily be reconfigured for future upgrade and improvements, such as hardware acceleration for different kind of high-speed tests. It also contains an embedded CPU system running Linux and test software. The board is communicating
with a host computer over Ethernet. This computer, which is running the debug software, can therefore be located anywhere. If the system needs to be mobile a laptop is preferable. The main debug software is running in a virtual environment for easy maintenance and compatibility. This system needs to function during the next 10-15 years, as long as the digitizers needs to be maintained. It needs to be reliable and robust. However, some hardware may have to be replaced since they may not last that long. The development board could break down at some point. However, the board is commercially available and could easily be replaced with a new one without significant testing and debugging. If the board after some years for some reason would not be available, it could be replaced with a newer generation since the necessary part of the design is written in VHDL and could easily be implemented on a new FPGA. A newer board would most probably be better and still have all the required features. Generation of a new embedded system and a Linux system will most certainly be easier. The computer can not be expected to be in use for 15 years either. However, running the debug software in a virtual operating system makes it independent from the hardware and the operating system it is running on. Virtualization technology will be maintained in the future by software developers and will most certainly still be freely available. This eliminates the need for software maintenance from our side, by allowing us to stay with the old operating system on any new hardware.

The system could be used to test other systems as well in a similar way, requiring only some software development for the board. Even the hardware could be modified if other communication links than TTC and G-Link would be desired.

POSTERS SESSION / 5

ATLAS Level-1 Level-2 Trigger Integration Commissioning

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The ATLAS detector will be exposed to proton proton collision at the center of mass energy of 14 TeV with the bunch crossing rate of 40 MHz. In order to reduce this rate down to the level at which only interesting events will be fully reconstructed, a three-level trigger system has been designed. The level 1 (LVL1) trigger reduces the rate down to 75 kHz via the custom-built electronics. The Region of Interest Builder (RoIB) delivers the Region of Interest (RoI) records to the level 2 (LVL2) trigger which runs the selection algorithms with the commodity processors and brings the rate further down to ~3 kHz. Finally the Event Filter (EF) reduces the rate down to ~200 Hz for permanent storage. The LVL1, LVL2 systems will be overviewed. The commissioning in situ using almost full detectors, the full trigger system and the DAQ system will be discussed. Results on system functionality and performance based on the cosmic data will be presented. Some studies on system scalability and reliability will be shown with preselected simulated events running through the trigger and dataflow system.

Summary:

The ATLAS LVL1 system identifies the basic signatures of interesting physics with high efficiency algorithms executed via custom electronics, but based on detector data of coarse granularity. It consists of three components, the Calorimeter Trigger, the Muon Trigger and the Central Trigger. The Central Trigger includes the Central Trigger Processor (CTP) and the Muon-to-CTP-Interface (MUCTPI). The Calorimeter Trigger system forms electron/photon, tau/hadron, and jet multiplicities as well as global event energy information. The MUCTPI obtains muon candidate information from the barrel and endcap muon trigger chambers, then produces muon multiplicities for six configurable transverse momentum (pT) thresholds. Based on these local trigger objects the CTP makes the trigger decision (L1A) with a configurable trigger menu. The L1A signal is distributed to all subdetectors to initiate readout of the triggered event.

The ATLAS RoIB is a customized VME system. For each L1A it assembles RoI information identified at LVL1 into a full record and passes it to the Level 2 Supervisors (L2SV). L2SVs distribute the records to the LVL2 processing farm which runs the high level trigger (HLT) algorithms. A small fraction of the full event data is requested in fine granularity at this level and a decision to accept or reject is made. Events accepted by LVL2 are fully assembled and formatted in the Event Builder (EB) nodes. Subsequently the complex selection algorithms are executed on full events on the EF farms.
The LVL1 system is fully installed and the LVL2, DAQ systems are being deployed towards the final scale. Integrated commissioning is being performed by taking cosmics with partial muon detector and calorimeter. Cosmic data have been recorded in situ and analyzed. The results show all subsystems function as expected and the full hardware and software chain installed at the experiment site works in a coherent and consistent way.

Specific tests of the trigger and DAQ system are also being performed without detector, focusing on system scalability, reliability, behavior under stress and fault tolerance. The system is being tuned to the optimal state for the data taking, with the preselected simulated proton proton events running through the trigger and dataflow chains, including RoIB, LVL2, EB, EF and sometimes partial LVL1. The subsystem performance has been scrutinized. Some critical system quantities, such as the trigger rate and the event processing time, have been studied using different trigger algorithms as well as different dataflow configurations.

MICRO ELECTRONICS USER GROUP / 176

Access to ASIC Design Tools and Foundry Services at CERN

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POSTERS SESSION / 45

Achieving Best Performance with VME-based Data Acquisition Systems and 2eSST

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The double edge Source Synchronous Transfer (2eSST) is the fastest block transfer cycle offered by the VME64x standard. The maximum achievable data-rate foreseen by the protocol is 320 Mbyte/s. In this paper we present a reference design based on a FPGA for the reader willing to implement 2eSST in his VME64x application. By using this template, we have designed a custom Bit Error Rate Tester, in order to probe the block transfer reliability within and beyond the data rate limit presently set by the standard. Our results show that 800 Mbyte/s data transfers can be achieved in a 21 slots crate with a BER smaller than 10^-12.

Summary:

Since its appearance in the 80’s, the VMEbus played a leading role in the embedded computing, real-time control and data acquisition systems for High Energy Physics experiments. Nowadays, the original standard has undergone major improvements and new features have been added to its physical and logical layers. The double edge Source Synchronous Transfer (2eSST) is the fastest block transfer cycle offered by the VME64x standard. It consists of exchanging bursts of 64-bit words between the master and the slave without any handshake. The data sender validates words with rising and falling edges on a strobe line, thus achieving a Double Data Rate (DDR) transfer. In this protocol, the transfer rate is only limited by the timing skews of the data lines with respect to the strobe. Presently, the standard sets the transfer rate to 320 Mbyte/s.

In our paper we present a reference design to implement 2eSST in a FPGA-based VME board and we propose a general implementation and layout scheme. The nature of 2eSST suggests the deployment of FPGAs providing DDR input/output blocks, but our scheme applies even to older, non-DDR capable FPGAs. Our design implements a Bit Error Rate Tester (BERT) and we used it to perform Bit Error Rate (BER) tests on 2eSST transfers within and beyond the maximum data rate specification. We measured
BER, data timing jitter and eye diagrams with different bus load configurations and data patterns. Our measurements show that, on a 21 slots VME crate, it is possible to achieve reliable 2eSST transfers with rates up to 800 Mbyte/s, keeping the BER under $10^{-12}$.

The BERT has been conceived such that the user can use it as a starting point for the design of its own application. In this view, we also discuss the critical issues the user has to deal with in the design of a 2eSST interface both at FPGA and board levels.

Plenary Session 1 - OPENING / 143

An overview of the Experimental High Energy Activity in Greece

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On behalf of the Greek HEP Community

The major contributions of the Greek Experimental High Energy Community in both Accelerator and non-Accelerator experiments in the last decade will be presented. The strong points of the HEP scientific community will be stressed and an outlook for the future activities will be outlined with emphasis on carrying joint R&D projects and participating in future High Energy Physics Experiments.

Parallel session B1 - Trigger 1 / 39

Analysis of the initial performance of the ATLAS Level-1 Calorimeter Trigger

Adam Davis1; Alan Watson2; Alvin Tan2; Andrea Neusiedl3; Attilia Hidvegi4; Barbro Asman4; Birgit Oltmann1; Bruce Barnett1; Bruno Bauss1; Christian Bohm1; Christian Goringer1; Christian Olhm1; Christopher Curtis2; Damien Prieur1; David Charlton5; David Hadley2; David Sankey1; Eike-Erik Kluge5; Eric Eisenhandler6; Felix Muller1; Florian Pohlisch1; Frederik Ruhr2; Gilles Mahout5; Hans-Christian Schultz-Coulon5; Ian Brawn1; Johanna Fleckner3; John Morris6; Jürgen Thomas5; Juraj Bracinik2; Kambiz Mahboubi5; Karlheinz Meier5; Klaus Schmit1; Marius Johansen1; Mark Stockton7; Markus Bendel1; Martin Gallacher2; Martin Wessels3; Martin Wildt3; Mohammed Abarrouche7; Murrough Landon6; Neil Collins2; Norman Gee1; Paolo Adragna4; Paul Hanke5; Paul Thompson2; Pavel Weher2; Peter Faulkner2; Peter Watkins2; Rainer Stamen1; Ralf Achenbach2; Richard Booth1; Richard Staley2; Robin Middleton1; Sam Silverstein1; Sebastian Eckweiler3; Stefan Rieke3; Stefan Tapprogge3; Sten Hellman1; Stephen Hillier2; Taylor Childers5; Thorsten Kuhl1; Tony Gillman1; Torbjorn Moe1; Ulrich Schafer3; Victor Andrei3; Victor Lendermann5; Viraj Perera1; Weiming Qian1

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The ATLAS first-level calorimeter trigger is a hardware-based system designed to identify high-pT jets, electron/photon and tau candidates and to measure total and missing ET in the calorimeters. The installation of the full system of custom modules, crates and cables was completed in late 2007, but, even before the completion, it was being used as a trigger during ATLAS commissioning and integration. During 2008, the performance of the full system has been tuned during further commissioning and cosmic runs, leading to its use in initial LHC data taking. Results and analysis of the trigger performance in these runs will be presented.
Summary:

The ATLAS first-level calorimeter trigger (L1Calo) is a hardware-based system with a high degree of adaptability provided by widespread use of FPGAs. The real-time path of the trigger is subdivided into a Preprocessor, which takes analogue signals from the calorimeters and digitizes them, followed by two digital processor systems working in parallel: the Jet/Energy-sum processor and the Cluster Processor. It provides all the calorimeter based trigger information used by the Central Trigger Processor to make the final Level-1 trigger decision, and as such provides the majority of the individual inputs to this decision.

Along with the trigger decision path, L1Calo also provides read-out data and 'region-of-interest' (RoI) data on events accepted for further processing. The read-out data is used to monitor and understand the trigger decision, but the RoI data is used at a more fundamental level to guide the second level trigger. The correct operation of all these streams is necessary in order for ATLAS to be operational from the first day of LHC beam. Much of the functionality of the system can be verified via calorimeter calibration systems and rare high-energy cosmic events. However, the final tuning of timing and signal processing requires LHC beam with the correct beam-interaction timing.

The full system has been installed since the end of 2007, and has now been tested both stand-alone and in integrated runs with the rest of ATLAS over a long period. Even before the end of 2007, a partial system was being used to form triggers on high-energy cosmic events in ATLAS. During 2008, these integration and cosmic runs became increasingly sophisticated, allowing the correct performance of many aspects of the system to be thoroughly tested. Events with significant energy could be used to cross-check the trigger decision against the data read-out from the calorimeters themselves. The integration with the ATLAS data-acquisition and high level trigger systems could also be checked using this data.

It is hoped that LHC will start to produce beams during the summer of 2008. This will precipitate a great deal of analysis of beam and signal timing in order to optimize the performance of the calorimeter trigger. This will have to be executed quickly and efficiently to ensure that the trigger is properly timed for first collisions. When proton-proton collisions are achieved, it will then be necessary to measure the efficiency of the trigger and decide on suitable thresholds to maximize the potential for LHC physics.

The architecture of the L1Calo system will be presented, along with results from data taking in 2008, showing how the trigger achieved its goals in all areas – namely, calorimeter integration, algorithm implementation, trigger formation and RoI provision.

TOPICAL 1 - LHC Upgrades / 81

Architecture of the readout electronics for the ATLAS upgraded tracker

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The upgrade of luminosity of the LHC (SLHC) will necessitate changing the ATLAS tracker. The new fully silicon tracker will contain pixel layers, short-strip layers and long-strip layers. The silicon strip detector will be organized in staves or super-modules. The readout electronics will follow this organization and be based on front-end ICs, module controllers and super-module controllers. This presentation will describe the proposed readout architecture, the different options for powering the front-end electronics and for controlling the detector, as well as the on-going developments.

POSTERS SESSION / 40

CMS ECAL LV Control System performance
The CMS ECAL Low Voltage system is made of 136 WIENER MARATON power supplies, delivering about 250kW of power to the on-detector electronics. The system is controlled by the PVSS-based Detector Control System (DCS), which communicates with the MATATON local controllers via 11 CANbus branches. The stability of the 2.5V power, delivered to the Very-Front-End electronics is controlled by the DCU readout, accessible via DAQ - Control Token Ring chain. The setup parameters and the system status has to be read/stored from/to the Detector Configuration/Conditions data bases.

The overall control system performance, as well as the performance of each component will be analyzed. The timing and reliability of the Framework - PVSS-OPC server-Local controller chain will be presented. Connection to the DAQ for the DCU readout and status display will be discussed.

**Parallel Session A5 - Installation & Commissioning / 73**

**CMS Tracker Services: present status and potential for upgrade**

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A report is given on the completed programme of installation, connection and testing of the CMS Tracker services, culminating in the full checkout of the Tracker as an integrated system. Finally, in the context of future upgrades to the CMS Tracker, we report also on the potential capacity and constraints of re-using the current services.

**Summary:**

The CMS Tracker services, multitudes of pipes, cables, and fibres for cooling, power, control, readout as well as the thermal screen and alignment system have been installed and tested recently and are ready for operation.

During the period from March to November 2007, Prior to Tracker detector installation, all the services were laid from several off-detector locations up to the 32 PP1 patch panels, which are located just inside both ends of the CMS solenoid magnet at 16 different angular positions around the inside of the coil. Approximately 1000 pipes, 2300 electrical cables and 500 fibre optic cables, all 25m to 60 m in length, were installed and tested.

All of the services installation and testing work was done in a tightly managed, overlapping sequence that distributed the various activities over the whole of the CMS central barrel wheel YB0, managing to work in parallel with other CMS activities, including installation of ECAL and heavy lowering of the barrel wheels and endcaps of CMS. The pipes, cables and fibres were all inspected to check the correct routing and continuity tests were made to check for breaks. In addition, a sector of the Tracker cooling pipes were tested by passing coolant at -30C to check also the insulation of the pipes. Upon completion of the Tracker services to PP1 the Tracker was installed in December 2007.

Only one serious problem occurred during the installation of the services. A heat exchanger failure caused the loss (of half) of the Tracker cooling system and potential contamination with brine of the pipes to PP1. This problem has been solved but only after a long campaign of decontamination, repair and re-commissioning work, which has involved a change in the cooling fluid from brine to C6F14 in both Tracker cooling plants.

In the meantime connections and testing work continued. During the first 3 months of 2008 the Tracker connections were all made and tested in an intense period of activity. The pipes, fibres and cables were laid between the Tracker and PP1, followed by the respective connections at PP1 (and the Tracker bulkhead in some cases). The completed piping was pressure-tested to check for leaks; the optical fibres were tested again with an OTDR, now at the level of the full optical link. The measurements on the fibre system will be reported in a separate paper. The electrical connections were visually inspected.
with electrical testing integrated into the later system tests. These checks generated some minor repair work, after which the PP1 covers were put in place.

At this stage, the completed parts of the Tracker could be powered up and tested as an integrated system. At present 7% of the full Tracker system has been ‘checked-out’. This first part of the check-out used a temporary cooling plant and the procedure will accelerate once the final cooling plant becomes available. The results to date are that the tested fraction of the Tracker is fully functional, apart from one detector element in the Outer Barrel (TOB) which is connected to an irreparably broken optical fibre ribbon and a few other readout fibres which were already known to be broken inside the Tracker volume. As expected, a small number of fibre connections at PP1 or the backend have required re-cleaning. A basic test of the full control network of the Tracker was also possible since this required no cooling. After reordering of some swapped control cable connections, and re-cleaning of some fibre connections at the backend, the entire set of control ‘rings’ within the Tracker volume are now working.

Looking ahead to the distant future, it is foreseen that the CMS Tracker will be upgraded to a much more performant Tracker, most likely with many more detector channels. We must however consider the re-use of all the existing Tracker services laid between the backend and PP1. Apart from the optical fibres, which lie on top of all other services on YB0, all the Tracker pipes and electrical cables from PP1 to the back-end are situated under the cables of ECAL and HCAL which are expected to remain in place for the lifetime of CMS. There is little room remaining to lay new services for the Tracker to PP1 and the PP1 internal volume is almost fully utilised so we must try to re-use the existing cables and pipes. In addition, the fibre installation was a large and difficult task in itself and it would also be ideal to recycle also this part of the system. As a result, we now have some tight constraints on services available for the upgraded Tracker. These constraints will be reported in detail with reference to the various ongoing activities investigating how to make best use of the existing services for the upgrade.

POSTERS SESSION / 71

CMS Tracker, ECAL and Pixel Optical Cabling: Installation and Performance verification

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The installation of over 55000 optical links for the readout and control of the CMS Tracker, ECAL and Pixel detectors is now completed at CERN LHC Point 5. During the 2007 cabling campaign 672 optical cables that span between the experimental and service caverns were installed and tested. The connection to the optical, highly dense, patch-panels inside CMS followed in the first months of 2008. Within the quality control programme, an extensive test campaign was carried out in parallel in order to validate the cabling and connection process and feedback any improvements. In the end 99% of the failures were recovered and the Tracker, in particular, resulted with 0.13% of not working channels. For the Tracker, a verification of the optical link performance followed once the detector was powered-up and commissioned.

Summary:

The CMS optical cabling system for the readout and control of the ECAL Barrel, Tracker and Pixel sub-detectors comprises 55000 single pigtailed fibres, 4500 12-fiber fanouts and 672 multi-ribbon trunk cables (96 fibres each). The pigtails (no longer accessible during the cabling operations) are connected to the fanouts inside the sub-detector volume. From the edge of each sub-detector, the fanout tails have to reach the in-line patch panel (PP1, inside the CMS cryostat) where they connect to the cables. In a 6 week-long cabling campaign that started in October 2007 the pre-connectorized cables were pulled, laid and fixed one by one along the edges of CMS from PP1 to the back-end racks in the adjacent service cavern (about 60m distant). The procedure followed was the same for all the sub-detectors starting from the ECAL Barrel (108 cables distributed in 36 patch-panels) and continuing with the Tracker and Pixel (534 cables in 32 PP1).

During the installation the cables were systematically tested with a photon-counting Optical Time-Domain Reflectometer (OTDR) in order to verify the mechanical integrity of the fibres. In addition feedback was given to the cabling crews laying the cable in case any of the problems observed could be corrected by changing the cabling procedure.
It was important to maintain the testing-time to a minimum to ensure testing kept pace with the cabling to give the possibility to replace or repair a cable before it was no longer accessible. Thus the OTDR was equipped with a custom-developed optical splitter reducing the time of testing from 1 hour/cable (1 fibre at a time) to 20 min/cable (12 fibres at time).

In December 2007, after the cabling, the ECAL Barrel fanouts were connected at the patch-panels and the system measured again with the OTDR (test of the “full-links”) before the final connection at the back-end. A similar procedure was followed for the Tracker and Pixel which also required the fanouts to be routed along the 4m cable channel from the bulkhead to the patch-panels (for the Pixel a fanout extension was also required).

The quality control protocol, extensively practiced in the past years, required that 100% of the links be checked after the connection at PP1 to validate the quality of the fibre routing and connections as well as, in the Tracker case, to measure the overall optical link lengths needed later for synchronization. As an example, for the Tracker (completed in March 2008) 91 interventions were required to re-clean/re-mate defective connections and 20 to repair (with a fusion splice) broken ribbons. In the end only 12 channels were lost (non repairable) proving not only the good quality of the components but also the validity and robustness of the quality assurance programme.

For the Tracker, the procedure also includes a verification of the optical link performance when the system is powered on. In the initial phase, the cabling functionality is checked and this may require some troubleshooting, especially at the back-end connections since they were not checked in the previous tests. Subsequently the link calibration parameters (e.g. working point, gain) are measured also at different temperatures. The measurements of gain in particular can be compared with the expected values derived from the production tests in order to show that the link specifications have been met.

### Plenary Session 1 - OPENING / 145

**CMS in Greece**

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In this report the contribution of the Greek teams participating in CMS experiment is briefly presented. The contribution refers to the CMS Preshower, the CMS trigger/DAQ system, the CASTOR forward calorimeter, the CMS physics reconstruction and selection, and the preparation for Physics analysis.

### TOPICAL 1 - LHC Upgrades / 77

**CMS microstrip tracker readout at the SLHC**

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**Co-author(s):** Geoff Hall


The increased luminosity at the SLHC and associated increases in occupancy and radiation levels present severe challenges for the CMS tracker, which will require complete replacement. Inner pixelated regions will expand to higher radii and the outer tracker region will most likely be instrumented with short strip silicon sensors. It is also necessary for the tracker to provide information to the level 1 trigger.

Power consumption is one of the main challenges for the tracker readout system, because of the higher granularity. We will present the current status of readout chip development for a short strip outer tracker, with projections for performance and power consumption.

**Summary:**
The biggest challenge for tracker readout systems at the SLHC is power consumption and provision. Higher luminosity and therefore granularity means more front end chips. Advanced CMOS technologies will help, but power savings/chip will depend on functionality.

The current CMS strip tracker readout system is analogue, with no sparsification on-detector, utilising 0.25 μm CMOS technology throughout. The readout architecture at SLHC is not yet defined, but will certainly be different. Data transmission links at SLHC will be digital, taking advantage of commercial developments, so front end digitization is required if we decide to retain pulse height information. ADC power estimates indicate that this is possible, but only after a multiplexing stage. Zero-suppression may also be needed to reduce the transmitted data volume and maximise the ratio of FE chips to links, to minimize link power contribution.

0.13 μm CMOS technology will be used to develop readout circuits for SLHC. MPW (multi-project wafer) access to the technology is available, and has already been characterised for HEP applications. We need to begin mass production of readout chips several years before installation, so timescales dictate that prototype development must begin now.

Power provision is also a major challenge. Since 0.13 μm chips operate at half the supply voltage of 0.25 μm, the supply current increases even if the total SLHC tracker power remains the same as LHC, increasing power dissipated, and voltages dropped, in cables. Serial powering or on-detector DC-DC conversion will help, both of which have implications for FE chip design.

Front end specifications must be developed. A number of relevant sensor technology issues are yet to be decided, and are the subject of wider CMS tracker R&D. Aspects which are directly relevant to the readout chip development are:

- sensor signal polarity: n-side readout of p-substrate or vice-versa.
- sensor-FE chip coupling: DC coupling simplifies sensor design and reduces cost, but requires the front-end chip to sink or source leakage currents.
- sensor strip lengths and pitches: capacitance and leakage current, and hence noise, depend on length and pitch, requiring optimization of the amplifiers.

We report on the current status of developments for CMS short strip tracker readout at SLHC, giving predictions for performance and power consumption for electronic architectures matched to different sensor and readout choices.

### Plenary Session 6 - LHC upgrades: needs and reality / 152

**CO2 cooling for HEP experiments**

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The new generation silicon detectors in High Energy Physics (HEP) Experiments require more efficient cooling of the front-end electronics and the silicon sensors itself. To minimize reverse annealing, the silicon sensors must be cooled down to a temperature of about -5°C. Other important requirements of the new generation cooling systems are a low mass and a maintenance free operation of the hardware inside the detector.

Evaporative CO2 cooling systems are ideal for this purpose as they need smaller tubes than systems with Fluor Carbons. The heat transfer capability of evaporative CO2 is high and CO2 is radiation hard.

CO2 is used as cooling fluid for the LHCb-Velo and the AMS-Tracker cooling systems. A special method for the fluid circulation is developed at NIKHEF in order to get a very stable temperature of both detectors without any active components like valves or heaters inside the detector. This method is called 2-Phase Accumulator Controlled Loop (2PACL) and is a good candidate technology for the design of the future cooling systems for the Atlas and CMS upgrades.

In this paper the design and the test results of the LHCb-VELO CO2 cooling system are discussed and a comparison is made between the use of Fluor Carbons and CO2 in a typical HEP detector.
Characterization of the noise properties of DC to DC converters for the sLHC

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The upgrade of the LHC experiments sets new challenges for the powering of the detectors. One of the powering schemes under study is based on buck converters mounted on the front-end modules. The switching noise emitted by these converters is susceptible to affect the performance of the powered systems. A model to identify and to control the noise sources of the converter was developed. A reference test setup with associated measurement methods is used to characterize the noise properties of the converter. Complementary tools and simulations were also used to evaluate the noise couplings at system level.

Summary:

1. Introduction.

The experiments at the sLHC will be more demanding in terms of power and cabling than at the LHC, in particular for the trackers. The cabling constrains of the detectors, together with the thermal management and the overall power efficiency force the development of new radiation hard and magnetic field tolerant powering. One of the proposed powering schemes is based on an air core buck converter to be mounted on the front end modules of the trackers. The switching converter and its air core inductor will sit in the close vicinity of the front-end detectors and electronics. In order to achieve the appropriate noise performance of the front-end system, the noise properties of the converter need to be characterized and the way in which the noise interacts with the front-end electronics needs to be understood.

1. Modeling of the EMC properties.

The switched converter produces its noise in the form of common mode currents that are developed at the board level through stray capacitances at critical nodes. These nodes are identified and the magnitudes of the stray capacitances are estimated. The noise currents produced at these nodes depend strongly on the topology of the converter. Similarly, the air core inductor produces some leakage magnetic field in its vicinity, which can cause some near field inductive coupling to the front-end system. The magnitude of the coupling depends on the inductor topology and on the properties of the current that flows through it. With this, it is possible to determine the minimal distance between the inductor and the sensitive front-end areas.

1. Test setup.

The sample prototypes of the radiation hard converter need to be characterized in a standard manner that allows for objective comparisons of the noise properties. For this, a reference test setup is used. The test bench is built around line impedance stabilization networks (LISN) that normalize the common mode impedances over the entire noise frequency range. The noise currents are measured using calibrated current probes and a spectrum analyzer. The test setup is complemented with qualitative evaluation tools. Near field probes are used to identify hot spots of EMI sources on the samples. A near field scanning table is also used to produce a two dimensional image of the near field EMI emission of the sample boards.
1. Measurements.

Several samples of converters were modeled and measured on the reference test setup. The obtained results allowed identifying the topological aspects of the converters that could be implemented in the design of a custom, radiation hard and magnetic field tolerance buck converter for the trackers at the sLHC.

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Collaborational Effort on Radiation Tests (report from subgroup B)

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Commercial DC-DC

Parallel Session A6 - Trigger2 / 136

Commissioning of the ATLAS Level-1 Central Trigger system

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The ATLAS Level-1 Central Trigger (L1CT) consists of the Central Trigger Process (CTP) and the Muon to Central Trigger Processor Interface (MuCTPI). The CTP forms the final Level-1 Accept (L1A) decision based on the information received from the Level-1 Calorimeter Trigger system and from the muon trigger system through the MuCTPI. Additional inputs are provided for the forward detectors, the filled-bunch trigger, and the minimum-bias trigger scintillators. The CTP also receives timing signals from the LHC machine. It fans out the L1A together with timing and control signals to the Local Trigger Processor (LTP) of the sub-detectors. Via the same connections it receives the Busy signal to throttle the Level-1 generation. Upon generation of L1A the L1CT sends trigger summary information to the DAQ and Region-of-Interest to the Level-2 Trigger system.

In this contribution we will present an overview of the final L1CT trigger system as it is now installed in the ATLAS experiment and we will describe the current commissioning and integration activity at the experimental site. The system is now continuously used during cosmic-ray runs to exercise the full trigger chain and read-out of sub-detectors. These test are bridging the experiment towards the commissioning phase with protons in the LHC as it is foreseen for this summer. We will discuss in particular the results achieved in operating the system with cosmic-rays and, possibly, the commissioning results with the first proton events in the LHC.

POSTERS SESSION / 17
Commissioning of the SDD data concentrator card CARLOSrx

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The data concentrator card CARLOSrx is a readout board developed for the ALICE ITS Silicon Drift Detector (SDD) experiment held at CERN. CARLOSrx is a 9Ux400 mm VME board, containing 4 FPGAs with the purpose of processing data coming from 12 SDD detectors and sending them to a computer running the DATE software. We have 24 CARLOSrx installed at CERN, each CARLOSrx is able to receive data from 12 SDD detectors, so we are able to read the data produced by all the SDD detectors. This paper presents the results obtained during the runs performed at CERN.

Summary:
CARLOSrx is a 9U x 400 mm VME board used in the ALICE experiment to read data produced by SDD detectors.
24 CARLOSrx boards have been installed in 3 VME crates located in the counting room at CERN for ALICE experiment.
The most important tasks of CARLOSrx are to receive data from detectors and send them to a computer for future analysis, send clock and program all the front end electronics.
Each board receives data from 12 SDD modules through 12 optical fibers; the board also directly interfaces with the trigger system and the DAQ chain.
CARLOSrx is composed principally of 4 FPGAs (three of them process the data coming from detectors and one manages the VME bus interface) and 4 FIFOs (256 Kword x 32 bits) that buffer the information during the data taking.
We have installed all 24 CARLOSrx at CERN, ready to receive data from 260 SDD detectors, the complete barrel for the experiment ALICE ITS SDD.
The firmware loaded on CARLOSrx can be reprogrammed via VME using a commercial CPU VME.
We have also developed a software to generate different files for the JTAG configuration of the front end electronics. With this software tool we can easily produce different configuration files for each chip presents in the chain.
We had two Cosmic runs during December 2007 and February 2008 and during this period the boards were tested in different condition of work: constant, random and physics triggers.
For the first time we were able to test the functionality of the entire DAQ chain for SDD detectors inserted in the real setup of the ALICE experiment, with all the other detectors powered on and the system controlled by the ECS (Experiment Control System).
This paper present the latest development of the board and the results obtained during the cosmic runs.

POSTERS SESSION / 122

Commissioning the CMS silicon strip tracker

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The CMS silicon strip tracker is the largest device of its type ever built for the detection of charge particles produced in beam-beam collisions. There are 24244 single-sided micro-strip sensors covering an active area of over 200 square meters and nearly ten millions of readout channels. The sub-detector was installed inside CMS in December 2007. We report on detector performance studies from the commissioning phase, when the complete readout system was calibrated and synchronized for the first time, and on experiences from global cosmic runs with other sub-detectors of the CMS experiment.

Summary:
The CMS silicon strip tracker (SST) is unprecedented in terms of its size and complexity, providing a sensitive area of over 200 square meters and comprising ten million readout channels. The readout system is based around a 128-channel custom front-end ASIC known as the APV25 chip, an analogue optical link system and an off-detector Front-End Driver (FED) VME board that uses FPGA technology for much of its processing capabilities. 76000 APV25 chips sample, amplify, buffer and process signals from silicon strip sensors mounted on 15000 front-end modules at the LHC collision frequency of 40 MHz. On receipt of a Level-1 trigger, the APV25 chips transmit analogue pulse height data to 440 FEDs, which digitize, zero-suppress and format the data. The resulting event fragments are then transmitted to the CMS online computing farm, which hosts a software-based second-level trigger system.

Commissioning such a large-scale readout system requires sophisticated, automated procedures to bring the detector into an operational state that is suitable for physics data-taking. Examples of such procedures are: detection of the readout system connectivity and partitioning; internal synchronization of the front-end system (with a precision at the level of a nanosecond); latency scans to synchronize to the passage of charged-particle products of beam-beam collisions; pulse shape tuning of the APV25 amplification stages to achieve optimal signal-to-noise and minimize pile-up; and the determination of calibration constants used by the FEDs in order to zero-suppress the data. These procedures, amongst others, are used to tune, measure and monitor the operational performance of the sub-detector.

The strip tracker was installed inside the CMS experiment at Point 5 on the LHC accelerator ring in December 2007. Presently, “checkout” of the ~350 control rings within the strip tracker is underway, which focuses on identifying possible problems with the connectivity and services of the control, readout, monitoring and power supply systems. Once checkout is complete, the strip tracker will be commissioned as a complete entity and operated with the other sub-detectors of CMS during global cosmic runs. No results are yet available from commissioning at Point 5, but large-scale tests (comprising data-taking with 1.7 million channels of the completed strip tracker system) during the integration phase in the summer of 2007 demonstrated the high-quality construction of the strip tracker and excellent performance, with a dead/noisy channel count at the per mille level and a noise performance that compares favourably with the design specification.

We will report on results and experiences from the commissioning phase and global operations with the CMS experiment during cosmic runs, focusing on the performance aspects of the strip tracker readout system. First beam-beam collisions are expected in the latter part of 2008.

Plenary Session 5 - Commissioning the LHC machine and interlocking with experiments / 125

Commissioning the LHC Accelerator and its Physics Programme

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The LHC is an accelerator with unprecedented complexity where the energy stored in the magnets and in the beams exceeds that of other accelerators by one-to-two orders of magnitude. An initial phase of so-called “hardware commissioning” has thus been introduced, during which the comprehensive commissioning of all technical systems is undertaken without beam in an effort to ensure a safe and reliable start-up of the LHC accelerator and in order to minimise any technical problems. This paper presents the experience from this approach and presents the results. The strategy for the staged commissioning period with beam that is to follow the “hardware commissioning” phase is also presented. Typical accelerator parameters and associated performance levels are given for each stage with beam and a typical LHC accelerator schedule is shown.

All experiments will have installed initial detectors and will be ready for commissioning with beam at the start of LHC operation in 2008. The physics programme is expected to be rich even at the projected initial luminosities. This talk also presents the requirements and expectations of the experiments for the accelerator start-up with beam and early collisions, the heavy-ion runs and the special proton runs, initial conditions that may be used subsequently to set priorities in order to exploit optimally the first LHC beams for physics.
Completion of the CMS Muon Barrel Alignment System and its integration into the CMS detector environment.

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During the past years our group has built, calibrated, and finally installed all the components of the Muon Barrel Alignment System of the CMS experiment. This paper covers the results of the hardware commissioning, the full system setup and the connection to the CMS Detector Control System (DCS). The step-by-step operation of the system is discussed: from collecting the analog video signals and preprocessing the observed LED images, through to controlling the front-end PCs and forming the measurement results for the CMS DCS. The first measurement results and the initial experiences of the communication with the DCS are also discussed.

Summary:

Although all the elements of the CMS Muon Barrel Alignment System have been carefully tested during the assembly and calibration, it is mandatory to perform the full commissioning of the whole system. The commissioning consists of two steps: the functionality test, and the initial start-up measurement. During the functionality test, all the parts are checked using the full chain of installed elements including the cabling, Ethernet network, main control, DAQ PC and its software, and the low voltage units. After the functionality test, all the optical connections (i.e. each light source detected by the corresponding video-sensor) have to be measured. This measurement serves as an initial input to build up the control program based on the expected images and exclude the invisible connections (e.g. out of the visibility due to installation tolerances or objects blocking the light). The summary of the results of the commissioning is also given in the paper. Analog signals from the cameras are processed by a PC104-type computer, called the BoardPC. Each alignment module (MAB) has its own BoardPC, making 36 pieces altogether. Therefore, a highly parallelized computing network is formed. BoardPCs are equipped with a video digitizing card and a so called Custom Board, which was designed and produced by ATOMKI, Debrecen, Hungary. Each Custom Board contains a 24-way video multiplexer, several current generators for LED sources, and read-out electronics for digital temperature and relative humidity meters installed on the MABs. Drive units for these meters are also housed on the Custom Boards. Board PCs boot from the local network server, but after boot-up they act as autonomous machines and are able to calculate LED centroids or to submit raw images observed by their cameras. An additional computer acts as a boot, DHCP, and file system server. Furthermore, this machine coordinates the work of the BoardPCs and connects to the CMS online computing network. On this central controller machine, Java based software is responsible for the optimized measurement sequence, where the order of the individual centroid measurements are decided using applicable rules, rather than on a predefined sequence.

This Measurement Control software communicates with the supervisor panel via a custom protocol. This panel is written in a process monitoring language, used industry-wide, called PVSS. It gives information about the measurement and the actual status of the system. Alignment personnel can send commands through this panel. The other main part in our PVSS project is the Low Voltage control. The subsystem uses Caen power supply modules. This hardware communicates with PVSS via the OPC industrial standard. The supervisor panel allows alignment experts to set the low voltage modules of the system. The whole subsystem will use a finite state machine model, and will therefore fully comply with the experiment’s guidelines. Due to this, the Muon Barrel Alignment System can be fully integrated into the CMS Detector Control System. It means that our subsystem can provide states and alarms upward to the CMS Detector Control System, and is able to accept commands from the Run Control.
Control, test and monitoring software framework for the ATLAS Level-1 Calorimeter Trigger

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The ATLAS first-level calorimeter trigger is a hardware-based system designed to identify high-pT jets, electron/photon and tau candidates and to measure total and missing ET in the ATLAS calorimeters. The complete trigger system consists of over 300 custom designed VME modules of varying complexity. These modules are based around FPGAs or ASICs with many configurable parameters, both to initialize the system with correct calibrations and timings and to allow flexibility in the trigger algorithms. The control, testing and monitoring of these modules requires a comprehensive, but well-designed and modular, software framework, which we will describe in this paper.

Summary:

The ATLAS first-level calorimeter trigger (L1Calo) is a hardware-based system with a high degree of adaptability provided by widespread use of FPGAs. The real-time path of the trigger is subdivided into a Preprocessor which takes analogue signals from the calorimeters and digitizes them, followed by two digital processor systems working in parallel: the Jet/Energy-sum processor and the Cluster Processor. The design necessitates over 300 VME modules of about 10 different types, each of which has a unique register and memory map. The complete set of these modules contains around 2000 individually programmable registers, as well as many kBytes of look-up table memory.

It is clear that the software needed to control a system on this scale needs to be sophisticated enough to manage the different properties of each module, but also modular enough to be maintainable over the long period of commissioning and running of the ATLAS experiment. The L1Calo software is primarily written in C++ with some Java libraries included. Alongside the module control, there is also a safety monitoring system implemented via a Finite State Model operating over CANbus.

There are several distinct areas of software that can be clearly separated, but must have some means of interaction. For example, the configuration parameters must be stored in a common database framework which is independent of the rest of the software, but many of the other software components (e.g. configuration, monitoring) will need access to this information. The software framework must also fit into the existing ATLAS online software environment to be successfully integrated into a standard integrated run. Some of the design choices and implementations used in the L1Calo software framework will be described.

One of the most fundamental areas are the underlying VME access libraries, which were designed so that they could be used in several ways: under the control of run-control to configure modules at run start, using standalone programs or using an interactive GUI for expert intervention at the VME register level. Another large body of the software is dedicated to a detailed simulation of the hardware at the level of data that can be probed at each level of the trigger processing. This is again driven by the database settings to closely model the behaviour of each module. An exact match between the hardware and simulation results provides a rigorous test of the correct performance of the hardware.
There are several different libraries dedicated to calibration, both of signal timing and of energy of input signals. These are based around a common calibration strategy which extends the run concept to encompass multi-step runs, where parameters are adjusted between each run. Finally, and most recently, a set of libraries dedicated to monitoring and event-by-event analysis has been developed. These will be used to ensure that the trigger is operating correctly during normal data taking, immediately flagging up errors, inconsistencies or merely unusual features to the shift crew.

All of these areas of software will be described, with an overview of how they fit together in the L1Calo software architecture.

POWER WORKING GROUP / 159

Critical areas and ATLAS next steps

Parallel Session B5 - Power / 19

Custom DC-DC converters for distributing power in SLHC trackers

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The tenfold increase in the number of channels in SLHC trackers, and the wish to actually decrease the material budget to improve the physics performance of the detectors, set uncomfortable limits for the on-detector power budget. A power distribution system based on DC-DC converters has the potential to contribute significantly to the drastic reduction in wasted power necessary to meet these limits. A possible distribution scheme, based on two stages of conversion performed by custom-developed components, is discussed together with the main technical challenges for the development of these components.

Summary:

In the design of upgraded trackers for SLHC, the HEP community will strive to reduce material budget with respect to the LHC trackers just completed. A quick look at the relative contribution to the total material inside these trackers clearly shows that cables and cooling systems are amongst the 3 main contributors – the third being the mechanical supporting structure which is also somehow related to the other two.

Since both cables and cooling depend on the amount of power burnt in the tracker, we evidently need to manage such power: how to minimize the power necessary to perform the electronic functions required inside the trackers and how to bring this power where it is needed. To address the first issue, designers of front-end, control and communication electronics will need to optimize their designs to perform the essential functions at minimum power. This will most likely result in FE ASICs manufactured in advanced CMOS/BiCMOS technologies, where different voltage levels are used for different functionalities (e.g. analog and digital), and where large circuit blocks are turned off whenever possible. To address the second issue, the power distribution system shall provide regulated power to the on-detector electronics with minimum losses on the way. This implies the capability of locally supplying different voltage levels, with loads variable in time, from a small number of low-current cables from the off-detector power supplies.

This contribution presents a power distribution system based on two stages of DC-DC converters and having the potential to meet the above requirements.

A first stage with a conversion ratio of 4 reduces the input voltage to an intermediate bus voltage of
about 3V. This component shall therefore be compatible with an input voltage of 12V, which forbids the
use of the same advanced low-voltage submicron technologies used for the front-end ASICs. Special
high-voltage technologies from automotive applications look adequate, but require qualification and
special design techniques for reliable radiation hardness. One example of such qualification study will
be presented. On the other hand, the topology of this first stage of conversion is strongly influenced by
the necessity to use air-core inductors as magnetic elements, and of minimizing the output ripple and
the noise. A possible topology addressing all these constraints is discussed.

The second stage, acting as a Point-Of-Load converter, takes power from the 3V intermediate bus and
converts it to the appropriate voltage required by the electronics. This POL sits very close to the on-
detector ASICs, possibly even on-chip, and given the 3V input voltage requirement it can be manufac-
tured in the same advanced technology. This in turn makes it possible to achieve a switching frequency
in the tens of MHz range – which limits the noise injected in the system at frequencies where the FE
ASICs are most sensitive. A high switching frequency allows for inductor values in the nH range, avail-
able for on-chip integration in advanced CMOS processes for RF applications. A possible topology for
the POL converter will also be discussed.

POSTERS SESSION / 74

DAQ and Control Systems for the CMS Global Calorimeter Trigger Matrix Processor

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A new trigger component based on the uTCA standard is being developed for the CMS Global
Calorimeter Trigger (GCT). The new system is designed to handle the exchange of data between
GCT and the Global Muon Trigger and is called the GCT Muon System. The GCT muon system con-
sists of a uTCA crate with a custom uTCA backplane instrumented with several Matrix processor
cards, which use a Xilinx Virtex-5 FPGA and an M21141 72x72 cross-point switch. We discuss the de-
velopment and use of the various communication systems available for the Matrix processor. Given
the nature of the Virtex-5 FPGAs used as the basis of the design, there are several communication
protocols available. In this paper we focus on the use of PCI express and Gigabit Ethernet UDP/IP
using the built-in Virtex-5 interfaces, and TCP/IP and IPMB via an NXP microcontroller interface
on the Matrix board itself. The use of these interfaces for slow control of the board and fast Data Ac-
quisition (DAQ) are discussed in terms of available bandwidth and resource usage. Furthermore we
discuss the implications of the use of such industry-standard interfaces as a replacement for more
traditional simplex busses such as VME. To that end we outline the development of a new Hardware
Abstraction Layer (HAL) with built-in overlapped I/O and one possible serial bus architecture
providing a metastability-tolerant interface and auto-discovery for ease of use.

Summary:
The Matrix Processor is a generic processing module designed for use in the GCT Muon system as well
as a prototype for the next-generation CMS trigger system which is anticipated for future upgrades
of the off-detector electronics. The board combines advanced telecoms switching and the latest Xilinx
Virtex 5 FPGAs in a dense 3U uTCA form-factor. Being a specification based on serial links, uTCA
provides definitions of how to design electronics that can interoperate using several standard protocols,
including Gigabit Ethernet (GbE) and PCI express (PCIe), as well as a card management interface derived
from the Inter-IC (I2C) specification (called IPMB). The Xilinx Virtex-5 FPGAs natively support GbE and
PCIe, containing both tri-mode Ethernet MACs and PCIe endpoints. These can be driven either into the
uTCA backplane or to the optical fibres on the front of the Matrix board. The board also provides a
10/100 Ethernet control interface via an NXP microcontroller. This provides a plethora of interfaces to
choose from for both command/control and DAQ functionality.

In this paper we discuss the usage of these interfaces in the context of a larger configurable trigger
system. The implications of using these industry-standard interfaces and the replacement of more tra-
ditional simplex bus interfaces such as VME is also considered. To that end we discuss the development of a new Hardware Abstraction Layer (HAL) based on overlapped I/O that allows the concurrent completion of register reads/writes from a single application in a thread-safe manner, necessary for optimal performance when using such interfaces. Coupled to this we discuss a possible bus implementation that simplifies the construction of the internal configuration space in the FPGA firmware.

POSTERS SESSION / 99

DC- DC Power Conversion with Voltage Ratios > 10 for LHC Upgrade Detectors

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Our group is researching commercial power converters having voltage ratios greater than ten that are capable of running in the ATLAS Silicon Tracker high luminosity upgrade environment. The devices therefore must operate in a high magnetic field (2 T) and be radiation hard to ~50-100 MRad and ~ 1015 neq/cm². These converters are to be mounted on the same multi-chip modules as the ASIC readout chips or in close vicinity without introducing any additional readout noise due to the MHz switching frequencies. Such devices will permit higher voltage power delivery to the tracker and thus increase overall power efficiency by limiting the ohmic losses in the ~100 meters of cable between the tracker and the power sources.

Summary:

There is a clear need for a new system of power delivery to the upgraded Atlas Silicon Tracker for the SLHC. Conventional powering will result in an efficiency of power delivery to the detector of about 10% with existing cables whose size are already limited in cross section due to space and mass constraints. A system featuring DC-DC converters with voltage ratios of ten will result in an estimated efficiency on the order of 80% with existing cables.

One approach to DC-DC conversion utilizes the buck regulator architecture. As DC-DC buck converters are commonly used in the commercial market, we have been surveying and testing current available devices to understand the current state of the art. Additionally we are investigating industry trends to determine if a commercial solution with our unique requirements might be forthcoming.

Foremost of our unique requirements is operation in a high magnetic field. This necessitates the use of an air core inductor, which implies the need for high switching frequencies that lie in the readout ASIC’s bandwidth. Additional noise introduced by the converter is thus one of the primary concerns. The radiation hardness of the devices, and the relatively high voltage ratios needed are also of primary concern.

Over the past year we have tested a number of devices that, although they lack the high voltage ratios required, have enabled us to learn a number of lessons. For example, the one device that we irradiated with gammas up to 100 Mrad showed no change in performance. Also, we have conducted noise tests with our own custom module utilizing current Atlas ABCD ASICs connected to a large silicon strip detector and mounted with a daughter buck regulator board. We found no noise increase due to switching noise on the power and ground. Magnetic/electrical pickup on the 8 cm silicon strips from the air-core inductor required shielding to reduce the noise to a satisfactory level.
Market forces are now driving the development of a new generation of converters with ratios greater than 10. We will shortly be testing such promising devices for their radiation hardness, efficiencies and noise performance. Additionally, we have fabricated several small micro-H inductors that show promise in their initial testing. Results of the testing of the new devices will be presented.

**POSTERS SESSION / 76**

**Data Acquisition System for the KL Experiment at J-Parc**

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We present the proposed Data Acquisition (DAQ) System for the KL Experiment at J-Parc, Japan. It comprises three distinctive flavors of 6U VME boards: a 14-bit, 125 MHz ADC module for reading out an approximately 3000-channel Cesium-Iodide (CsI) detector; a 12-bit, 500 MHz ADC module for reading out a 100-channel Beam Hole Phase Veto (BHPV) detector; and a digital Trigger module able to provide a detector-wise synchronous energy sum. The CsI Calorimeter readout board amplifies analog pulses from 16 photomultipliers and passes them through a 10-pole shaper before digitizing. Data are then processed locally with field programmable gate arrays (FPGAs) to determine real-time energy values for the system Trigger Supervisor. The ADC module is provided with a pipeline, up to 4us long, which stores the acquisitions, awaiting the system trigger pulse. After a trigger, data are packed and buffered for readout via the VME32/64 backplane. The full design and preliminary test results will be described.

**Summary:**

This paper presents the Data Acquisition (DAQ) System for the Step-1 phase of the E14 experiment, a high energy physics kaon experiment at the Japan Particle Accelerator Research Complex (J-PARC). The goal of the experiment is to measure the rate of the rare decay KL->π0 νν̄bar. This flavor changing neutral current decay is predicted by the Standard Model to happen only once every 3.3×10^{11} KL decays. If not observed or observed at a rate very different from the predictions, it will shed light on the mechanism responsible for CP in the quark sector.

The front-end electronics comprises over seventeen 6U VME Crates, and includes three distinctive blocks:
- The Cesium Iodide (CsI), using custom 14-Bit, 125MHz ADC Modules, with 16 channels per module. This block has up to 3,000 Channels.
- The Veto Detectors, using the same custom 14-Bit, 125MHz ADC Modules, fitted with a different firmware. This block has up to 512 channels.
- The Beam Hole Phase Veto, using custom 12-Bit, 500MHz ADC Modules, with 4 channels per module. This block has up to 100 channels.

In the CsI Calorimeter, every analog pulse generated by the photomultiplier tube (PMT) is amplified and passed through a 10-pole filter/shaper with a cutoff frequency of about 10 MHz, which converts the fast PMT pulse into a Gaussian form, while keeping the total energy information constant. The filter/shaper was calculated for optimal Full Width Half-Height (FWHH) of the resulting shape with respect to fitting and timing. After shaping, each pulse is applied to a sample-and-hold ADC chip. Digitized data are processed locally with field programmable gate arrays (FPGAs). Altera EP2S60F1020C5 chips from the STRATIX II family that perform the board total energy calculation and determine real-time board energy related values. These values are passed through the crate’s backplane to custom Transition Boards for successive summing in the crate. The result is a crate-level energy value, which is sent over to the Trigger Supervisor Module, for final decision, and eventual trigger pulse generation. Each ADC module is provided with a pipeline, up to 4us (500 samples) long, which stores the acquisitions while awaiting the system trigger pulse. After a trigger, data are packed and buffered for readout. In this experiment, events happen in 0.75 second long "spills", followed by 2.65 second long periods of no activity. All events acquired in the 0.75 second spill can be stored in the on board 32 MBytes SRAMs. This allows readout only during the no activity period, to improve the overall signal-to-noise performance. The readout can be performed via the VME32/64 backplane, or via an optional front panel optical link.
Sampling for all calorimeter channels is simultaneous on one low jitter system clock. In conclusions, this DAQ System is designed to accommodate the particular requirements for the JParc KL Experiment, such as signal conditioning with 10-pole filters that convert narrow PMT signals into Gaussian shaped pulses with optimal FWHH; low input noise; powerful real-time processing with on board FPGAs, and relatively small overall size.

POSTERS SESSION / 134

Data acquisition systems for future calorimetry at the International Linear Collider

Matthew Wing

A data acquisition system is described which will be used for the next generation of prototype calorimeters for the ILC. The design is sufficiently generic such that it should have applications elsewhere, be they other ILC detectors or elsewhere within physics. An underpinning thread is the use of commercial components. Therefore the system should be easily upgradeable, both in terms of ease of acquiring new components and competitive prices. Results and tests already done will then be shown indicating the potential of the approach. The status of the system to read out prototypes in 2009 will be discussed.

Summary:
Within the CALICE collaboration, which is designing a calorimeter for the International Linear collider (ILC), a collection of UK groups (CALICE-UK) are part of the effort to prototype a highly-granular calorimeter composed of silicon and tungsten. The CALICE-UK groups have designed an R&D programme for the design of the data acquisition (DAQ) system for a future calorimeter. In the work, DAQ equipment will be developed which attacks likely bottlenecks in the future system and is also sufficiently generic to provide the readout for new prototype calorimeters, such as the prototype to be built in the EUDET project. The principle of a generic design using commercial components should be applicable to many detector sub-systems. Therefore, the R&D to be performed here may have consequences or applications for DAQ systems in high energy physics in general.

Although of a generic nature, the final ILC calorimeter acts as a test-case for the DAQ system under development. Data will be transported off the detector via a “Layer-1” switch which can re-route data should the off-detector data receiver not be available due to a fault or busy signal. These switches are cutting edge technology being used in the telecommunications industry and could improve the efficiency of data taking in high energy physics experiments. Further details of the overall system will be discussed, both for data coming off and being sent off the detector.

The PCs which act as the off-detector receiver contain PCI cards, which are again all based on commercial, off-the-shelf technology. The PCI card acquired has been developed and built by the company PLD applications. This contains optical and electrical links with a large FPGA and PCI-Express bus. The PCI card will act as a data receiver and also source for the clock, control and configuration data. This card will allow high data rates to be received off the detector which can then be used by detectors which require this or aggregate large amounts of data and thereby require less hardware. Results on the performance of the PCI card, optical switch and data transfer rates and efficiency will be discussed.

The actual system, based on the generic design, being built within the EUDET framework for the CALICE technological prototypes will be detailed and specifics of hardware and software given. Its status and readiness to read out prototypes in 2009 will be discussed.
Design Considerations for Area-Constrained In-Pixel Photon Counting in Medipix3

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Medipix3 is a single photon-counting hybrid pixel detector which records the discrete number of photons incident on a pixel. It aims to diminish the effects of charge diffusion across the sensor volume by considering the total charge collected by all pixels within a local neighbourhood during the evaluation of a charge event. The integration of multiple functions within the compact pixel area requires the manual layout of custom transistors, optimizing their physical placement and connections using non-standard techniques. This work describes various area-saving design strategies to optimize the use of available space in the digital section of the Medipix3 pixel.

Summary:
The digital section of the Medipix3 pixel two binary counters which can be read out in three readout modes: sequential read/write (SRW), continuous read/write (CRW), and semi-sequential read/write (SSRW). In SRW, both counters record charge events during the same exposure time, and then are read out in turn during the readout time. During readout, no charge events are recorded; thus there is "dead-time." In CRW, one counter records charge events while the contents of the other counter are serially shifted. In this mode, there is no deadtime, but only a single energy threshold is considered in the evaluation of charge events. In SSRW, the counters operate independently.

The digital counters can be configured as two 1-bit, two 4-bit, two 12-bit, or a single 24-bit binary ripple counter. In the event that a counter’s maximum value is reached, the charge counting pulses are halted in order to prevent overflow from occurring. The counters can be reset by either serially shifting ‘0’ through all the bits during readout, or by asserting an asynchronous FastClear flag.

The digital circuits occupy a total area of 52 µm by 21 µm. In order to fit as many transistors as possible within that area, minimum-sized transistors are used for the 0.13 µm IBM process.

Schematic-Level Area-Saving Techniques

The 24 counter bits occupy the most amount of space within the digital section of the pixel. Thus, extensive effort was expended on the optimization of the design of the bit. This paper will include a study of different flip-flop architectures which were considered for use in the counter bit. A 16 transistor master-slave static flip-flop was chosen for its small size and robustness. The paper will also discuss how area optimization was considered in the design of the overflow prevention and reset circuits.

Layout-Level Area-Saving Techniques

Standard digital design flows use pre-designed logic gates from digital design libraries. These libraries include a layout description of each logic gate. Place and route tools logic gate descriptions as fundamental building blocks and connect the individual logic gates together to realize the overall circuit. Although this is the simplest way to lay out a circuit, it is not the most area-efficient. Much area can be conserved by overlapping as many pairs of common nodes as possible within the same active area, to reduce the area cost of placing two discrete active areas side by side. Using this principle, the counter circuits are optimized in blocks of up to 120 transistors, and the layout of these transistors are physically placed such that as many pairs of common nodes share the same active area as possible. Furthermore, metal lines and vias are arranged such that the minimum spacing required by the process design rules is respected. Techniques to reduce the number of manual iterations required to find the optimal physical configurations of these transistors will be discussed. Such techniques are appropriate for area-constrained layouts where standard digital libraries and place and route tools cannot be used, and where the speed requirements are relaxed.

Parallel Session B5 - Power / 132
Design Considerations for High Step Down Ratio Buck Regulators

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Buck topology is the workhorse in most of the power electronic devices. Buck converter is step-down DC to DC converter. It utilizes two switches (two FETS or one FET and one diode) along with an output inductor and output capacitor.

Whether you look at the large computer server, personal computer Desktop or laptop, cell phone or GPS unit all will contain a buck topology design in one form or the other.

Summary:

As the name implies Buck converter reduces the input voltage. The simplest way to reduce the input voltage is to use a voltage divider circuit, but this is very inefficient and as the excess voltage is wasted as heat. An alternate method that would not waste energy and be reasonably efficient in the range of 90 +/-% efficiency. This can be achieved by using two FETS which are turned on/ off at a specific frequency resulting in chopping the input voltage and followed by the output inductor and capacitor (which is a low pass filter) the resulting chopped DC voltage is filtered by the output LC providing a clean stepped down DC voltage. The switch connects the source voltage to the inductor, where the energy is stored and in 2nd phase inductor is discharged into the load.

Buck converter is the basic building block that drives the power electronics. There are various forms of step-down converters, non-isolated or isolated versions of the same topology namely, push-pull, forward, flyback, active clamp forward are all isolated versions of step-down converters.

Prior to selecting the design approach, it is critical to understand the system needs/specs and design limitations

The paper with go thru the small signal analysis of buck converter using Vaporian’s switch model. This is a very powerful tool allowing one to analyze / simulate the circuit.

Considering the switching behavior of MOSFET is critical portion in order to evaluate the conduction and especially the switching losses associated with the topology. Both high side and low side MOSFET switching losses are analyzed. The drive circuitry along with the drive voltage plays a critical role in determining the switching losses. The paper will address these issues.

Parallel session A1 - ASICs / 93


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CMOS Monolithic Active Pixel Sensors (MAPS) have demonstrated their strong potential for tracking devices, particularly for flavour tagging. They are foreseen to equip several vertex detectors and beam telescopes. Most applications require high read-out speed, requiring sensors featuring digital
output with integrated zero suppression. The most recent development of MAPS at IPHC and IRFU addressing this issue will be reviewed. An architecture will be presented, combining a pixel array, column-level discriminators and zero suppression circuits. Each pixel features a preamplifier and a signal processing circuit (CDS) reducing the temporal and fixed pattern noise. The sensor is fully programmable and can be monitored. It will equip experimental apparatus starting data taking in 2009/2010.

**Summary:**

Subatomic physics experiments express a growing need for very high performance flavour tagging, with emphasis on short lived particles (e.g. charmed mesons) poorly accessible through their decay vertex with existing pixel technologies. The trend is therefore to go significantly beyond the tagging performances achieved up to now, relying on a highly granular, thin, radiation tolerant, fast and multi-layer vertex detector installed very close to the beam interaction point.

MAPS are developed since several years in order to fulfil this requirement, based on their intrinsically attractive trade-off between granularity, material budget, radiation tolerance and read-out speed. One of their most specific aspects is that the sensitive volume and the front-end read-out electronics are integrated on the same substrate. Being fabricated in standard CMOS processes available through many commercial microelectronics foundries; they are attractive for their cost effectiveness and the fast multi project run turn over.

MAPS were retained for several applications, ranging from subatomic physics experiments to bio-medical imaging devices. Their first use inside a vertex detector is associated to the upgrade of the STAR experiment at RHIC. MAPS also equip the beam telescope of an EU project, called EUDET, underlying the R&D for the ILC (International Linear Collider) vertex detector. The most recent steps of the development of MAPS for these applications achieved at IPHC-Strasbourg and IRFU-Saclay will be presented.

Numerous application domains require simultaneously high granularity and fast read-out speed. Integrating signal processing functionalities inside the sensor, such as CDS (Correlated Double Sampling), AD converter, data zero suppression circuitry is then facing severe constraints from the pixel dimensions, readout speed and power consumption. The purpose of the contribution is to show a new CMOS MAPS architecture combining on the same substrate a pixel array with 18.4 µm pitch occupying an active area of about 2x2 cm², column-level discriminators for analogue-to-digital conversion and a zero suppression circuit for data sparsification. Each pixel contains an amplifier and a CDS micro-circuit achieving temporal and fixed pattern noise reduction. The sensor is fully programmable and can be monitored via a JTAG controller.

The development of this architecture is based on 2 separate prototyping lines: one addressing the upstream part of the signal detection and processing chain, and one devoted to data sparsification and formatting. 2 prototype circuits were fabricated in the AMS CMOS 0.35µm technology addressing these two research lines. The sensor exploring the signal sensing and analogue processing features 128 columns of 576 pixels ended with a discriminator. Each pixel contains a pre-amplifier and a CDS circuitry. The sparsification chip incorporates the zero suppression logic and the output memories needed for the EUDET beam telescope and the STAR vertex detector upgrade.

The contribution to the workshop includes a description of the architecture of both chips and an overview of some prominent tests results.

**Parallel session B2 - Optoelectronics / 69**

**Design and Radiation Assessment of Optoelectronic Transceiver Circuits for ITER**

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We present the design and characterization results of different electronic building blocks for a MGy gamma radiation tolerant optoelectronic transceiver aiming at ITER applications. The circuits are implemented using the 70GHz ft SiGe HBT in a 0.35µm BiCMOS technology. A VCSEL driver circuit has been designed and measured up to a TID of 1.6 MGy and up to a bit rate of 622Mbps. No significant degradation is seen in the eye opening of the output signal. On the receiver side, both a 1GHz, 3kΩ transimpedance and a 5GHz, 20dB Cherry-Hooper amplifier have been designed.

Summary:
In future nuclear fusion reactors, in case ITER (International Thermonuclear Experimental Reactor), the requirements of integrated electronic circuits with respect to radiation tolerance are quite severe. For instance, during remote-handled maintenance tasks, several systems and circuits will need to remain operational even after exposure to a TID (Total Ionizing Dose) in the order of MGy. The development of instrumentation for controlling the robotics needed to perform these periodic maintenance tasks in the reactor core is therefore challenging. The anticipated gamma radiation levels are similar to those expected in the S-LHC. This paper will focus on the potential use of a fiber optic communication link as an umbilical between the robotics and the control room. More specifically we will present and discuss our recent results on the design and assessment of the radiation hard optical transceiver electronics. All circuits are implemented using the 70GHz ft SiGe HBT in a 0.35µm BiCMOS technology.

For the transmitter side a driver was implemented for a long wavelength (1550nm) VCSEL (Vertical Cavity Surface Emitting Laser). The circuit was tested before, during and after several Co60 gamma irradiation experiments up to a TID of 1.6MGy. The off-line measurements of the driver applying a 27-1 PRBS up to 622Mbps reveal a near constant eye opening in the output signal. The output current through the laser for a digital 1 input will be shown to remain constant within 0.2%, as obtained from the measured data during irradiation. These results can be related -through SPICE simulations- to the characterization results of the individual transistor components under the same radiation conditions. Even though several transistor parameters are observed to shift dramatically, the performance characteristics of the driver show only minimal degradation.

On the receiver side several electronic building blocks have been designed in the same 0.35µm BiCMOS technology. The TIA (Transimpedance Amplifier) is the first block after the photodiode and converts the diode current into a voltage, sufficiently high above the noise floor of the subsequent PA (PostAmplifier). The TIA features a transimpedance gain of 3kΩ for a 1GHz bandwidth. The equivalent input noise current given by the integrated output noise voltage divided by the transimpedance gain is 0.6µA. The circuit was designed taking transistor radiation effects into account. We included the previously measured degradation in the simulation via a DC SPICE model extension of the bipolar transistors. For the PA a sequence of differential bipolar Cherry-Hooper amplifiers was designed with a simulated bandwidth of 5GHz and a gain of 20dB per stage. The receiver circuits are currently being processed.

In summary, we will present recent design and characterization results on the most critical electronic building blocks in a MGy radiation tolerant optoelectronic transceiver for application in ITER. All circuits were designed in a 0.35µm SiGe BiCMOS technology.

Parallel Session A5 - Installation & Commissioning / 79

Design and commissioning of the ATLAS Muon Spectrometer RPC Read Out Driver

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The RPC subsystem of the ATLAS muon spectrometer provides the Level-1 trigger in the barrel and it is read out by a specific DAQ system. On-detector electronics pack the RPC data in frames, tagged
with an event number assigned by the trigger logic, and transmit them to the counting room on optical fibre. Data from each sector are then routed together to a Read-Out Driver (ROD) board. This is a custom processor that parses the frames, checks their coherence and builds a data structure for all the RPCs of one of the 32 sectors of the spectrometer. Each ROD sends the event fragments to a Read-Out subsystem for further event building and analysis. The ROD is a VME64x board, designed around two Xilinx Virtex-II FPGAs and an ARM7 microcontroller. In this paper we describe the board architecture and the event binding algorithm. The boards have been installed in the ATLAS USA15 control room and have been successfully used in the ATLAS commissioning runs.

**Summary:**

In the beams of the LHC collider, protons are grouped in “bunches” that interact (bunch crossing) every 25 ns. From the point of view of the trigger system, the ATLAS apparatus is a synchronous network working at the bunch crossing frequency (40 MHz) of the LHC. For each of the 32 sectors of the barrel spectrometer, the front-end electronics pack RPCs’ data in frames, tagged with an event number assigned by the trigger logic. Data in each event are associated to a unique progressive number (Event Identifier, or EVID) and to a number identifying the bunch crossing that generated the collision (Bunch Crossing Identifier, or BCID). Data from each sector are transferred to the counting room via optical fibre and are then routed to a Read Out Driver (ROD) board.

The ROD hosts an event builder logic based on a Finite State Machine cluster that parses the frames, checks their syntax and builds an event fragment. Each ROD sends the event fragments, across the optical link S-Link, to a Read-Out subsystem for further event building and analysis. The ROD also manages the timing signals of the trigger and data acquisition system. For this purpose, the ROD hosts a TTCrq receiver module from which it optically receives the ATLAS timing and control signals. The ROD is a VME 64x board, equipped with two XILINX Virtex II FPGAs, labelled as VME FPGA and ROD FPGA, and an ARM7 microcontroller.

The VME FPGA interfaces the whole board with the VMEbus and allows the user to access the ROD FPGA memory locations and configuration registers and to read the microcontroller’s data. The core of the ROD board is the ROD FPGA. It performs the event building of the detector data by means of a cluster of Finite State Machines (FSMs). Also, this FPGA hosts the registers for the configuration and control of the entire event builder engine. It is interfaced with the TTCrq module - from which it receives the TTC timing signals and the 40 MHz LHC’s clock - and to the S-Link transmitter. The ROD FPGA communicates with the VME FPGA via a serial synchronous custom protocol, carried out by two point-to-point unidirectional lines with a data rate of 80 Mbit/s. The main task of the ARM7 microcontroller is to program the TTCrq receiver, via I2C protocol. This makes it possible to access all the TTCrq registers, both for configuration and monitoring purposes. The microcontroller also allows reading, via the internal ADC, the three power supplies on the ROD board (5V, 3.3V, 1.5V).

The ROD Event Builder Engine has been designed with some error handling procedures, in order to recovery from EVID or BCID errors, format or syntax errors and timeout errors. Some specific fields are also included in the ROD frame, in order to perform analysis on the ROD event builder performances. In this paper we describe the board architecture and the event binding algorithm. The boards have been installed in the ATLAS USA15 control room and have been successfully used in the ATLAS commissioning runs. During the commissioning of the ATLAS Muon Spectrometer, several millions of cosmic muons have been acquired through the Read-Out Driver without any failure of the event building logic.

**POSTERS SESSION / 15**

**Design and measurements of SEU tolerant latches.**

Mohsine Menouni

1 Unknown

The single event upset (SEU) tolerance of various latch designs in 0.13um CMOS technology has been studied by both measurement and simulation. The aim of this work is to optimize the design for critical registers on the next generation pixel readout chip for ATLAS upgrades (denominated FE-I4). Results form irradiations with 24 GeV protons will be presented and compared to previous
Design studies of a low power serial data link for a possible upgrade of the CMS pixel detector

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The material budget inside the sensitive tracking volume is highly dependent on the dissipated power for data transmission. It is therefore important to have a very low power serial data link, that allows to transmit digital data over short distances within the tracking volume. Such a low power ohmic data transmission through micro-twisted transmission lines aims for a transmission speed of 160/320 MHz and allows to concentrate the tracker data to multi gigabit optical data hubs. For such a future link we need low swing differential drivers and receivers with PLLs for frequency multipliers and clock recovery. We have implemented in radiation hard layout all the necessary components on a recently submitted 250nm CMOS test chip. After reporting on the experience gained with low power data transmission in the current CMS pixel detector we present the design considerations and first results for this new 160/320 MHz serial link that may work with differential signal levels as low as 10mV.

Design, production and first operation of the ALICE Silicon Pixel Detector system

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The ALICE Silicon Pixel Detector (SPD) constitutes the two innermost barrel layers of the ALICE experiment. The SPD is the detector closest to the interaction point, mounted around the beam pipe at r=3.9 cm and 7.6 cm, respectively. In order to reduce multiple scattering the material budget per layer in the active region has been limited to \( \approx 1\% \) X₀. It consists of 120 hybrid silicon pixel detector modules with a total of \( \approx 10^7 \) cells. The on-detector read-out is based on a multi-chip-module containing 4 ASICs and an optical transceiver module. The control room located read-out electronics is housed in 20 VME boards and builds the interface to the ALICE trigger, data acquisition and control system. In this contribution the detector components design and production are reviewed. The detector commissioning and experience during first operation are presented.

Summary:

The ALICE Silicon Pixel Detector (SPD) constitutes the two innermost barrel layers of the ALICE experiment. The SPD is mounted close to the interaction point (r=3.9 cm and 7.6 cm, respectively). It consists of 120 hybrid silicon pixel detector modules (half-stave) with a total of \( \approx 10^7 \) cells. The active elements of the half-stave are two silicon sensors (70.7 x 16.8 mm²) glued to a multi-layer Al flexible flat cable carrying power and signal lines. Each half-stave consists of 10 pixel chips bump bonded to the two silicon pixel sensors and is read out by a multi-chip module. Each pixel chip contains a matrix of 8192 cells. Out of the SPD acceptance area copper flat cables are used for power supply connections. The off-detector electronics in the control room consists of 20 VME boards (router). Each router holds three plug-in daughter cards (link receiver), which are connected to two detector modules each.
off-detector electronics forms the interface to the ALICE trigger, data acquisition and detector control system. A complex optical fiber distribution network with a high number of intermediate patch panels connects the detector modules to the electronics in the control room.

The SPD cooling is based on a C4F10 evaporative system with 40 μm thin cooling pipes directly integrated into the carbon fiber support structure, on which the half-staves are glued. PLC based interlock processors monitor constantly the temperature of the half-staves and act directly on the power supplies. The constraints in terms of compactness and material budget of the SPD required the development, prototyping and qualification of many different components. The SPD has been installed in summer 2007. Commissioning runs and dedicated cosmic ray sessions have been undertaken. A review of the design, production and installation process is reported in this contribution, as well as the system commissioning and the experience during first operation.

**TUTORIAL - Designing Printed Circuit Boards Not To Fail / 154**

### Designing Printed Circuit Boards Not To Fail (1)

1) Circuit boards fail primarily for mechanical and electro-chemical reasons.
2) Failure mechanisms in circuit boards.
   a) Vibration (mechanical fatigue).
   b) Mechanical shock (high stress).
   c) Thermal fatigue (thermally induced fatigue).
   d) Humidity effects (diffusion of water vapor).
   e) Condensing moisture effects (electromigration and dendritic growth).
3) These failure mechanisms represent stresses that produce cumulative damage effects that lead to loss of product life over time.
4) "Time-to-failure as a function of the stress" can be modeled as a stress-life relationship on log-log paper. This will later allow us to produce equivalent damage accelerated tests.
5) What is design margin?
   a) Stress-Strength interference.
   b) Design margin is also easily portrayed on the life-stress relationship graph.
6) We need design margin for each failure mechanism relative to the damage it will see in its intended lifetime.
   a) The intended lifetime is defined as the severe use application.
7) How much margin is enough?
   a) Where does the 3X concept come from?
8) What is "Damage in its intended lifetime" and how do we quantify this damage.
   a) The severe use situation as a function of the normal use – the other 3X concept.
9) Design process to insure that we have adequate margin against a lifetime of damage for the severe use situation.
   a) Design equations for thermal fatigue. (example worked in class)
   b) Design equations for vibration. (example worked in class)
   c) Design equations for humidity. (example worked in class)
   d) Design solutions for condensing moisture. (examples shown)
10) Summary of test methods for weakness discovery and design margin evaluation

**Summary:**

Understanding the physics of how circuit boards fail provides the ideal starting point for failure prevention. This half day tutorial will begin with a comprehensive explanation of the "physics of failure" for electronic circuit boards, and then provide design solutions relative to each failure mechanism discussed. Empirical design equations along with test methodology will be explained through examples. "Quick Learning Cycle" test methods that help in the design for reliability will be explained through video examples.

Quantitative reliability planning and evaluation for circuit boards will be explained through the concepts of Stress-Life models and Stress-Strength Interference. Design margins needed for the severe use situation will be explained as well as how to quantify the severe use condition. The class will culminate with an explanation of test flow design that includes the best reliability test methods including acceleration factors resulting from increased stress testing.
POSTERS SESSION / 28

Detector Control System for the electromagnetic calorimeter in the CMS experiment – summary of the first operational experience.

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A full scale implementation of the Detector Control System (DCS) for the electromagnetic calorimeter (ECAL) in the CMS experiment is presented. The operational experience from the ECAL commissioning at the CMS experimental cavern and from the first ECAL and global CMS data taking runs is discussed and summarized.

POSTERS SESSION / 112

Detector noise susceptibility issues for the future generation of High Energy Physics Experiments

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The electromagnetic noise characterization of the FEE and the compatibility of the different systems are important topics to consider during the experiment upgrades. A new power distribution scheme based on switching power converters is under study and will define a noticeable noise source very close to the FEE detector electronics. The knowledge of the FEE noise issues in previous detectors is an important object to guarantee the design goals and the good functionality of the detector upgrade. This paper shows an overview of the noise susceptibility studies performed in different CMS sub-detectors. The impact of different topologies in the final FEE sensitivity and design recommendations are presented to increase the robustness of the systems to the future challenging power distribution topologies.

Summary:

Electromagnetic noise and interference have been a major concern during the integration of the CMS experiments. Grounding and shielding problems have arisen during the integration stage in different sub-detectors requiring time, an important number of tests and studies to solve them. The effort to find the root cause and the solution of these problems can be minimized performing noise susceptibility studies during the design and the prototype stage of the FEE.
In general, most of the detector electromagnetic compatibility problems are associated with the noise level both generated by power units and radiated by the distribution system and the susceptibility of the FEE. Switching power supplies generate high frequency noise due to the switching action. This noise propagates through the distribution cables and boards, where can be either radiated to other systems or conducted to the FEE, reducing the performance of the experiment. Although a big effort is put in the converter design to reduce the noise emission, the levels achieved have to be directly compatible with the levels required by HEP detectors defined by the intrinsic FEE topology and the integration of the unit at system level. The front-end electronic noise sensitivity level can be either evaluated at the early stage of the system design via modelling and simulation or measured on prototypes. In the first case, corrective actions can be taken during the design stage, whereas in the second case, it is possible to identify from prototypes critical elements and inappropriate layouts that are responsible for the performance degradation of the FEE. To define the immunity level of the FEE to conductive disturbances, several tests are conducted by injecting currents through the FEE input power terminals and slow control cables. The goal of these tests is two-fold: firstly, the test will characterize the immunity of the system to RF perturbations defining weak points in the design and second, it will provide data to define the emission level to be imposed to the switching power supply connected to them.

This paper presents the characterization of the FEE sensitivity of different CMS subsystems to common mode and differential noise. The variation of the susceptibility function corresponding to different CMS front-end electronics respect to the grounding connection, filter implementation, cable and shield connections, detector-FEE connections and PCB designs are analyzed. Noise immunity tests and numerical simulations of the FEE susceptibility have been used to evaluate the weakest areas of the system and to define the impact of the design in the noise immunity of the next generation of high energy physics experiments. Based on these measurements and analysis, design recommendations are presented to increase the robustness of the system to the future challenging power distribution topologies.

POSTERS SESSION / 11

Development and Testing of an Advanced CMOS Readout Architecture dedicated to X-rays silicon strip detectors

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An advanced VLSI analog readout architecture, dedicated for X-ray imaging. Critical design issues such as the noise optimization and the shaper implementation technique are addressed and the first test results of a fabricated prototype in a 0.35 μm 3.3 V CMOS process are presented. Important feature of the design is the novel CR-RC² pulse shaper configuration since in this section, transconductor circuits are used in order to provide a broad range of continuous variable peaking time, programmable gain and adjustable undershoot while still maintaining the noise performance and the required linearity of the specific radiation detection application.

Summary:
Using the leapfrog filter design methodology and the Semi Gaussian shaping theory an advanced front end analog processor for a particular X-rays radiation detector was proposed. The specific processing channel consists of a low noise pre-amplification block and a pulse shaping stage and has been designed for multi-channel radiation detectors with capacitance ranging from 1 to 10 pF. In the specific ASIC a novel shaping filter topology based on operational transconductance amplifiers is addressed. Some design considerations and the noise optimization of the pre-amplification stage are also presented. The total IC readout system compatibility to the stringent nuclear spectroscopy requirements is examined performing measurements that confirm its satisfactory performance. The architecture although it provides a relatively long peaking time, is fully integrated and appears to be greatly flexible since the use of OTAs as the topology building cells results to externally adjustable characteristics. Considering the architecture measured performance, the prototype provides peaking time 1.81 μs, conversion gain of 3.3 mV/fC and enc (e- rms) of 382 e- + 21 e-/pF. The system consumes 1mW and the occupied area of the
full VLSI structure is 0.2017mm². Characterization of the analog processor and measurement results are presented supporting the theoretical analysis and confirming that the system operates according to design specifications and can be used for nuclear spectroscopy applications. Concerning future improvements, the shaping filter can be even more optimized mainly in terms of the linearity and the power dissipation performance. Better linearity results can be obtained at the cost of power dissipation by increasing the power supply rails. Additionally, it can also be improved in terms of the OTA circuit since several low power and low voltage advanced design techniques are available in the IC literature.

**Parallel session A1 - ASICs / 14**

**Development of FE-I4 pixel readout IC**

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A new hybrid pixel readout integrated circuit denominated FE-I4 is being developed for use in ATLAS upgrades. The design goals include 4 times higher rate capability, 4 times the active area (full reticule), and 38% smaller pixels than the presently used FE-I3 IC. The target applications are a possible smaller radius replacement of the present inner layer and/or outer layers or disks of a super-LHC detector. For the innermost layer of a super-LHC detector a further design generation will be needed, and the present effort serves as a stepping stone towards this ultimate goal. Small size analog/digital prototype blocks have been fabricated in 0.13um feature size bulk CMOS technology. An overview of the full chip design-in-progress is presented, along with status and test results from various test chip prototypes.

**Plenary Session 2 - OPENING / 138**

**Development of a 3.2 GPixel Camera for the Large Synoptic Survey Telescope (LSST)**

The LSST is an 8.4 meter survey telescope currently under development for operation on the 2,700 meter Cerro Pachon mountaintop in central Chile. LSST will have features which make it uniquely capable of carrying out multiple science missions including "Type 1A" supernovae surveys to constrain dark energy parameters, weak lensing probes for dark matter tomography, transient phenomena, galactic structure, and "Near Earth Asteroid" (NEA) discovery. These science goals impose strict requirements and challenges for the LSST camera. These include a wide-field (3.2 GPixel), high quantum efficiency focal plane, and 3,200 channels of high speed, low noise readout electronics contained within the camera. This paper describes those challenges and the development of the camera, its sensors, and the readout electronics required to meet them.
Parallel session A1 - ASICs / 87

Development of a Front-end Pixel Chip for Read-out of Micro-Pattern Gas Detectors.

Harry van der Graaf, Ruud Kluit, Vladimir Gromov

*NIKHEF*

With a growing need for high resolution, radiation hard and low mass pixel detectors the Micro-Pattern Gas Detector is a good candidate. This detector requires a dedicated front-end read-out chip with improved readout architecture to deal with the high data rate. In addition, it is highly required to keep power consumption as low as possible.

Some of prototype IC’s have already been submitted and tested in order to demonstrate high performance of a new front-end (preamplifier and comparator) and feasibility to implement high resolution TDC-per-pixel architecture.

In line with the present results we will discuss design goals and system requirements for a full-reticle chip.

Summary:

Recently the RD51 collaboration has been initiated with the purpose to bundle and coordinate developments of Micro-Pattern Gas Detectors (MPGD). MPGD’s could very well be used in tracking detectors for upgrades of ATLAS and CMS and large area TPC’s. Optimization of the read-out electronics is one of the goals of the collaboration. At this moment seven institutes and organizations have expressed interest in a common development of a pixel front-end chip optimized for MPGD’s.

Some of the system requirements are the following:
1) For high spatial resolution pixel’s pitch is to be about 55 um.
2) For 3D track reconstruction high resolution (sigma is 0.5 ns) drift time measurements are required.
3) Low gas gain operation and high single electron efficiency are needed. This requires low-threshold operation (threshold of 400 electrons) and therefore low input referred noise (sigma is 80 electrons).
4) Pulse height measurements are required (time-over threshold method).
5) Simultaneous data taking and data readout is required.
6) Required modes of operation.
   a) All pixels data readout mode (image frame based).
   b) Data (hit) driven readout mode (continuous readout with zero suppression).
   c) Triggered data readout mode (only data associated within a certain time window).
7) Power consumption 200mW/cm2 (preliminary target).

The GOSSIP0-2 chip is a prototype for the MPGD front-end electronics [1]. The main goal of the prototype was to demonstrate the feasibility and behaviour of TDC-per-pixel concept based on local oscillator (540MHz) architecture [1] in a 16x16 pixels array. It has been reported before that such a TDC block itself complies with system requirements such as high precision of the drift time measurements, low power consumption and good robustness to instability of the power supply voltage and temperature.

At the same time, the ongoing testing of the GOSSIP0-2 chip indicates that the time resolution of the digital TDC block is limited by the performance of the preamplifier and the comparator. We will discuss these limitations and other unexpected problems occurring in the front-end block of the pixel read-out and possible improvements.

Proposal for dedicated readout architecture with different modes of operation will also be discussed.


POSTERS SESSION / 117

Development of a fast readout system for DEPFET sensors

Author(s): Manuel Koch
The DEPFET sensor is a favorable technology for use in particle physics experiments. The current system is developed for application in the vertex detector of the planned International Linear Collider (ILC). Besides high spatial resolution, low noise and a low material budget a very high readout speed is required. A new prototype readout system has been built; utilizing a new generation of DEPFET sensors (PXD5) with up to 256x1024 channels, new steering ASICs (called Switcher3), new readout ASICs (called DCD2) and a new FPGA-based high speed PCB. An overview of this system will be given and first measurements will be shown.

Summary:

The DEPFET sensors are based on a fully depleted high resistivity silicon substrate, where a field effect transistor is directly integrated into every pixel. An additional implantation below the FET creates a potential minimum for electrons right underneath the transistor channel. Signal electrons created by an impinging particle will be collected in this so-called internal gate, resulting in a modulation of the transistor current. This concept allows the first amplification stage to be realized with a very small input capacitance, thus featuring intrinsically low noise measurements. Pixel sizes of 24x24um² guarantee a binary position resolution of ~7um, while a resolution <4um can be achieved using analog readout. In addition to high spatial resolution, low power consumption and low material budget, the physics goals of a future vertex detector for the ILC require a high readout speed to cope with the expected hit densities. For this purpose a new prototype readout system is being developed. The DEPFET system consists of the sensor matrix itself, a control ASIC (called Switcher3), a readout ASIC (called DCD2) and a FPGA-based control and data acquisition system.

The Switcher3 chip is a fast analog multiplexer with an integrated intelligent sequencer. It is used to select and enable individual pixel rows for readout operation, and to perform a clearing operation of the accumulated charge. The outputs must be able to switch voltages of up to 10V and achieve rise/fall times of <10ns for a load of 20pF. Fast settling times are not only crucial for high speed readout, but also for complete clearing of the accumulated charge ensuring a low noise operation. The second ASIC (DCD2, “drain current digitizer”, successor of CURO) is used to process the drain signal currents of the DEPFET. The drain voltage has to be kept constant for high speed readout; therefore a regulated cascode has been chosen to provide a low input resistance to the DCD2 chip. The design has been optimized for input capacitances of up to 40pF, which corresponds to the drain lines of long DEPFET matrices (1024 Switcher channels and 256 readout channels). The DCD2 chip features an algorithmic current-based ADC with eight bit resolution in every input channel; the signal currents are immediately digitized. One LVDS channel per six input channels is used to transfer the data to an FPGA at rates up to 600Mbit/s. This prototype ASIC allows the connection of up to 72 input channels. A new readout PCB has been designed, featuring a Virtex-4 FPGA and a USB2 connection for data transfer to a PC. It can provide all necessary steering signals for the Switcher3 and DCD2 chips, while also providing the connectivity for future beam test efforts. A burst data rate of 14.4Gbit/s per 144 DCD2 input channels is supported. An additional focus is the implementation and testing of algorithms for zero suppression and data manipulation. Additionally, a new Hybrid PCB has been designed, hosting one DCD2 and two Switcher3 chips. A 128x128 DEPFET matrix can be connected; optionally a 256x1024 DEPFET matrix can be used to evaluate the readout performance with higher input capacitance.

POSTERS SESSION / 34

Digital part of PARISROC: a photomultiplier array readout chip

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PARISROC is the front end ASIC designed to read 16 PMT for neutrino experiments. It’s able to shape, discriminate, convert and readout data in an autonomous mode. The digital part manages
each channel independently thanks to 4 modules: top manager, acquisition, conversion and readout. Acquisition is in charge to manage the SCA with a depth of 2 for charge and fine time measurement. Coarse time measurement is made with a 24 bits gray counter. Readout module sends converted data of hit channels to an external system. Top manager controls the start and stop of the 3 others modules. The ASIC will be submitted in June 2008.

Summary:

PARISROC (Photomultiplier ARray Integrated in Sige ReadOut Chip) is the front end ASIC designed for the FMM2 R&D project dedicated to neutrino experiments. Next generation of neutrino experiments that will take place in megaron size water tanks will require very large surface of photodetection and volume of data. For the funded project, this large surface of photodetection is segmented in macro pixels made of 16 Photomultiplier tubes (PMT) connected to an autonomous front end ASIC: PARISROC.

The digital part of the ASIC is made of 4 modules which are acquisition, conversion, readout and top manager. Actually, PARISROC is based on 2 memories. During acquisition, discriminated analog signals are stored into an analog memory (the SCA: switched capacitor array). The analog to digital conversion module converts analog charges and times from SCA into digital values. These digital values are saved into registers (RAM). At the end of the cycle, the RAM is readout to an external system.

The SCA of each channel are managed independently like a FIFO. During acquisition data are written into the SCA. In fact the voltage is held into the capacitor thanks to a "track and hold" cell. When analog to digital conversion is in progress, analog signals are read and compared to a ramp of a Wilkinson ADC. Finally, after the readout, data are erased from the SCA. Then, the SCA is operational for another acquisition (track mode). As the SCA depth is 2, during conversion and readout discriminated signals can still be stored in the SCA.

For the readout, only hit channels are send out with a pattern of 4 data: channel number, coarse time, charge and fine time. Each data is coded in gray and the total number of bit for one frame is 52 bits. The top manager module controls the 3 others ones (Acquisition, Conversion, Readout). When 1 channel is hit, it waits a constant delay to allow triggers on others channels. Then ADC conversion and readout are respectively launched. The maximum cycle length is about 200µs when all channels are hit.

The layout of PARISROC is made in AMS 0.35µm SiGe process. The dimension of the digital part is about 1800 x 1000µm with a total number of I/O of 137. The ASIC will be submitted in June 2008 and first tests results are expected at the end of 2008. PMM2 is funded by the French National Agency for Research under the reference ANR-06-BLAN-0186.

Parallel session B1 - Trigger 1 / 26

Digital signal integrity and stability in the ATLAS Level-1 Calorimeter Trigger

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The ATLAS first-level calorimeter trigger is a hardware-based system designed to identify high-pT jets, electron/photon and tau candidates and to measure total and missing ET in the ATLAS calorimeters. Apart from the initial analogue stage, the trigger system consists of a multi-stage pipelined digital processor distributed over several crates of custom-built modules. The high demands for interconnectivity between both crates and modules are solved by a variety of high-speed digital links, using several signaling standards, including both electrical and optical transmission. The techniques used to establish timing regimes, and verify correct connectivity and stable operation of these digital links, will be presented.

Summary:

The ATLAS first-level calorimeter trigger (L1Calo) is a hardware-based system with a high degree of adaptability provided by widespread use of FPGAs. The real-time path of the trigger is subdivided into a Preprocessor, which takes analogue signals from the calorimeters and digitizes them, followed by two digital processor systems working in parallel: the Jet/Energy-sum processor and the Cluster Processor. The full system has been installed since the end of 2007, and has now been tested both stand-alone and in integrated runs with the rest of ATLAS over a long period.

The overall performance of the trigger in ATLAS commissioning and early LHC data is discussed in a separate contribution, as is the analysis of the analogue signals from the calorimeters. This contribution will detail the methodology and results of commissioning the many digital links needed to perform the trigger processing.

There are many separate stages of digital connectivity along the various processing paths in the L1Calo system, each with different contraints, and therefore almost as many different solutions to the challenges at each stage. The choices of technology were governed by the required band-width into and out of each processing element, be it an FPGA, module or crate. The basic unit of input to the digital processor is an 8-bit calibrated transverse energy value, of which there are over 7000 instances. The algorithms demand that many of these are used as input to multiple instances of each algorithm. The processing clearly must be performed in parallel, but the overlapping nature of the algorithms means that much of the data must be duplicated to several locations.

The vast majority of the inter-crate digital connectivity is used to transfer the individual energies to the algorithm processing systems. This is achieved using high-speed serial LVDS links. Over 7000 differential pairs are required, and both the exact connectivity and correct timing of these signals is crucial to the performance of the trigger. The methods used to establish a good timing regime, and also to verify that no cables are misconnected, will be presented.

Within the digital processor crates, the challenge of inter-module connectivity is met by a dense custom backplane with approximately 22,000 pins per crate. This carries digital signals of various standards and at different speeds. For the real-time path, the fastest signals run at 160 Mbit/s using a single ended protocol to minimize pin count. These connections also require careful timing and verification, and results of these tests will be shown.

Amongst the other digital links in the system are the readout links, which allow data to be recorded in order to verify the correct performance of the trigger. All significant modules in the system provide read-out data, and a common link solution was used by all modules to send this data. This consists of optical fibres using a serial transmission protocol. All such read-out fibres are routed to Readout Drivers, which differ only in the firmware load needed to format the data for each module. These, and other, links were also tested for stability and correct data transmission, and the methodology and results will be presented.

Discussion

Discussion
Discussion

Distributed Low Voltage System for the FrontEnd electronics of the HADES RPC TOF wall

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This contribution presents the power supply system designed for the frontend electronics of the HADES RPC detector, installed at GSI (Darmstadt, Germany). The system is designed as a distributed architecture and contains custom Low Voltage boards based on DC-DC switching converters to obtain high efficiency and reduce spacing. The switching converters have been conveniently filtered to reduce EMI, obtaining very low output noise. Experimental results prove that the low noise levels achieved at the output of the switching converters behave as good as laboratory power supplies, not producing any worsening in the response of the frontend electronics.

Summary:

The high sensitivity and bandwidth required by frontend electronics in physics experiments requires low noise supply voltages. Despite power supply systems being traditionally based on commercial linear power supplies, which provide very clean voltages, the increase of power demand with bigger and bigger experiments requires the development of more efficient and custom solutions.

The power supply system developed for the Resistive Plate Chamber detector (RPC) of HADES is based of self-made electronics making use of switching power techniques that provide the advantage of reaching high efficiencies at reduced space.

The power system consists of a distributed architecture: first, commercial AC-DC power supplies convert the 230AC mains into 48VDC. Then custom Low Voltage boards convert the 48VDC into the required low voltages (+6V, -6V and +4V) via isolated DC-DC switching modules. Filters for the two principal modes of conducted EMI propagation (differential and common mode) were mandatory at the input and output of the DC-DC modules to reduce the output noise. Galvanic isolation of the modules avoids ground loops, which is a usual source of common mode EMI. The layout of the PCB was carefully considered to reduce parasitic capacitance to ground and mutual coupling (to reduce electrically and magnetically generated EMI respectively). A shielding box connected to input ground is used to limit radiated emission. Ripple at the output of the DC-DC board is lower than 2mV, and noise levels for a bandwidth of 1Ghz is as low as 25mV.
Twisted pair cables without any shielding carry the low voltages to the frontend electronics which contains Low DropOut regulators (LDO) to provide stable voltages at the point of load and compensate for the different voltage drops due to various cable lengths. The control system is based on the 1-wire bus, that is used to provide monitoring of output currents and voltages, being the 1-wire bus controlled by an ETRAX single chip computer that sends the data through Ethernet via EPICs.

In summary The power supply system designed for the HADES RPC frontend electronics features high efficiency by using switching DC-DC converters. To avoid interferences with the frontend electronics, the supply voltage is filtered to provide very low noise levels, taking special care of the common mode noise. Experimental results for a full sector reveal the possibility of using such a power system without worsening the response of the frontend electronics, obtaining a time resolution for the frontend electronic of 50 ps.

**POSTERS SESSION / 10**

**Electronics of LHCb calorimeter monitoring system**

Anatoli Konoplyannikov

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All calorimeter sub-detectors in LHCb, the Scintillator Pad Detector (SPD), the Preshower detector (PS), the Electromagnetic Calorimeter (ECAL) and the Hadron Calorimeter (HCAL) are equipped with the Hamamatsu photomultiplier tubes (PMT) as devices for light to electrical signal conversion. The PMT gain behavior is not stable in a time, due to changes in the load current and due to ageing. The calorimeter light emitting diode (LED) monitoring system has been developed to monitor the PMT gain over time during data taking. Furthermore the system will play an important role during the detector commissioning and during LHC machine stops, in order to perform tests of the PMTs, cables and FE boards and measurements of relative time alignment.

The aim of the paper is to describe the LED monitoring system architecture, some technical details of the electronics implementation based on radiation tolerant components and to summarize the system performance.

**Summary:**

The main aim of the LHCb calorimeter light emitting diode (LED) monitoring system is to monitor the PMT gain in time of data taking with precision better than 0.5 %. The other important role of the system will be during the detector commissioning and testing in the LHC machine stops for PMT, cables and FE board tests and relative time alignment.

Each LED of the system illuminates up to 40 tubes and total amount of the monitoring channels is about 700.

The electronics of the LED monitoring system consists of three functional parts. The 700 LED drivers with PIN diode and amplifier are used for illuminating tubes and monitoring the LED stability itself. The light emitting diodes are different for each sub-detector and optimized for the individual detector requirements. A subsystem for the LED intensity control allows a variation of the LED intensity across a wide range for the PMT linearity measurements. This subsystem includes 40 electronic boards. A LED Triggering Signal Board (LEDTSB) (a 9U VME module) is performing the LED triggering pulse control and distribution. Twelve LEDTSB boards are used for precise time adjustment of the calibration signals with respect to the calibration trigger signal.

The calorimeter monitoring system is placed on the detector in a radiation hard environment. The electronics has been designed taking into account this factor.

Main characteristics of the monitoring system are mentioned below:

- Precision of the PMT gain monitoring is about 0.3 %.
- Individual time setting for each LED in range of 300 ns with 1 ns step.
- PIN diode with amplifier is used for monitoring the LED stability itself.
- Control Logic FPGA is placed on a mezzanine card and equipped with radiation hard ACTEL pro-ASIC chip APA300.
- Memory of the scanning algorithm FPGA with 64 patterns of the output trigger signals allows perform all needed sequences for LED flashing.
- The calorimeter monitoring system is linked to the LHCb ECS system by the SPECS serial bus (developed in LAL).
Last year the LHCb calorimeter monitoring system is intensively used for detector commissioning and
tested for getting the first data of this year.

**POWER WORKING GROUP / 163**

Enpiron radiation test results

Parallel session B2 - Optoelectronics / 59

**Evaluation of Multi-Gbps Optical Transceivers for Use in Future HEP Experiments**

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1 CERN

Future experiments at CERN will increase the demand for high-bandwidth optical links. Custom de-
velopments for deployment within the detector volumes will be based upon commercially available
transceivers.

We present our evaluation of commercial multi-Gbps optical transceivers and optoelectronic com-
ponents. This serves as the basis to evaluate the performance of the future Versatile Transceiver
that is being developed at CERN in the context of the Versatile Link project. We describe the experi-
mental set-up for parametric testing, the devices evaluated and our treatment of the performance
data.

Summary:

High Energy Physics (HEP) experiments, such as the ones currently undergoing commissioning at the
Large Hadron Collider (LHC), require tens of thousands of optical links each in order to extract raw data
from the detector and to distribute clock and control data to the front-end electronics. An upgrade of
the current LHC (super LHC or SLHC), planned for 2013-18, is expected to increase the luminosity by an
order of magnitude to 1035/cm2/s, which will require higher-speed optical links with better radiation
tolerance.

The Versatile Link project aims to propose both the architectures and the basic building blocks required
for the implementation of future optical links across the various SLHC experiments. One of the main
building blocks is a Versatile Transceiver (VTRx) for deployment on-detector that will be radiation hard
and multi-Gbps capable.

A crucial stage of the VTRx sub-project will be the evaluation and validation of the versatile transceiver
prototype modules. To accomplish this task we have set up a variety of test equipment, developed some
software tools and specified the evaluation criteria and test procedures.

To develop the test set-up and evaluate the current state of the art, we have evaluated several com-
mercial transceiver (TRx) modules from several families: SFP, XFP and SFP+. In the process, we have
established performance benchmarks to which the VTRx modules can now be compared. Due to its low
power consumption and high performance level we have chosen SFP+ devices as a basis for our custom
VTRx development. We have also built and tested transmitters using commercial drivers attached to
both off-the-shelf and custom lasers.

To evaluate TRx modules we have defined test points where it would be relevant to perform parametric
testing. There are two basic types of measurements that we have used to characterize a TRx module:
the eye diagram and the Bit Error Rate (BER) testing. To obtain the former we used a multi-Gbps data
source and a multi-GHz sampling scope with electrical and optical input modules. To obtain the latter
we used a multi-Gbps FPGA-based BER Tester (BERT).

The following signal information has been extracted from the eye diagrams: levels (average and dif-
fERENCE), Q-factor, rise and fall times and jitter components (random and deterministic). We have also
saved the raw data and performed off-line mask margin tests using custom masks. The BER test is a
link level measurement but we have used it to qualify the receiver part of a TRx module. By measuring
the BER for various attenuation levels of the input optical signal to the receiver, its sensitivity can be
Having gathered data from the parametric testing, these data must be compared so that a choice between devices can be made based on their respective test results. Since it is very difficult to accomplish this task by looking directly at all of the performance data together, we have introduced the concept of a Figure of Merit (FoM). We started by defining a set of minimum requirements and then constructed the FoM by calculating the relative distance between the measured parameters and the minimum requirements. The FoM concept has allowed us to clearly establish those commercial devices that are most suitable candidates for customization in order to turn them into Versatile Transceivers.

**Parallel session A2 - ASICs / 103**

**Evaluation of Two SiGe HBT Technologies for the ATLAS sLHC Upgrade**

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As previously reported, silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) technologies promise several advantages over CMOS for the ATLAS upgrade [8]. Since our last paper, we have evaluated the relative merits of the latest generations of SiGe HBT BiCMOS technologies, the 8WL and 8HP platforms. These 130nm SiGe technologies show promise to operate at lower power than CMOS technologies and would provide a viable alternative for the Silicon Strip Detector and Liquid Argon Calorimeter upgrades, provided that the radiation tolerance studies at multiple gamma, neutron, and proton irradiation levels included in this investigation show them to be sufficiently radiation tolerant.

**Summary:**

SiGe technologies are known for their high transconductance at low current. BiCMOS Silicon-germanium (SiGe) Heterojunction Bipolar Transistor (HBT) technologies are of interest for high luminosity applications in high energy physics because they have the benefit of requiring less power than standard CMOS technologies while still having low noise and fast shaping times even after exposure to high radiation levels [3]. Prototype readout circuits using SiGe HBT technologies are currently planned for submission later this year. The prototype circuits are designed for use in the upgrade of the Silicon Strip Detector and Liquid Argon Calorimeter of the ATLAS detector as part of the Large Hadron Collider upgrade (sLHC) [1][2]. In these applications, power consumption is a critical parameter, which must be minimized. These preliminary circuit designs have been used to guide the assessment of relevant device parameters. The design of a low noise amp (LNA) with SiGe 8WL and 8HP technologies will be briefly discussed.

The intent of this investigation is to assess the relative radiation hardness of the 8WL and the 8HP SiGe platforms. This is a follow up to a previous paper from this 2005 conference where only preliminary results were presented [8]. Previous SiGe generations have already been reported to be quite radiation tolerant up to a high dose, showing post-radiation current gains well above workable limits [4-6]. Compared to 8HP, 8WL is a lower cost option, with 100 GHz peak IT versus 200 GHz for 8HP, and has reduced...
depth deep trench isolation, a thinner, implanted subcollector, and a higher resistivity substrate. Both are available with a 150nm CMOS technology to provide high-speed BiCMOS ASIC solutions.

This radiation study envelopes the predicted target radiation levels that will be reached at 60 and 20 cm radii in the upgraded ATLAS detector. For the inner most silicon strip detector we predict a 25 Mrad total ionizing dose (TID) and a total 1-MeV neutron fluence of 1.0x10^15 neutrons/cm^2, while the radiation levels for the liquid argon calorimeter are expected to be lower by more than an order of magnitude.

We investigated both ionization damage and displacement damage in with the use of gamma, neutron, and proton irradiations [8]. By comparing the effects of the various radiation sources, the two principal mechanisms behind the radiation damage can be differentiated [7]. In looking at these different mechanisms of the radiation damage, this investigation presents a breakdown of the effects of bias on SiGe technologies during proton and gamma irradiation. Variations in the effectiveness of bias in SiGe technologies during irradiation are briefly presented. Additionally, the effects of hard neutrons vs. thermal neutrons in SiGe technologies by use of cadmium shielding are also presented. This has potential effects on the need for thermal neutron shielding when using SiGe technologies in the ATLAS upgrade.


POSTERS SESSION / 115

Evaluation of high-speed single fiber communication using Wavelength Division Multiplexing.

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There are many reasons for keeping the number of communication fibers in a data acquisition system to a minimum. We are therefore evaluating different schemes for using Wavelength Division Multiplexing (WDM) techniques. WDM is a useful tool for achieving high data bandwidths when up scaling current systems and to allow fiber sharing between multiple data sources. Different strategies such as single fiber single wavelength (SFSW), diplex transceivers and modulation using off board laser sources are investigated.
While the primary target is related to the ATLAS upgrade, the work can also have more general applications. Key concepts are cost, size, ruggedness and scalability.

Summary:

The present TileCal digitizer system in ATLAS comprises 256 drawers with up to 8 quasi-independent digitizer boards per drawer. A patch panel at the end of the drawers is the only access point for power and communication. The current digitizers preprocess the data and send only accepted events off the detector. The maximum readout bandwidth is 80 Mbps per board, transmitted over a single fiber per drawer.

In the maximal SLHC upgrade scenario, calorimeter data for every bunch crossing would be read out, increasing the bandwidth of the digitizer system by a factor of 60 to up to 50 Gb/s per drawer. It would be advantageous to use the existing fiber plant to avoid laying new fibers. This could be achieved using Wavelength Division Multiplexing (WDM) technology. Using WDM will also open up for high speed duplex communication over a single fiber, either by using diplex electro-optical modules, Single Fiber Single Wavelength (SFSW) modules or standard passive WDM multiplexers.

Four options are being evaluated for the ATLAS TileCal digitizer application using WDM. The first option is to use standard lasers with the same wavelength on all boards. This scheme is less expensive than the other options, but requires an electro-optical/opto-electrical interface card at the patch panel to produce the different wavelengths for the WDM output.

The second option is to use lasers with fixed but different wavelengths for each board. This would only need a passive WDM MUX module at the patch panel, but the replaced boards must have a laser wavelength matching the originals. Using pluggable lasers (XFP standard) solves this, but pluggable lasers are more susceptible to poor environmental conditions, and may not be the best choice for the TileCal application.

The third option is to use tunable lasers on the boards and a passive WDM MUX at the patch panel. Here, boards can be replaced without regard to wavelength order. Tuneable lasers with sufficient speed are currently expensive, as they are just beginning to become available. As prices go down, though, they present us with a flexible upgrade path with a wide range of use.

The fourth option is to feed the digitizers with an off board laser source and use modulation techniques. This saves on PCB complexity inside the drawer but introduces more fiber connectivity points. Using 16 (or 32 for redundancy) signals, half is used as feeds and the other half for output. Since reflections and crosstalk are significant in this solution, the topology is critical when attempting to achieve single fiber operation.

Executive Summary

Francois Vasey

1 CERN

Parallel session B2 - Optoelectronics / 21

Experiences with the ATLAS Pixel Detector Optolink and researches for future links

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The ATLAS Pixel optical link connects the readout electronic in the counting room and the active detector elements. After installation the link has been commissioned and tuned. Tests for optical and electrical functionality of components sorted out failures on the off-detector side and had the system more than 99% functional after installation.

For optical links in future detectors in higher radiation environments thermal effects in laser-diodes become essential and have to be understood. A research program to study thermal properties and its consequences will be discussed and is performed in the context of the Joined ATLAS/CMS activities.

Summary:

The ATLAS Pixel detector package is connected with it’s off-detector readout and control system via an optical link. This optolink consists of an optoboard on-detector, containing receiving and transmitting optical and electrical components. 80m of both, radiation hard and radiation tolerant, fibre connect this optoboard with an optical interface off-detector, the Back-of-Crate card.

All optical components ran through production testing before installation into the pixel package respectively the off-detector readout crates. Before final installation, the Pixel package was fully tested and qualified. The same qualification was done after installation and showed new failures which are mostly located outside the package itself in the off-detector readout hardware.

These faulty off-detector optical components needed replacement even though previous tests passed and their failure is still under investigation. Failure modes of the optical link as well as methods to find those faulty links are to be shown.

All functional detector components are signed off with a functional optical link and were tested for data transmission. During calibration of the detector, various features of the optical link (delays, duty cycle correction) are to be tested, which are meant to increase physical performance. These are not critical for general functionality of the Pixel detector and thus were not part of the link qualification. Methods to set up parameters of the optical link to retrieve ideal functionality are to be shown during this presentation, as is for problems during tuning and how to resolve these with a change of concepts for the future.

To step into the development of future optical links a research program to study laser diodes which serve a higher bandwidth and withstand a higher radiation environment. A measurement to determine material properties like the thermal resistance is set up. Thermal effects become nearly as important as irradiation damages inside the material when looking at the radiation tolerance of semiconductor laser diodes.

Heat effects inside the laser diodes affect the laser output power in the same order as the irradiation itself. The better the heat can leave the diode the longer the laser can work and the more radiation can be tolerated. The thermal resistance has to be measured for the pure laser diode and also for the laser package to be able adopt mounting and the heat sink optimal.

To characterize the laser diodes foreseen for new detectors a setup to measure the output wavelength of the lasers in dependence of the junction temperature is used. With this the thermal resistance of the laser diode can be determined.

The setup has been realized for CMS tracker studies and will now be used for testing new lasers for SLHC. The CMS setup at CERN serves as basis and reference setup, while a new setup is built in Wuppertal optimizing some components. The laser characterization is done in context of the Joined ATLAS / CMS Optogroups work.

**POSTERS SESSION / 108**

**FPGA Implementation of Optimal Filtering Algorithm for Tile-Cal ROD System**

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Traditionally, Optimal Filtering Algorithm has been implemented using general purpose programmable DSP chips. Alternatively, new FPGAs provide a highly adaptable and flexible system to develop this algorithm.

TileCal ROD is a multi-channel system, where similar data arrives at very high sampling rates and is subject to simultaneous tasks. It include different FPGAs with high I/O and with parallel structures that provide a benefit at a data analysis.

The Optical Multiplexer Board is one of the elements presents in TileCal ROD System. It has Cyclone devices that present an ideal platform for implementing Optimal Filtering Algorithm. Actually this algorithm is performing in the DSPs included at ROD Motherboard.

This work presents an alternative to implement Optimal Filtering Algorithm.

**Summary:**

Digital Signal Processor (DSP) is actually the main component in the TileCal Read-Out Driver (ROD) System. The DSPs are responsible for data reconstruction in real time at the ATLAS first level trigger rate (100 KHz). The DSP has to compute energy, phase and Quality Factor (QF) for all the channels in less than 10 μs at the ATLAS maximum rate and send the reconstructed data to the second trigger level.

The Optimal Filtering (OF) Algorithm reconstructs the amplitude and phase of a digitized signal by a linear combination of its digitized samples, pedestal subtracted. DSPs executes OF Algorithms in real time.

To reduce data loss due to radiation effects, the TileCal collaboration decided to include data redundancy in the output links of the FrontEnd. This was accomplished using two optical fibres which transmit the same data. For this purpose a new module, called Optical Multiplexer Board (OMB) was conceived. This board would be able to provide, in case of error in one link, the correct data to the ROD input by analyzing the Cyclic Redundancy Codes (CRC) of the data packets on both fibers coming from the FEB. OMB has Cyclone devices that provide an ideal platform for implementing low-cost digital signal processing (DSP) systems on an FPGA. Cyclone devices present a flexible hardware solution in which we can implement an Optimal Filtering Algorithm.

This work presents an alternative to implement Optimal Filtering Algorithm.

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**FPGAs in 2008 and Beyond**

Peter Alfke

1. Xilinx, Inc

Since 90 nm, Moore’s Law offers diminishing performance increase, requires architectural changes:

- Bigger LUTs, dedicated hard cores, microprocessors and transceivers.
- Virtex-5 had excellent start in 2007
- In 2008: Virtex-5 FXT.
- PPC440 with attached 5 x 2 Crossbar for performance and flexibility.
- GTX Transceivers achieve 6.5 Gbps data throughput.

After 2008 through 2013:

- 45 nm followed by 32 nm technology.
- More transistors and lower cost per function. (average 10% per year, or factor 10 every 7 years)
- Capacity limited by die size
- Performance limited by power and heat budget.
- Various effects and trade-offs are discussed.

**Summary:**
Below 90 nm, Moore’s Law no longer gives higher speed for free. Most performance improvement must come from architecture: 6-input LUTs, better memory, hard cores for Ethernet, PCIe, Gigabit transceivers, embedded microprocessors.

Virtex-5 had an excellent start in 2007, and still has no serious competition in its field. New in 2008 is Virtex-5FXT with PPC440 microprocessor(s) plus up to 48 faster transceivers.

PPC440 is not only faster than its PPC405 predecessor was in Virtex-4, it is also more flexible and far more efficient thanks to an embedded 5x2 Crossbar which supports two simultaneous transfers over 128-bit wide channels.

The PPC440 also has an Auxiliary Processor Unit Port for attaching a co-processor, e.g. a floating point unit. Xilinx offers a soft core that supports IEEE single- and double-precision floating point operation, and is between 6 and 28 times faster than running software on the PPC440, or 3 times faster than an equivalent co-processor solution running on the Virtex-4.

Virtex-5 FXT and ‘TXT devices offer up to 48 Transceivers with improved features and higher data rate. Wide frequency range, 150 Mbps to 6.5 Gbps, at only 200 mW per channel.

Each transmitter offers programmable pre-emphasis, while each receiver has analog equalization and digital multi-tap Decision Feedback Equalization (DFE). The receiver can handle up to 150 consecutive 1s or 0s without losing lock, but also supports 8B/10B, 64B/66B and Interlaken protocol.

2009 to 2013

45 nm technology, followed by 32 nm

Moore’s Law is still alive, offering more transistors and lower cost per function (average 10% per year, or a factor 10 every 7 years)

But raw transistor speed will become more difficult to improve, and supply voltage scaling reaches its limits.

Chip capacity will grow, since it is determined by the ratio of die size to feature size.

System performance will mainly be limited by the power and heat budget.

Issues:

Need for alternative technologies optimized for either performance of power, not both. Limited power budgets: 2 W max for cell-phones, due to heat, even if there will be better batteries.

As feature size shrinks, manufacturing spread becomes a bigger issue, affecting yield. Increase in logic density might outstrip pin-count (presently at around 1200). High demands on long-term reliability can preclude experimentation with new device materials and exotic processing.

Higher design productivity.

Users’ design time may become a limitation. Design re-use becomes more important. Place-and-route times must remain acceptable, need for incremental compile and block-based design. Learn to utilize multi-core computers.

The Future:

As systems get more complex, and their product lifetime decreases, FPGAs become an ever more attractive solution.

Parallel Session B3 - Machine-Experiment, BCM / 54

Fast Beam Conditions Monitoring (BCM1F) for CMS.

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The CMS Beam Conditions and Radiation Monitoring System (BRM) is composed of different subsystems that perform monitoring of, as well as providing the CMS detector protection from, adverse beam conditions inside and around the CMS experiment. This paper presents the Fast Beam Conditions Monitoring subsystem (BCM1F), which is designed for fast flux monitoring based on bunch by bunch measurements of both beam halo and collision product contributions from the LHC beam. The BCM1F is located inside the CMS pixel detector volume close to the beam-pipe and provides real-time information. The detector uses scVD (single-crystal Chemical Vapor Deposition) diamond sensors and radiation hard front-end electronics, along with an analog optical readout of the signals.

POSTERS SESSION / 37

Fast FPGA-based trigger and data acquisition system for the CERN experiment NA62: architecture and algorithms

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We present the design of the trigger and DAQ system for NA62, with emphasis to the first level of trigger (L0).

The L0 level runs on-line and is designed as a segment of the DAQ chain. FPGAs are used to evaluate fast trigger conditions, entirely on the digitized information from read-out electronics.

In this way, the whole digitized information from detector is available for triggering and no separate branches of read-out electronics are necessary.

We shall present our design for the L0 architecture, the implementation of trigger conditions on the FPGAs, the hardware we developed and tests.

Summary:

Here we present the design of the trigger and DAQ system for NA62, with emphasis to the first level of trigger (L0).

NA62 is an experiment hosted at CERN, which aims to measure the branching fraction of the ultra-rare K+ → π+μν̅ decay (expected at order of 10^{-10}).

The trigger is organized in three levels, performing a data bandwidth reduction from an overall size of 1-2 TB/s produced by continuous digitization of detector hits, down to few tens of KB/s for permanent mass storage.

The L0 level of trigger runs on-line and is designed as a segment of the DAQ chain, where the evaluation of fast trigger conditions is performed entirely on the digitized information from read-out electronics.

In this way, the whole digitized information from detector is available for triggering and no separate branches of read-out electronics are necessary (as usual in this kind of experiments).

This feature has relevant impact on trigger control, flexibility and cost effectiveness, that will be addressed in the presentation.

The L0 level is implemented in hardware (further levels in software) within a set of TELL1 boards, the same used for a common trigger and read-out data flow in the LHCb experiment.

Mezzanine cards containing high performance TDCs plugged in the TELL1 process discriminated detector signals and provide the internal TELL1 FPGAs with digitized hit times. This information is used to evaluate fast trigger conditions within the FPGAs.

We shall present our design for the L0 architecture, the implementation of trigger conditions on the FPGAs, the hardware we developed and tests.
Fast transient recorder for spectroscopy experiments

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Many experiments in physics with high data rates, short analog signal pulses (40ns), fast rising edges and large dynamic ranges require transient recorders with very high resolution. Additionally double pulses can occur on many spectroscopy experiments, like the COMPASS recoil proton detector. These pulses are recorded and separated by numerical digital processes to extract time and amplitude information and used to create a trigger signal.

To meet these challenging requirements the so-called GANDALF transient recorder has been developed with a resolution of 12bit at 1Gsps. Extended with additional memories this module is not only a dead time free readout system but also has huge numerical capabilities provided by the implementation of a Virtex5SXT FPGA to solve challenges for double pulse separation and timing resolution in the sub-nanosecond range.

Summary:
Development of a fast transient recorder for spectroscopy experiments with high resolution of 12bit at 1 Gsps and huge numerical capabilities.

OPTO ELECTRONICS WORKING GROUP / 171

Fibre Irradiation Tests Results of Oxford and SMU

Parallel session B1 - Trigger 1 / 68

First results on the performance of the CMS Global Calorimeter Trigger

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The CMS Global Calorimeter Trigger (GCT) has been designed, manufactured and commissioned on a short time schedule of approximately two years. The GCT system has gone through extensive testing on the bench and in-situ and its performance is well understood. This paper describes problems encountered during the project, the solutions to them and possible lessons for future designs, particularly for high speed serial links. The input links have been upgraded from 1.6Gb/s synchronous links to 2.0Gb/s asynchronous links. The existing output links to the Global Trigger (GT) are being replaced. The design for a low latency, high speed serial interface between the GCT and GT, based upon a Xilinx Virtex 5 FPGA is presented.

Summary:
This paper is devoted to the challenges faced and lessons learnt during the development and commissioning of the GCT system and refer to the architecture of the design and the implementations of high speed serial links. Both are likely to be used in future systems and are of value to the larger LHC trigger community.

The main challenge with the GCT and with most trigger systems is the high bandwidth requirements coupled with the fact that data often needs to be shared or duplicated, and done so with low latency.
The GCT uses a mixture of high speed serial links and wide parallel busses. The high speed serial links are necessary to concentrate the data into a single FPGA, thus reducing data sharing requirements and making the processing efficient. The latency cost of these links is not negligible and thus wide parallel busses operating conservatively at 80MHz are used for the rest of the system.

The GCT is modular, which allowed multiple design teams to work in parallel in the initial stages of the product. It also simplified each board, thus reducing the layout and design time. It has also allowed the GCT-to-GT links to be replaced without requiring complex changes to the main 9U VME data processing card.

The revised GCT was originally designed to accommodate the existing interfaces to the GT and RCT:

The original GCT-to-GT interface was based on National Semiconductor DS92LV16 electrical high speed serial links operating just beyond specification. In the revised GCT design these links were placed on a dual CMC daughter card. The interface was successfully tested. However, when new shorter cables were used for the GCT-to-GT links it was noticed that the SERDES links occasionally lost lock. This was traced to reflections from the receiver. A new interface is being built based on the Virtex 5 FPGA and 16 bidirectional optical links operating up to 3.2Gb/s.

The GCT input interface with the Regional Calorimeter Trigger (RCT) consists of 63 Source Cards which transmit the RCT data using high speed optical links to the 8 Leaf Cards of the GCT. The source cards convert the parallel differential ECL from the RCT to high speed serial optical signals with 8B/10B encoding and a CRC check per orbit. During commissioning it was noted that occasionally one of the links on the Leaf card was generating CRC errors. The original hypothesis was that this was due to the quality of the clock used to drive the SERDES signals, which was close to the specification limit.

The system continues to operate in this way which has the benefit that we can use a very low jitter clock source and the latency is not affected because the increase in latency due to the clock domain bridge on the Source card is cancelled by the internal logic in the SERDES units operating faster.

Plenary Session 1 - OPENING / 144

Greek Contribution to the ATLAS experiment

Christine Kourkoumelis¹

¹ University of Athens

The Greek contribution to the construction and commissioning of the ATLAS Muon spectrometer will be reviewed. In addition, the physics studies, leading to lepton final states, performed by the Greek Groups will be summarized.

POSTERS SESSION / 96

Grounding, Shielding and Cooling Issues on LHCb electronics at the LHC pit 8.

Author(s): Daniel Lacarrere¹

Co-author(s): Dirk Wiedner ¹ ; Eric Thomas ¹ ; Gloria Corti ¹ ; Jorgen Christiansen ¹ ; Laurent Roy ¹ ; Rolf Lindner ¹ ; Vincent Bobillier ¹

¹ CERN
The grounding, shielding and cooling issues are important factors in the design and the maintenance of all the electronics systems. Inadequate grounding, shielding or cooling can lead to unreliable operation of the sub-detectors. This paper provides an overview on the LHCb strategy and achievements in the field of grounding, shielding and cooling for the electronics equipments.

Summary:
The LHCb detector is designed to study the CP violation in the B-mesons at the LHC collider. The installation of the experiment was completed in June 2008, ready for data taking in July 08 as scheduled. The experimental cavern (ex-DELPHI at LEP) 100 m underground at pit 8 has been divided in two areas. The detector area (UXB) is separated from the protected area (UXA) by a radiation shielding wall of 3200 t of concrete. The UXA area is essentially dedicated to the non-radiation tolerant electronics, CPUs farm & detector control systems. This area is always accessible when the LHC operates. The grounding, shielding and cooling issues are important factors in the design and the maintenance of all the electronics systems. Inadequate grounding, shielding or cooling can lead to unreliable operation of the sub-detectors. This paper provides an overview on the LHCb strategy and achievements in the field of grounding, shielding and cooling for the electronics equipments. Practical details are also reported.

POSTERS SESSION / 3

High-Resolution Time-to-Digital Converter in Field Programmable Gate Array

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Two high-resolution time-interval measuring system implemented in a SRAM-based FPGA device are presented. The two methods ought to be used for time interpolation within the system clock cycle. We designed and built a PCB hosting a Virtex-5 Xilinx FPGA and high stability oscillators to test the two different architectures. In the first method, dedicated carry lines are used to perform fine time measurement, while in the second one a differential tapped delay line is used. In this paper we compare the two architectures and show their performance in terms of stability and resolution.

Summary:
High-resolution Time-to-Digital Converters are often required in many applications in high-energy and nuclear physics. Furthermore, they are widely used in many scientific equipments such as Time-Of-Flight (TOF) spectrometers and distance measurements. Different configurations of tapped delay lines are widely used to measure sub-nanosecond time intervals both in ASIC and FPGA devices. However, the design process of an ASIC device can be expensive, especially if produced in small quantities, while FPGAs lower the development cost and offer more design flexibility. In 1997, Kalisz et al. [1] proposed an FPGA-based approach: their design used a variation of conventional delay line and offered a time resolution of 200 ps. In 2000 [2], rapid progress in electronics technology allowed them to achieve a time resolution of 100 ps. It should be noted that the above used FPGA devices were one-time programmable so that each iteration involved the utilization of a new device. By using SRAM-based FPGAs, the user benefits from the in-system-programming (ISP) and reconfiguration features. Resolution values between 50 ps and 500 ps have been achieved with this technology [3]. Two different digital delay line circuits have been designed and tested by the authors thus far [4]. We designed and built a PCB hosting a Virtex-5 FPGA from Xilinx [5] to test the two different TDC architectures. Two high stability oscillators from Valpey-Fisher have been installed in order to compare their performance side by side. Test points for high-bandwidth active probes are used to perform the Virtex-5 clock signal characterization. They are placed just near the FPGA, making the shortest distance for the device output signals. SMA connectors are used to send the START and STOP signals to the board. They may adopt differential lines or single ended signaling schemes.
Both approaches of the two architectures use the classic Nutt method [6] based on the two stage interpolation. The time interval \( T \) to be measured is decomposed into three intervals:
- the integer number \( N \) of the reference clock periods \( T_c \) is measured by a binary counter;
- two short intervals \( \Delta t_1 \) and \( \Delta t_2 \) at the initial and final part of the measured interval, each having a duration within one clock period.

The fine time measurement of the short time intervals have been performed in two different methods. The delay elements exploit either general purpose resources, like logic element, or special purpose resources, like dedicated carry logic. The first architecture uses carry chain delays, while in the second one a differential tapped delay line is used. The main design problem was the implementation of the delay line by using the logic cells offered by the FPGA technology. In order to assure the uniformity of the propagation delays, the cells have been placed and routed by hand.

In this paper, we describe the implementation and characterization of the two different fine TDC. The behaviour of the two architectures is compared and we show their performance in terms of stability and resolution.

References:


**POSTERS SESSION / 2**

**Implementation of the control and supervision of ALICE ZDC positioning systems**

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**Co-author(s):** Thorsten Gallmeister ¹

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The ALICE Zero Degree Calorimeters (ZDC) have been installed to either side of the LHC IP2 in the machine tunnel next to the dipole magnet D2. The calorimeter modules are mounted on a special table equipped with a mechanism to lower the modules away from the beam orbit during injection and acceleration. During stable operation the modules can be raised individually to be aligned with the beam orbit. The horizontal clearance between ZDC modules and beam pipe will be only about 3 mm. Anti-collision switches are therefore installed to protect the beam pipes against accidental damage. The movement of the calorimeter modules and the protection switches are remote controlled by the ALICE ZDC positioning system.
Incremental Firmware Development and Partial Reconfiguration in the Xilinx Virtex-5

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The size and complexity of the latest generations of FPGAs has increased dramatically. This in turn means that the time taken to develop and build even small firmware projects is increasing exponentially. Pre-constrained logic placement and routing is becoming critically important for the use of specialized components in the FPGA such as serial link interfaces. This necessitates significant changes from ‘normal’ firmware tool flows in order to effectively develop systems based on these devices. In this paper we discuss several methods for improving turnaround speed and design safety, including: pre-placed and pre-routed hard macros / RPMs, pre-synthesised black-box netlists, and incremental synthesis, place and route. Possible methods of dynamic partial reconfiguration are also discussed in this context.

Summary:

The current CMS trigger and DAQ electronics is based on FPGA and processor technology several generations behind the currently commercially-available devices. Most systems in CMS are based on either the Xilinx Virtex-II or the Xilinx Virtex-II Pro (and similar Altera-made FPGAs). Since then Xilinx has developed the Virtex-4 and Virtex-5, scaling in feature size from 250nm to 65nm and incorporating many new hardware features such as Digital Signal Processing (DSP) cores, tri-mode Gigabit Ethernet (GbE) MACs and PCI express (PCIe) endpoints amongst others. Furthermore, total logic capacity has increased approximately ten-fold with a corresponding increase in maximum clock speed.

However this creates a new problem: FPGA firmware synthesis and routing is an extremely computationally-intensive process. Given the arrangement of logic and routing in the devices and the scaling of feature size in deep submicron technology, the complexity of logic placement and routing is increasing at a greater-than-geometric rate. Without the development of new firmware development techniques to manage this increase in complexity, firmware build times can increase from minutes to hours and even days.

In order to avoid these problems we have been investigating the incorporation of pre-synthesised and pre-placed/ routed modules (known as ‘black box’ modules, ‘hard macros’ or ‘relationally-placed macros’, depending on their construction) into a larger design. In addition we discuss the use of incremental synthesis, placement and routing, which rely on the use of a previously build design as a ‘guide’ for the next build. The benefits and difficulties of these various approaches are discussed.

Finally we discuss the application of these approaches in the concept of dynamic partial reconfiguration, which relies on the use of a ‘static’ module within a larger variable design, which allows internal reconfiguration of a device without disrupting the state of the module being used to provide general configuration and communication to the FPGA.

POSTERS SESSION / 43

Infrastructures and monitoring of the on-line CMS computing center

Attila RACZ

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This paper describes in detail the infrastructures/installation of the CMS on-line computing center (CMSCC) and its associated monitoring system. In summer 2007, 640 readout Units/builder Units have been deployed along with ~150 servers for...
DAQ general services. Since summer 2008, ~500 filter units have been added and today, the CMSCC has an on-line processing capability sufficient for a LV1A trigger rate of 50 kHz. To ensure that these ~1300 servers are performing the tasks we expect from them, a multi-level monitoring system has been put in place. This system is also described in this paper.

Summary:

The on-line CMS computing center, located at the surface of the experimental site, performs the event assembly (640 event fragments produced by the detector are assembled into a single event of ~1MB) and subsequently, executes the high level trigger algorithms (HLTs) in order to select the events to be stored for later off-line analysis. The heavy infrastructures (false floor, water ducts, racks, power rails) were installed in years 2005 and 2006. The cabling for the first batch of 800 servers (event builder PCs) started early 2007. The event builder PCs have been installed and commissioned in summer 2007. They are acting also as event analyzers as long as the data volume does not require dedicated PCs to run the HLT algorithms. About 500 servers for data analysis have been installed this summer in view of the LHC startup. Additional 1500 servers are foreseen for 2009 to reach the full processing power. The monitoring system is watching the servers at different levels: the first level is dealing with physical parameters (voltages, temperatures, fans) and maintenance/repair actions. The second level is monitoring the services provided by each server (ssh, tcp, presence of drivers, etc). The third level is looking at the application performances. Data retrieved by the three levels of monitoring are stored in a database.

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Installation and Commissioning of the ATLAS LAr Read-Out Electronics

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The cryostats of the ATLAS LAr calorimeter system are installed in the ATLAS cavern since several years. Following this, an effort to install and commission the front end read-out electronics (infrastructure, crates, boards) has been ongoing and is finished now, in time for the cavern closure.

Following cautious procedures and with continuous testing-campaigns of the electronics at each step of the installation advancement, the result is a fully commissioned calorimeter with its readout and a small number of non-functional channels. A total of only 0.017% of the read out channels is dead and 0.4% need special treatment for calibration. The presentation will give a general overview of the installation and refurbishment campaign of the ATLAS LAr calorimeter electronics and show results of the calibration runs that were taken continuously during the various phases of commissioning. Different problems observed and addressed will be discussed. It will describe noise studies that have been performed and shortly review the solutions implemented to reduce noise. The excellent stability of the calorimeter readout will be demonstrated by showing results from pedestal and pulse height studies.
Installation, Commissioning and Performance of the CMS Electromagnetic Calorimeter Electronics

Nicolo Cartiglia

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This talk reviews the CMS high resolution electromagnetic calorimeter (ECAL) on- and off-detector electronics and its commissioning within CMS in-situ. In particular it presents results on electronics noise, monitoring, dead channels and performance, together with the experience gained during installation. The talk will also include results from the first months of ECAL operation during the commissioning of LHC.

Instrumentation for Gate Current Noise Measurements on sub-100 nm MOS Transistors

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This work describes a laboratory instrument that was developed to characterize the gate current noise performances of CMOS devices with minimum feature size in the 100 nm span. As a consequence of the reduction of the gate oxide thickness, these devices are affected by a non-negligible gate current due to direct tunneling phenomena. In this paper, the analysis of this noise contribution is particularly aimed at evaluating the resolution limits of readout circuits that will be used in future high energy physics (HEP) experiments. The noise measuring instrument and some of the results of gate current noise characterization will be presented.

Summary:

In the last decade, the requirements of high granularity in the design of the readout electronics for HEP experiments have led to an extensive use of deep-submicron CMOS devices. While approaching the 100 nm span, the CMOS technology has entered the sub-3 nm gate oxide thickness regime. In such a regime, MOSFET devices exhibit a non-negligible gate-leakage current, due to the finite probability of electrons directly tunneling through the insulating SiO2 layer. This current contribution, which originates from discrete charges randomly crossing a potential barrier, is affected by noise fluctuations which may degrade circuit performance in analog applications.

In particular, in detector readout circuits integrated in sub-100 nm CMOS technologies, the resolution, which is limited by the noise from the input transistor, may be degraded by the parallel noise source in the device gate current. In order to evaluate the effects of this noise contribution, and also to supply suitable design criteria, accurate characterization and modeling of gate current noise are mandatory.

The noise characterization is carried out by means of a purposely developed instrument with the required accuracy in an adequate frequency range, considering the dependence of the gate current from device geometry and bias conditions. This measuring instrument consists mainly of a transimpedance stage amplifying the noise due to the gate-leakage current, which is detected by a commercial spectrum analyzer. The constraint for the minimum detectable noise is essentially dictated by the noise of the amplifier and its feedback resistor: the value of such a component has been chosen as a compromise between accuracy and bandwidth of the measuring system. As a consequence, it was possible to carry out measurements from 1 Hz up to 100 kHz. Nevertheless, such a bandwidth allows us to fully characterize the gate current noise, which exhibits white, 1/f and Lorentian-like behavior in this frequency range.
After presenting the details of the interface circuit design, the setup and procedures for gate noise measurement, results relevant to transistors belonging to a 90 nm technology will be also presented and discussed.

The last part of this work will be devoted to evaluating the impact of gate current noise on the equivalent noise charge (ENC) performance of front-end circuit, especially at long (> 100 ns) shaping times, where such a contribution may become an issue.

POWER WORKING GROUP / 158

Introduction

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LLRF electronics for the CNAO synchrotron

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The Italian National Centre for Oncological hAdrontherapy (CNAO) is undergoing its final construction phase in Pavia and will use proton and carbon ion beams to treat patients affected by solid tumors. At the heart of CNAO is a 78 meters circumference synchrotron, capable of accelerating particle up to 400 MeV/u with a repetition rate of 0.4 Hz. Particle acceleration is done by a unique VITROVAC load RF cavity operating at a frequency between 0.3 and 3MHz and up to 3kV peak amplitude. This paper describes the Low Level RF electronics developed for this synchrotron.

Summary:

A complete digital LLRF system has been designed at LPSC in order to control the CNAO accelerating cavity. The two main tasks of the electronics, cavity control and beam control, are assigned to two independent dedicated Digital Signal Processors (DSP). A Field Programmable Gate Array is managing digital I/Os, ADCs readout, memory access and is performing fast digital signal processing tasks such as I/Q demodulation of the cavity and beam pickup signals.

The RF cavity frequency is generated by a Direct Digital Synthesizer (DDS) which amplitude is digitally controlled by a logarithmic amplifier. Two other DDS are used for the generation of a sampling clock (sixteen time the cavity frequency) and a general purpose external synchronization signal (variable phase).

The LLRF electronics is connected to the CNAO control-command system thanks to 5 high speed serial links in order to transfer acceleration cycle parameters (Frequency, Amplitude, Cavity tuning current, beam position, etc ...). A slow control interface is also provided thanks to an Ethernet microcontroller board developed at LPSC. This Ethernet slow control link is used for in situ DSP programming and FPGA configuration. It also provides access to the parameter tables of the beam and cavity DSP and enable data retrieval of the embedded data acquisition system that stores all input and output signals during a given acceleration cycle.

Although specifically designed for the CNAO synchrotron, the versatility of the architecture and the fact that the board can be remotely configured and programmed very easily make it usable on different accelerators. First tests of the beam control ability of the system have thus been done on the PS Booster at CERN and will be presented on this paper in addition to electronics architecture, lab measurements and test results on the CNAO cavity.

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Lessons from LHC
Twenty years ago the embryonic LHC Collaborations were trying to understand how to do experiments at the next generation of proton colliders. In particular, the electronics communities were faced with a number of difficult problems. Some problems were associated with the choice of technologies, some with adapting emerging technologies to the Particle physics environment, and some were associated with engineering very complex systems with limited resources. This year, the electronics systems that were engineered for the LHC experiments have been successfully commissioned, and the community has started to contemplate the challenges of upgrading some of these systems for Super LHC (SLHC). It is timely to reflect on what has has been learned from the engineering the LHC electronics systems and to consider possible future improvements.

Parallel Session A6 - Trigger2 / 8

Level-3 Calorimeter Resolutions Available for the Level-1 and Level-2 CDF Triggers.

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As the Tevatron luminosity increases more sophisticated selections are required to be efficient in selecting rare events from a very huge background. To cope with this problem, CDF has pushed the level 3 calorimeter algorithm resolutions up to Level 2 and, when possible, even at Level 1, increasing efficiency and, at the same time, keeping under control the rates. This strategy increases the purity of the Level 2 and Level 1 samples, produces free-bandwidth that allows to reduce the thresholds. The global effect is an increase of the signal efficiency on important Tevatron Standard Model Higgs search channels (H -> WW, HZ, HW).

The L2 upgrade improves the cluster finding algorithm, the resolution of the Missing Transverse Energy (MET) and the SUM Transverse Energy (SUMET) calculations. The same Level 2 MET and SUMET improved resolution has been made available to the Level 1 system, exploiting the same hardware used for the Level 2 upgrade.

The upgrade is based on the Pulsar board [1], a general purpose VME board developed at CDF and already used for upgrading both the Level 2 tracking and the Level 2 global decision crate [2]. The Level 2 upgrade has been designed, built, tested and commissioned in six months. It was accepted as the default system for CDF in August 2007.

The same Level 2 hardware can be used in such a way to provide the Level 1 calorimeter system of the same MET, SUMET resolution provided to Level 2. While in the upgraded Level 2 system the algorithms are executed in a commercial CPU within the typical Level 2 processing timing of 20 us, in the upgraded Level 1 system, MET and SUMET are calculated by powerful FPGAs[3] within 5 us. The Level 1 upgrade is currently ongoing and in commissioning phase.

We describe the CDF Level 2, Level 1 calorimeter upgrades, the architecture and the trigger performances, with particular emphasis on a new calorimeter MET_JET-based trigger performances used for CDF Higgs search.

Summary:

At Level 2 an array of 23 Pulsars organized into 3 different levels, merge all the calorimeter trigger towers inside a CPU where the Level 2 reconstruction is executed. The Pulsar boards receive data, over 288 LVDS cables, well before the Level 1 accept decision. The events are synchronized with the Level 1 decision inside the 18 first level Pulsars, so that only events accepted at Level 1 are allowed to go ahead along the Pulsar tree. The FPGA occupancy due to the Level 2 computation is very low.
so that we could easily implement the MET and SUMET calculation exploiting the extra FPGA logic. This calculation is executed at the full Level 1 input rate. A partial computation is executed on each first level Pulsar board and finally sent to a single extra Level 1 Pulsar that refines the final MET and SUMET values, compares to the trigger threshold and sends the decision to the global Level 1 logic.

Bibliography


POSTERS SESSION / 119

Low Power Multi_dynamics Front End for the Optical Module of a neutrino underwater telescope

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A proposal for a new front-end architecture intended to capture signals in the optical module of an underwater neutrino telescope is described. It concentrates on the problem of power consumption, signal reconstruction, charge and time precision. Preliminary test results on a demonstration board are shown.

Summary:

The NEMO underwater neutrino telescope uses large area photomultipliers (PMTs) inside optical modules (OMs) to detect the Cherenkov light emitted by the muons generated by neutrinos in the seawater. The PMTs are put in a 17" glass sphere capable to stand more than 350 Atm external pressures. The signals at the output of the PMT must be suitably coded and sent on-shore. The OM contains the PMT and its base board, the front-end electronics, the data pack and transfer electronics, the slow control interface and a set of environmental sensors. The work described in this paper is aimed at the development of a low-power front-end for the OMs of the NEMO submarine neutrino detector. A mini-tower equipped with 16 OMs (NEMO-Phase1 MiniTower) has been successfully deployed in December 2006 in front of the Catania harbour as a first prototype. The technological solutions adopted provided results in agreement with expectations. In the meantime, we have developed a solution which can fulfil all requirements of a km3-scale detector, in particular for what concerns power consumption, PMTs aging and signal dynamics. The final version of the presented front-end electronics will be employed in one of the 16 floors NEMOPhase2 Tower to be deployed at the end of 2008. This solution is based on the use of an Application Specific Integrated Circuit (ASIC) for the fast sampling of the PMT signal, which is performed according to its shape classification made by another unit. Two other units, one ADC
and a Field Programmable Gate Array (FPGA), provide digital encoding of the voltage sampled signals, the packing of the data and its transfer towards the shore station. An electronic board containing the PMT interface and the mentioned units constitutes the OM front-end. By means of the FPGA, this board receives the slow control signals and transmits the measurements of environmental parameters such as temperature and humidity, together with the data. A proposal for a system to capture signals from Optical Modules of an underwater neutrino telescope has been described, with focus on power consumption and dynamics considerations. All considerations regarding the signals and their acquisition are discussed, starting from the most general hypothesis possible, so that they will be valid for any underwater Cherenkov neutrino telescope. The development of the demonstration board to evaluate the advantages of the proposed architecture fitting the specifications of power dissipation, multiple input dynamics, signal reconstruction, establishes the basis for the definitive design of the final front-end board using the SAS chip. As soon as the chip will be available, the whole front-end will be tested together with the PMT.

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Mezzanine Cards for the EMU CSC System Upgrade at the CMS

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In this paper we discuss two ideas related to the design and application of mezzanine cards in the Endcap Muon (EMU) Cathode Strip Chamber (CSC) electronic system at the CMS experiment at CERN. The first is a proposal to upgrade the FPGA-based mezzanine cards using the most advanced Xilinx Virtex-5 family of FPGA. The second is related to design of a simple and compact mezzanine card with a commercial serializer/deserializer device and industry standard pluggable optical or copper transceiver module. Such a card could be a basic element of the general purpose gigabit data transmission link.

Summary:

The CSC detector comprises 468 six-layer multi-wire proportional chambers arranged in four stations in the Endcap regions of the CMS. Its Triggering and Data Acquisition systems consist of more than 14,000 electronic boards with approximately 4,500 Xilinx FPGA devices. More than 1,000 FPGAs are mounted on custom mezzanine cards that have been produced and installed on host boards of five types. The host boards reside directly on chambers, in the 9U crates on the periphery of the return yokes and in the Track Finder crate in the underground counting room. The mezzanine approach allows us to independently design, develop and upgrade the FPGA-based processing logic while preserving the host board functionality. The present electronic system is based on mature Virtex-E and Virtex-2 technologies. The new and most advanced family of Xilinx FPGA, the Virtex-5, offers several advantages over previous generations, including higher performance, lower power consumption, more flexible basic slice block, better clocking routing, more embedded memory. We have targeted two of our existing FPGA projects, the Muon Port Card and the Muon Sorter, to the Virtex-5 XC5VLX family of FPGA. The results of simulation show an increase in performance of ~50% for the same speed grade device. The ability of the new FPGA family to self-correct single event errors and report double errors is essential for the future SLHC upgrade.

The mezzanine approach can also be applied to data transmission links. The main parts of a typical serial digital link include the serializer (SER) and optical or copper transmitter on a transmission end and the optical or copper receiver and deserializer (DES) on a receiver end. In many cases the SER
and DES functions are combined in a single SERDES device. Optical modules are typically transceivers; among industry standards in the range from 1Gbps to 4Gbps the most popular is the Small Form-factor Pluggable (SFP) standard. In addition to optical, copper SFP modules (either passive or active) are also available. The idea of combining a SERDES device and a pluggable transceiver on a mezzanine card is not new, but existing implementations usually require relatively large space. Since both the Texas Instruments TLK family of SERDES devices and the SFP standard have significant potential for future projects, including the SLHC upgrade, we have decided to build a simple, compact and inexpensive mezzanine card using these components. Several pin compatible TLK devices support serialization and deserialization of 16- and 18-bit parallel data from 25MHz to 156.25MHz with the industry standard 8B/10B or start/stop encoding, provide either current- or voltage-mode serial interface and have an embedded PRBS generator. We describe this mezzanine card in detail in the paper. Sample boards with the TLK1501/2501/3101 devices are available for evaluation.

**Parallel Session A3 - Installation & Commissioning / 31**

**Mobile Test Bench for the LHC Cryogenic Instrumentation Crate Commissioning**

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The installation of the Large Hadron Collider (LHC) at CERN is completed. The magnets are installed and the emphasis is shifted to the commissioning. This work focuses on the commissioning of the cryogenic instrumentation. The LHC is a two-ring superconducting accelerator and pp collider of 27 km circumference. The dipoles will operate at 8.3 T, cooled by superfluid helium at 1.9 K. The operation and monitoring of the LHC require a massive amount of cryogenic instrumentation channels with a robust and reliable design. The cryogenic control system has to manage about 33000 input-output signals as well as 4000 control loops.

**Summary:**

The Large Hadron Collider (LHC) is a two-ring superconducting accelerator and proton-proton collider of 27 km circumference. The dipole magnets will operate at 8.3 T, cooled by superfluid helium at 1.9 K. Electrical Distribution Feedboxes (DFB) provide the electrical supply to the superconducting magnets. The LHC ring consists of 8 sectors, each divided in: regular arc (ARC, ~2.5 km), 2 dispersion suppressors (DS, ~0.5 km), and 2 long straight sections (LSS, ~0.5 km). The operation and monitoring of the LHC require a massive amount of cryogenic instrumentation channels - most of them operating in radioactive environment - with a robust and reliable design. The cryogenic control system has to manage about 33000 input-output signals, distributed along 27 km, as well as 4000 control loops.

798 instrumentation crates are installed, connected and tested underground. They house signal conditioning cards for the temperature sensors (TT), pressure sensors (PT) and liquid helium level sensors (LT), power cards to supply electrical power to the LHC cryogenic heaters (EH) and I/O cards to read the digital valve status. These crates communicate through a WorldFipTM field bus.

Information about electronics and instrumentation is stored in Layout Database. The commissioning of the Cryogenic Instrumentation (electronics, cabling, sensors, actuators), after their installation in the LHC tunnel is done by a Mobile Test Bench (MTB). Four Test Benches have been built at CERN to ensure the correct functionality of all electronics. The MTB is based on a PXI platform, running LabVIEWTM application.

The following tests are performed:

- Consistency test: Verification between actual and Layout database crate configuration.
- Card test: Electronic cards functionality check.
- Instrument test: Instruments presence and their functionality check.
- Pin-to-Pin test: Cable test for undesirable short circuits and continuity.
- FIP test: Full readout chain (sensor+electronics) functionality verification.
The MTB project uses Perforce, a Software Configuration Management (SCM) tool, which provides a centrally managed storage area for all files of a project, keeps detailed track of the history of each managed file and allows collaboration amongst users. More specifically Perforce is used to manage the LabVIEW software distribution from the developer team to the operator team, individual crate configuration files and also the results for all cryogenic instrumentation crates. The results are stored locally in the corresponding folder of the crate and after the completion of tests are submitted to the Perforce server and MTF - a network application that stores the data related to the management of the LHC equipment. The MTB is a valuable tool for resolving problems related to cables, sensors and connectors (i.e. wrong or not connected cables to the field instrument, wrong grounding/shielding in the cables/connectors, blown fuses, damaged cables or connectors, missing connections and mismatches with Layout DB and even Layout DB self inconsistencies).

Parallel Session A6 - Trigger2 / 6

Modular Trigger Processing - The GCT Muon/Quiet bit System and future applications

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The CMS Global Calorimeter Trigger HCAL Muon and Quiet bit processing function is being implemented with a micro TCA system. This system is reconfigurable in both logical functionality and data flow, allowing great flexibility to meet processing requirements. The system consists of a processing module based on a Xilinx Virtex 5 FPGA and custom backplane based on a Mindspeed crosspoint switch. Initial test results of the processing module will be available, and the overall progress of the design will be presented. In addition, future application of this technology for the SLHC level 1 trigger will be discussed.

Summary:

This system is being implemented utilizing a multi-gigabit switched serial mesh processing topology. It represents an evolution of the current GCT architecture, taking advantage of the lessons learned implementing the optical data transmission and concentration between the Regional Calorimeter Trigger racks and the GCT leaf cards. This topology is realizable in the micro TCA communications equipment standard, with a custom (though spec compliant) backplane. The core concept is that high speed serial links (both fiber and copper) are used for all communications both internally and externally. Analog crosspoint switching technology is used to provide a flexible communications mesh, allowing a regular hardware topology while retaining significant data routing options. Based on extensive experience with FPGAs in many applications, a concous decision was made to provide plentiful link routing, since connectivity remains the primary limiting factor in fully utilizing the logic resources of large FPGAs.

The processing module provides the data manipulation functionality to implement muon and quiet bit system logic, and directly interfaces to the fiber input from the RCT (through the GCT source cards). The processing module hardware will be available in a few months, and initial test results will be presented. Slow control, link testing on the FPGA, and loopback through the crosspoint should be complete. The backplane provides a combination of star/mesh connectivity, and is based on a Mindspeed 21141 crosspoint, and an Ethernet enabled micro controller for slow control. The processing module hardware will be available in a few months, and initial test results will be presented. Slow control, link testing on the FPGA, and loopback through the crosspoint should be complete. The backplane provides a combination of star/mesh connectivity, and is based on a Mindspeed 21141 crosspoint, and an Ethernet enabled micro controller for slow control. The backplane design is complete, and updates will be presented on the layout/fabrication process. Such a modular design is not only well suited to the GCT muon and quiet bit system, but can also be of use for general trigger processing. The combination of fine grained processing modularity and flexible data routing make it an attractive choice for the trigger upgrades currently being contemplated for SLHC. An initial proposed architecture of the SLHC level 1 trigger based on this technology will be presented.
NESTOR participation in the KM3NeT

NESTOR Collaboration is a key player in the Design Study of the KM3NeT, the European Deep Sea Neutrino Telescope and claims to have the best site in the Mediterranean for this. In this report we describe briefly the site properties, the pioneer NESTOR expertise, our contribution towards the KM3NeT and present the specially constructed, for telescope modules deployments, ship-platform “DELTA-BERENIKE”.

New sensors for particle detection with in-situ charge storage

Steve Worm

Image Sensors with In-situ Storage (ISIS) are being developed for use in future linear collider and fast imaging applications. The ISIS device consists of pixels each with a short charge storage register. Charge is collected by a photogate and stored in one of many in-pixel storage registers, for readout during quiet periods in the beam duty cycle. For an ILC application it is expected that 20 storage cells and a relatively low readout rate of 1MHz will be sufficient. I will present the results in testbeam of a CCD-based proof of principle device, with 16 x 16 ISIS cells with a buried channel CCD storage register in each.

A new device is currently being fabricated in a CMOS 0.18 micron process, and is due out at the time of the workshop. It incorporates interesting features of CCD-like buried channel and deep p+ shielding implants, which allow efficient charge collection and integration of readout structures on the same wafer.

Noise Susceptibility Measurements of Front-End Electronics Systems

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The conducted and radiated noise that is emitted by a power supply constrains the noise performance of the front-end electronics system that it powers. The characterization of the noise susceptibility of the front-end electronics allows setting proper requirements for the back-end power supply in order to achieve the expected system performance. A method to measure the common mode current susceptibility using current probes is presented. The compatibility between power supplies and various front-end systems is explored.

Summary:

1. Introduction.
The front-end electronics of particle physics detectors aim to achieve high levels of performance in terms of resolution and accuracy. This performance is limited by the system intrinsic noise, but also by the noise properties of the power supplies. The compatibility between power supplies and front-end systems can be characterized, to obtain a manageable noise performance of the entire system. A method to evaluate the conducted noise susceptibility of a front-end system is proposed. Front-end power converters emit also near field radiated noise; a method to explore the front-end susceptibility to radiated noise is proposed. The methods are applied to the front-end electronics of the absolute luminosity monitor for ATLAS (ALFA) and on the TOTEM front-end. On the basis of the susceptibility figures, the noise properties of the power supplies can be set for each system.

1. Bulk injection method.

The common mode current is known to be a back-end dominant source of noise that degrades the performance of a front-end system. The measurement of the front-end noise susceptibility is carried out with the injection of known common mode currents in the power supply lines over a given frequency range using bulk injection probes. The injected current is monitored with a calibrated probe and adjusted in an automated procedure. The voltage applied to the bulk probe allows to estimate the common mode input impedance and to identify the presence of filters and their effective frequency range.

1. Conducted susceptibility.

The conducted susceptibility measurement method was exercised on the ALFA front-end prototype. The power supplies feed a motherboard that interconnects with twenty five photomultiplier front-end modules (PMFs). Each PMF houses a MAROC front-end ASIC, that amplifies and discriminates the PMT signals. The signals are acquired and transmitted to the motherboard by FPGA logic. The motherboard packs and transmits the data through a GOL link. The system uses linear regulators, and the input power lines are fitted with common mode filters. The sensitivity of the PMF against noise is first determined by means of a threshold scan that delivers a noise S-curve. A threshold is then set and common mode currents are injected, with varying amplitudes up to 10mA and frequencies comprised between 150 kHz and 100 MHz. The measured common mode input impedance put in evidence the filters effectiveness between 35 MHz and 70 MHz. The injected current allows putting in evidence a susceptibility peak at 25 MHz, in agreement with the frequency response of the front-end preamplifiers. The relationship between the threshold and the current amplitude is explored.

1. Front-end power converters.

Power converters located in the vicinity of the front-end systems radiate electromagnetic fields that degrade the system performance. The compatibility between the TOTEM front-end electronics and switched power converters is explored. The susceptibility of the this system to near magnetic field is evaluated.

1. Conclusions.

The noise susceptibility of front-end systems is a key parameter that can be evaluated with accurate measurements. The obtained results bring valuable information on the noise coupling mechanisms between the power supplies and the front-end circuits, which can be used to set up appropriate filters and to specify a compatible power supply system.

POSTERS SESSION / 80

Noise analysis of Radiation Detector Charge Sensitive Amplifier Architectures.

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In this work, a detailed comparison of four equivalent charge-sensitive, folded-cascode amplifiers in terms of noise performance is presented. A couple of complementary structures, one with a noise-optimised input nMOSFET and the other with a noise-optimised input pMOSFET were designed in 0.35 um CMOS process by Austria MicroSystems (AMS). Another couple of complementary structures consisting of a noise-optimised input npn with a pMOSFET cascode, and the respective structure having a pMOS as input device, were developed in a 0.35 um SiGe BiCMOS process (AMS). The structures’ comparison is performed through simulation, after careful selection of the parameters that remain constant in all four variations.

Summary:
Detailed analysis was performed for the folded cascode architecture. Our primary concern was the examination of noise contribution of the devices pair, firstly the input transistor and secondary, the cascoded one. The four structures were: a) nMOS as the input and pMOS as cascode, b) pMOS as input, nMOS as cascode, c) npn as input, pMOS as cascode and d) pMOS as input and npn as cascode. To further isolate these noise contributors, ideal bias current sources and output buffer were used, in all four designs. Feedback was implemented using a capacitance in parallel with a large reset resistor.

In order to achieve a fair comparison, the bias current of the input branch was selected by applying noise-optimisation theory on the input npn available transistor. This bias was then kept constant for the rest implementations, where noise-optimization methodology was applied regarding the input MOS type to set its dimensions. This bias current selection, in addition to constant total power (current) consumption, leads to a constrained bias current for the cascode. This, in the case of the BJT cascode, results to a specific transconductance and parasitic capacitance value, constraining the cascode MOS dimensions in the rest cascode structures.

The output noise was examined in relation to the detector’s capacitance variation and the input branch’s bias current. In addition, the peaking time dependence (and consequently the operating bandwidth variation) was also examined, concerning the total output noise.

The results of this work aim in proposing input device selection criteria and consequently the folded cascode structure, in relation to the output noise, detector’s capacitance variations and the available process (CMOS or SiGe BiCMOS) in conjunction with fabrication cost.

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Parallel session B1 - Trigger 1 / 116

Operation and Monitoring of the CMS Regional Calorimeter Trigger

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The electronics for the Regional Calorimeter Trigger (RCT) of the Compact Muon Solenoid Experiment (CMS) have been produced, tested, and installed. The RCT hardware consists of 1 clock distribution crate and 18 double-sided crates containing custom boards, ASICs, and backplanes. The RCT receives 8 bit energies and a data quality bit from the HCAL and ECAL Trigger Primitive Generators (TPGs) and sends it to the CMS Global Calorimeter Trigger (GCT) after processing. Integration tests with the TPG and GCT subsystems have been successful.

Installation is complete and the RCT is integrated into the Level-1 Trigger chain. Data-taking, triggered with cosmic ray muons, is now regular. Progressively, the operation and configuration of the RCT has moved from mostly hands-on to a completely automated process. The tools to monitor, operate, and debug the RCT are mature and will be described in detail, as well as the results from cosmic muon data-taking with the RCT.

Summary:
The electronics for the Regional Calorimeter Trigger (RCT) of the Compact Muon Solenoid (CMS) Experiment have been produced, tested, and installed. The RCT has been integrated with the ECAL and HCAL Trigger Primitive Generators (TPGs) responsible for RCT input and the Global Calorimeter Trigger (GCT) that receives the RCT output. The hardware of the RCT consists of one 6U clock distribution crate with custom boards and eighteen 9Ux680mm double-sided crates containing a custom backplane and boards with custom ASICs. Including spares, almost 1800 boards of 9 different types have been produced. Included are a Clock Input Card (CIC), two Clock Fan-out Cards (CFCm and CFCc), backplane, Clock and Control Card (CCC), Receiver Mezzanine Card (RMC), Receiver Card (RC), Electron Identification Card (EIC), and Jet/Summary Card (JSC). This system receives 8000 calorimeter trigger tower transverse energies (ETs) and characterization bits from the ECAL and HCAL TPGs via 4 GBaud copper links. These ETs are summed over 4x4 tower regions for jet finding, missing ET, and total ET. Additionally, the individual tower energies and characterization bits are used to find electron candidates. These quantities are then forwarded to the GCT via their source cards for further processing and sorting.

The RCT crates, cables, and associated hardware have been installed underground and commissioned. The complete HCAL and barrel of the ECAL are fully installed and commissioned, resulting in the RCT’s routine use as part of the CMS Level-1 Trigger chain. Simple pattern tests verified the chain and its timing, and before the LHC turn-on, data has been taken using cosmic-ray muons to produce triggers. Progressively, the testing, configuration, and operation of the RCT has moved from command-line to a completely automated graphical user interface. Slow-control operations, such as power and temperature monitoring and control use the PVSS (Prozessvisualisierungs- und Steuerungs-System) SCADA (Supervisory Control and Data Acquisition) tool. RCT crate configuration and monitoring is done within the framework provided by the CMS Trigger Supervisor toolkit. As part of a Data Quality Monitoring (DQM) framework the RCT is checked both online and offline using a software Trigger Emulator (TE) for comparison. Finally, a set of custom offline crate tests using the TE and the RCT’s self-test mode check inter-RCT connections and external links for possible problems. Details of the hardware, the implementation of these tools, and results from cosmic muon data-taking with the CMS Regional Calorimeter Trigger will be described in detail.

POSTERS SESSION / 63

Operational Experience With The SCT Optical Links

Anthony Weidberg

1 Nuclear Physics Laboratory

The optical links for the SCT have all been installed in ATLAS and are now used for data taking. This talk will review the processes required for the commissioning the links and the tools used to set-up the links and monitor their performance. This allows for an assessment of the current quality of the optical links as well as starting to monitor their long term performance. The methodology for setting up the timing of the TTC links will be described. Lessons learned from the commissioning of the optical links will be discussed.

Summary:

The optical links for the SCT have been installed in ATLAS. The optical links read out the data from each of the 4088 SCT modules as well as providing the Timing, Trigger and Control data to each module. The final connections for the electrical and optical services for the links were completed last year and rapid tests were used to verify the continuity. It was essential to rapidly determine and fix any problems before access to the connections became impractical. A few cases of dirt inside optical connectors were found and were easily fixed by cleaning the connectors. One case of a broken fibre ribbon near the detector was found and this was repaired using a fusion splicer. The tests of the optical links, then allowed an assessment of the quality of the installed links, which was generally very good although there were a few dead channels. The chief causes of the dead and problematic links were ESD VCSELs and single fibres that were broken during the final integration, after which access became impossible. The low level of non-functional links will not lead to any significant loss of data, due to the data and TTC redundancy schemes that are being used. A very small fraction of the TTC links, have delivered
optical power lower than required for long term operation and the corresponding VCSEL arrays in the counting room will be replaced.

The methodology used for setting up the data and TTC links, as well as the tools that will be used to monitor their long term performance will be reviewed. This monitoring involves a combination of analogue measurements, digital scans and some simple in-situ Bit Error Rate measurements. Some proposals for how to improve these tools for the upgraded tracker at SLHC will be discussed.

For the Timing Trigger and Control links it is essential to be able to adjust the timing of the L1 signal in order to read out the triggered event. It is also necessary to optimise the phase of the 40 MHz clock received by each module in order to maximise the detector efficiency. The procedures used to achieve this involved measuring the lengths of all the optical fibres from the counting room to the on detector patch panels. The final optimization of the timing will be done by scanning the phase of the 40 MHz clock and measuring the module hit efficiency using track data. Results from this procedure using Cosmic ray data will be presented. The TTC system uses BiPhase Mark encoding to encode the command data on top of the 40 MHz clock. Therefore, in order to minimise the jitter for the 40 MHz bunch crossing clock, it is important to optimise the mark to space ratio of the incoming 20 MHz clock. The procedures used to achieve this will be explained.

Finally some general lessons learned from the commissioning of the optical links will be discussed which will be relevant for the optical readout of the upgraded tracking detectors for the SLHC.

OPTO ELECTRONICS WORKING GROUP / 166

Optical Links Quality - CMS

Plenary Session 4 - Optoelectronics, a global telecom carrier’s perspective / 149

Optoelectronics, a global telecom carrier’s perspective

Jeremy Batten¹

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This paper summarises the current approaches to high speed optical transmission design. Cable&Wireless operates a large global optical transmission network, with the main purpose of serving the bandwidth market and of providing connectivity for its Internet Protocol data networks. In long haul spans, dense wavelength division multiplexed systems with aggregate capacities of 1Tbit/s per fibre are deployed. The increase in bandwidth requirement is driving the need for more complex technologies that deliver a jump in system capacity. Emerging optoelectronic technologies are discussed, with particular focus on 40 Gbit/s per wavelength transmission and optical wavelength switching.

Plenary Session 6 - LHC upgrades: needs and reality / 140

Overview and Electronics Needs of ATLAS and CMS High Luminosity Upgrades

Nigel Hessey¹

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The LHC will start up in 2008 and ramp up in luminosity over 3 years to $10^{-34}$ cm$^{-2}$ s$^{-1}$. A series of machine upgrades will continue to increase this, eventually reaching $10^{-35}$ cm$^{-2}$ s$^{-1}$ around 2018. This talk summarises the physics possibilities that high luminosity will open up, and then describe the changes needed to ATLAS and CMS to meet the challenges of the high pile-up of overlapping events and radiation background. Electronics advances are needed throughout the detector and will be emphasized.

**Parallel Session B4 - Interconnects / 22**

**PMF the front end electronic for the ALFA detector**

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The front end electronic (PMF) of the future ATLAS luminometer is described here. It is composed by a MAPMT and a compact stack of three PCBs which deliver the high voltage, route and readout the output signals. The third board contains a FPGA and MAROC, a 64 channels ASIC which can correct the non uniformity of the MAPMT channels gain thanks to a variable gain preamplifier. Its main role is to shape and discriminate the input signals at 1/3 photo-electron and produce 64 trigger outputs. Laboratory tests performed on few PMFs have showed performances in good agreement with the requirements.

**Summary:**

The PMF (Photo Multiplier Front end) is the front end electronics designed for the ATLAS luminometer ALFA (Absolute Luminosity For ATLAS) made of 20 staggered U-V scintillating fiber layers inserted in Roman Pots (eight in total). Each of these plans is made of 64 fibers. The PMF consists of a 64 channels photomultiplier (MAPMT) and a very compact stack of three different PCBs (3x3 cm$^2$), mounted directly on the back and in the shadow of the MAPMT: a board which brings the high voltage to the MAPMT, an intermediate board used to send the signals to connectors located on the edge and, finally, a board with the readout chip MAROC (Multi Anode Read Out Chip), directly bonded on the PCB, on one side and a FPGA on the other.

The 64 inputs MAROC ASIC allows correcting for the gain spread of MAPMT channels thanks to a 6 bits variable gain preamplifier. For each channel the signal is shaped (fast shaper, 15ns) and discriminated to produce a trigger output. A multiplexed charge output is also produced both in analog and digital thanks to a Wilkinson ADC. The main requirements are the following: 100 % trigger efficiency for a signal greater than 1/3 of a photoelectron, a charge measurement up to 30 photoelectrons with a linearity of 2 % or better and a cross talk of 1 % or less. The performances of the second version of MAROC were checked successfully during the year 2007 at LAL-Orsay. A nice dispersion of the trigger output ($\pm$ 5 fC) was, in particular, observed. A sample of PMFs was produced during autumn 2007 as a prototype. Laboratory tests were performed both at LAL and CERN respectively on the third PCB (the one with MAROC) and on a full PMF equipped with a MAPMT illuminated by a LED. They were carried out using dedicated test board and acquisition software and have allowed the approval of the design and the green light for the final production and integration with the detector.

Beam tests of a complete Roman Pot, equipped with 23 PMFs, will take place during summer 2008 for two periods and will conclude the test phase and mark the beginning of the final production.

**POSTERS SESSION / 98**

**PMM2 ASIC : PARISROC**
PARISROC is a complete read out chip in AMS SiGe 0.35μm technology for photomultipliers array. It is made to allow triggerless acquisition for next generation neutrino experiments. The ASIC integrates 16 independent channels with variable gain and provides charge and time measurement by a 12-bit ADC and a 24-bits Counter.

Summary:
PARISROC is a front-end electronics ASIC designed for the next generation of neutrino experiments. These detectors will take place in megaton size water tanks and will require very large surface of photodetection. An R and D program, funded by French national agency for research and called PMm2, proposed to segment the very large surface of photodetection in macro pixels made of 16 photomultiplier tubes connected to an autonomous front-end electronics. The ASIC must only send out the relevant data by network to the central data storage. This allows to reduce considerably the cost of these detectors. This paper describes the front-end electronics ASIC called PARISROC. The PARISROC chip integrates 16 channels totally independents. Each channel contains:
- a low noise preamplifier with 8 bits variable gain (tuneable by a factor 4) to adjust the PMTs gain variation.
- a variable slow shaper (50-200ns) followed by an analogue memory with depth of 2 to provide a charge measurement up to 50pC.
- a second analogue memory with same depth to sample fine time measurement with precision of 1ns.
- a 12-bit Wilkinson ADC to convert the charge and fine time measures.
- a fast shaper (15ns) followed by 2 low offset discriminators to auto-trig down to 10fC. The thresholds are loaded by 2 internal 10-bit DACs.

A digital part manages all the acquisition, the conversion and the readout and provides by a 24-bit counter the coarse time measurement or timestamp. The design and simulation results of the first prototype will be presented.

POSTERS SESSION / 4

Performance of Specific Multi-Mode and Single Mode Passive Optical Components to Co60 Gamma Rays up to SLHC Integrated Doses

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The luminosity upgrade for the LHC (SLHC), will require new inner detectors capable of operating in the harsher SLHC environment. The expected SLHC doses are a factor of four times higher than those assumed for the LHC detectors. An optical readout system is planned for which all on-detector components must be significantly more radiation tolerant than was required for the current LHC detectors.

This paper presents first results on radiation tests of all the passive optical components that might be required inside the SLHC tracking detectors. The methodology for this testing will be described, so that meaningful comparisons can be made with data from other groups. Optical components based on 850 nm or 1310 nm were tested. A new more radiation tolerant and faster GRIN fibre than used by the current ATLAS detector was tested to the full SLHC dose. Tests were also done to study the dose rate dependence of the fibre damage. The SM fibre at 1310 nm used by the current CMS detector was also tested up to the SLHC dose. Radiation tolerance tests of fused taper and PLCC splitters and of small form factor connectors for 850 nm and 1310 nm were completed. The facility at the SCK-CEN reactor centre in Belgium was used. The exposures used Co60 gamma sources with dose rates of
15.2 kGy/hr and 1.5 kGy/hr. The results for the GRIN fibre will also be compared with results from the SMU group at even lower dose rates.

Summary:

The luminosity upgrade for the LHC (SLHC), will require new inner detectors capable of operating in the harsher SLHC environment. The expected SLHC doses are a factor of four times higher than those assumed for the LHC detectors. The higher luminosity at the SLHC will require more granular tracking detectors and imply that a higher data transmission rate will be required. An optical readout system is planned for which the consequences will be that higher speed digital links will be required to read out the increased number of channels and all on-detector components must be significantly more radiation tolerant than was required for the current LHC detectors.

This paper will present first results on radiation tests of all the passive optical components that might be required inside the SLHC tracking detectors. The methodology for this testing will be described, so that meaningful comparisons can be made with data from other groups. The methodology is based on having reliable in-situ measurements during the radiation exposures. Fibre splitters are used in all the test systems to allow for any drifts in the optical power output of the lasers. Low drift amplifiers were used for the p-i-n receivers. The methodology will be verified by extensive testing before irradiation. At this stage it is not yet known if the SLHC optical readout will be based on 850 nm or 1310 nm. Therefore these tests will cover components for both 850 nm and 1310 nm transmission. A new more radiation tolerant and faster GRIN fibre (than used by the current ATLAS detector) was tested to the full SLHC dose. Tests were also done to study the dose rate dependence of the fibre damage. The SM fibre at 1310 nm used by the current CMS detector was also tested up to the SLHC dose. Radiation tests of fused taper and PLCC splitters were also tested. Small form factor connectors for 850 nm and 1310 nm were also evaluated for radiation tolerance. These tests have been performed at the SCK-CEN reactor centre in Belgium. The exposures used Co60 gamma source with dose rates of 15.2 kGy/hr and 1.5 kGy/hr. The results for the GRIN fibre will also be compared by tests done by the SMU group at even lower dose rates.

The plans for the next stages of the radiation tests for the passive optical fibre connectors will be discussed.

POSTERS SESSION / 107

Power Distribution in a CMS Tracker for SLHC

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In the current CMS tracker power cables constitute a substantial fraction of its dead-material. In an upgraded tracker for an SLHC the current scheme of supplying power independently to each module is unlikely to be tenable due to excessive dead-material. A review of the current ideas for power distribution for a CMS tracker at the SLHC are presented, the experimental methods used to evaluate the performance of different schemes is described and the ongoing tests of different options are outlined.

POWER WORKING GROUP / 162

Progress on DC/DC Converters Prototypes
Radiation Damage of SiGe HBT Technologies at Different Bias Configurations

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SiGe BiCMOS technologies are being proposed for the Front-end readout of the detectors in the middle region of the ATLAS-Upgrade. The radiation hardness of the SiGe bipolar transistors is being assessed for this application through irradiations with different particles. Biasing conditions during irradiation of bipolar transistors or circuits have an influence on the damage and there is a risk of erroneous results. We have performed several irradiation experiments of SiGe devices from IHP in different bias conditions. We have observed a systematic trend in gamma irradiations, showing a smaller damage in transistors irradiated biased compared to shorted or floating terminals. On the other hand, no differences have been observed in neutron irradiations.

Summary:

The LHC at CERN is expected to start taking data during this year. In the meantime, a new project has started to try and extract more physics benefits after its expected life span of 10 years. The plan is to upgrade the accelerator in order to increase its luminosity in around one order of magnitude, it is called the Super-LHC. It has been shown that this will force the modification of the different experiments installed in the accelerator. In particular, the total inner detector of the ATLAS detector will have to be upgraded. Some of the microelectronics technologies proposed for the for the front-end readout of the detectors in the middle region of the upgraded inner detector are the SiGe BiCMOS technologies. These technologies should provide better performances in terms of power consumption, signal to noise, and processing speed, but they have to be evaluated in terms of radiation hardness.

In order to perform this evaluation, the devices should be submitted to different irradiation experiments, and then measure their performance after irradiation. These experiments are usually performed in complex irradiation facilities with difficult access to the irradiation area. This complicates the irradiation setup, in particular, biasing the devices during irradiation in order to mimic the real conditions is very difficult, and often impossible. This work studies the different result of radiation damage in the SiGe HBT transistors when submitted to irradiations with different particles in various bias configurations.

We have performed irradiations of SiGe HBT transistors with Co60 gamma particles, nuclear reactor neutrons, and 24 GeV beam protons in three different bias configurations: biased in forward active region (in similar conditions as they will be working in the real experiment); with all their terminals short-circuited; and with all their terminals floating. Differences in radiation damage have been observed for SiGe transistors submitted to gamma irradiations in biased configuration with respect to shorted and floating configurations. Biased transistors suffer less current gain degradations than shorted transistors, and these suffer less degradations than floating transistors. This tendency has not been observed in transistors submitted to neutron irradiations, where the radiation damage is the same for all bias configurations. Results proton irradiations will be also shown.

The variation of radiation damage in time after irradiation (annealing) has also been studied in order to discard differences in radiation degradation coming only from different degree of annealing of the damage due to their different biases during irradiation. Transistors have been measured right after irradiation, and then left some time for annealing in the same bias conditions, then re-measured. Less annealing has been observed for gamma irradiations in the biased transistors indicating that some of the damage differences observed actually come from different annealing levels, nevertheless some differences in damage remain after the full annealing process.

These results indicate that some differences can be observed in the damage of bipolar transistors submitted to ionizing radiation in different bias configurations. Comparison to previous result indicate that the quantitative value of these differences is very technologically dependent with respect to total dose, therefore these effects should be studied in detail before performing irradiation experiments of bipolar devices in bias conditions different of the real life ones, at the risk misleading results.
Readout Electronics of the ATLAS Cathode Strip Chambers

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The ATLAS muon spectrometer employs cathode strip chambers (CSC) to measure high momentum muons in the forward regions (2.1 < |\eta| < 2.7). Due to the severe radiation levels expected in this environment, the on-detector electronics are limited to amplifying and digitizing the signal while sparsification, event building and other tasks are performed off-detector.

We report on the commissioning of the CSC readout electronics and its integration into the ATLAS detector.

Summary:

The ATLAS CSC system consists of 32 chambers arranged in two endcaps. One chamber consists of four layers, each providing a precision measurement in the radial direction and a coarser measurement of the azimuthal coordinate.

The substantial radiation dose these chambers are expected to accumulate warrants minimal use of highly integrated circuits on the chambers themselves. Processing of digitized data is therefore performed entirely by the off-detector electronics.

The cathode strip signals are amplified, shaped, and the pulse height information stored in switched-capacitor arrays. When triggered, multiple consecutive time samples from all channels are digitized and transmitted off-detector via fiber optic cable.

The off-detector electronics control the sampling and digitization, sparsify the incoming data, organize them into event fragments, and pass them on to data acquisition. Sparsification includes zero suppression, rejection of out-of-time hits, and rejection of background clusters, e.g. from neutrons.

Digital signal processors (DSP) are used for processing the data, while control functions are implemented in FPGAs. One ROD motherboard is shared by 12 DSPs handling a total of two chambers or 1920 channels. Incoming and outgoing fiber optics communications are handled by a separate transition module which connects to the ROD through a custom backplane.

At this time installation of the chambers in ATLAS is complete. We report on details of the implementation, and the performance of the electronics during ATLAS commissioning.
The ATLAS Pixel Detector is the innermost detector of the ATLAS experiment at the Large Hadron Collider at CERN. Approximately 80 M electronic channels of the detector, made of silicon, allow to detect particle tracks and secondary vertices with very high precision.

After connection of cooling and services and verification of their operation the ATLAS Pixel Detector is now in the final stage of its commissioning phase. Prior to the first beams expected in Summer 2008, a full characterization of the detector is performed. Calibrations of optical connections, verification of the analog performance and special DAQ runs for noise studies are ongoing. Combined operation with other subdetectors in ATLAS will allow to qualify the detector with physics data from cosmic muons and colliding beam interactions.

The talk will show all aspects of detector operation, including the monitoring and safety system, the DAQ system and calibration procedures.

The summary of calibration tests on the whole detector as well as analysis of physics runs will be presented.

Summary:

The ATLAS Pixel Detector was connected to the electrical and cooling services and off-detector readout electronics in March 2008. All connections were certified before the detector was closed. Prior to the operation with the Large Hadron Collider (LHC) beam, all the necessary tunings of the pixel detector have been performed and the detector itself has been fully qualified. The detector has been successfully integrated into the ATLAS Trigger and DAQ system allowing data-taking with high efficiency synchronously with other sub-detectors.

The detector functionality checks have been performed starting from the early production phase. For this purpose, dedicated calibration techniques have been implemented. These techniques have been developed with each detector assembly stage, matching the demands of the real detector services and readout system. Additional calibration procedure, related to the operation in ATLAS, have been introduced. The characterization aims for stable operation of the detector and provides input for the offline analysis to guarantee high quality of the reconstructed data. Important detector characterization issues are:

- tuning of optical links - to have reliable connections between the detector and readout electronics and to adjust fine detector timing;
- threshold tuning - to have a uniform predefined threshold for all detector channels;
- \( \text{ToT} \) tuning - to have a uniform detector response upon detection of the same deposited charge for all detector channels;
- bump connectivity check - to check for unconnected channels;
- ToT calibration - to calibrate detector response to input charge;
- noise occupancy check - to verify low-noise performance and spot noisy channels;
- timewalk check - to study timing behaviour of detector channels;
- sensor check - to study charge collection efficiency and detector leakage current.

Previous experience with detector characterization so far has been limited to parts of the detector. For combined operation with test beam, only a few modules were used, whereas one whole endcal (~10% of the detector) was tested stand-alone under real operating conditions with cosmic
muons. In contrast, the results shown in this presentation give a summary of qualification tests for the whole detector in situ.

In addition, analysis of special data-taking runs with pseudo-random triggers to verify noise occupancy, as well as the outcome of combined runs with cosmic muons will be presented.

POSTERS SESSION / 64

Results on the Performance of the CMS Global Calorimeter Trigger for Electrons and Jets

Robert Frazier

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The CMS Global Calorimeter Trigger (GCT) is the device within the CMS Calorimeter Trigger system which is assigned the tasks of finding and sorting forward-, central- and tau-jet candidates, sorting isolated and non-isolated electron candidates, and reading out all the calorimeter trigger data. The GCT system is modular and uses 1.6 Gbps optical links to concentrate the calorimeter data in eight processing cards which accomplish the algorithm tasks by utilizing Virtex-II-Pro Xilinx FPGAs. The entire GCT system, including both electron- and jet-trigger hardware, has been installed and commissioned in the CMS underground cavern, USA-55. A sophisticated software package has been developed for controlling and configuring the GCT hardware and well as for monitoring the GCT status. Over the past one and a half years the GCT system has undergone detailed testing and its performance is well understood. The GCT design provides buffers at its inputs capable of holding 2048 events; these have been used to inject energy depositions corresponding to electrons and jets in order to test the GCT functionality by comparing its output with that of the GCT emulator. Entire SUSY, Higgs and QCD Monte Carlo background events that have a large number of jets in the final state have been used to validate the GCT performance. The results from all these studies are presented.

Summary:

The CMS Global Calorimeter Trigger (GCT) is an integral part of the CMS trigger system. Its function is to receive and process data from all 18 Regional Calorimeter Trigger (RCT) crates and send the four highest-ranking electron and jet candidates to the Global Trigger, where they are used for generating the Level-1 Trigger Accept decision. This system has been designed to be modular. Due to a compressed development schedule, it borrows heavily from existing designs.

The primary requirements of the GCT are to sort electron candidates, and generate and sort jet candidates. The design has been optimized for these tasks. Other requirements include jet trigger counters, total jet transverse-energy trigger, total transverse-energy and missing transverse-energy triggers, luminosity monitoring, and RCT readout. The GCT is composed of four module types, the Source, Leaf, Wheel, and Concentrator cards.

The Source Cards receive their input data directly from the RCT crates, and transmit their output data via multi-gigabit optical links to the GCT main-processing crate. The Source Cards are located in the same racks as the RCT, and their main function is to convert the differential ECL RCT signals to high-speed serial optical format. In addition, the Source Cards provide the means for data capture and readout of the RCT data. Test data can be injected at the Source Card inputs using the 2048-event buffers implemented for each Source Card input channel. The Leaf Cards are configured to receive either electron or jet trigger data on high-speed optical fibres. Each Electron Leaf Card processes the electron data from nine RCT crates, selecting the four highest-energy candidates for further processing. Similarly, the Jet Leaf Cards process data from three RCT crates each, and forward the four highest-energy jets to the Wheel Cards. The jet-finding algorithm implements a sliding window. This requires data from adjacent RCT crates (corresponding to adjacent physical areas on the detector) to be exchanged; hence, Jet Leaf cards are linked to their neighbours in a corresponding fashion to facilitate this algorithm. The Wheel Cards are only used for processing jet data, and combine the output of three Leaf Cards each. These three Leaf Cards process the data from nine RCT crates, or half of CMS. The Wheel Cards sort the jets generated...
by the Leaf Cards, and forward the data from the four jet candidates with the highest transverse-energy to the Concentrator Card. The Concentrator Card accepts data from two Electron Leaf Cards and two Wheel Cards. It performs the final sorting of both electron and jet candidates, and sends the four highest-energy candidates of each type to the CMS Global Trigger. In addition, it provides a VME interface (slow control interface), and an S-Link64 data acquisition interface for the entire Calorimeter Trigger system.

At TWEPP 2007 we presented the first results from integrating the GCT in the CMS trigger system, as well as the first results from validating the Electron Trigger. The Electron Trigger has been used over the past year as the main CMS calorimeter trigger and has provided for stable operations and data taking. Using the experience for running the Electron Trigger, we have developed an extensive control and monitoring package to operate the GCT. This paper describes in detail the GCT software package and its performance. The running experience with the Electron Trigger resulted in upgrades of the Electron Trigger hardware. The final results on its performance are described here.

In the first half of 2008 the Jet Trigger was installed in USC55 and was integrated in the GCT system. The Jet Trigger was tested by injecting patterns and Monte Carlo events in the 2048-event input buffers of the Source Cards. Tests with events which had both electrons and jets were also performed and are presented. The Jet Trigger has been integrated in the GCT software framework. Results on the performance of the Jet Trigger are presented.

Over the past year the GCT group has received requests from CMS physics groups for triggers which were not included in the original GCT baseline design. The GCT group is in the process of implementing these upgrades and a short review of the progress achieved is also presented.

**Parallel Session A5 - Installation & Commissioning / 62**

**SCT Commissioning**

**Anthony Weidberg**<sup>1</sup>

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The Barrel and EndCaps of the ATLAS SemiConductor Tracker have been installed in the ATLAS cavern since summer 2007. All the electrical and optical services were connected and rapid tests performed to verify their continuity. Problems with the cooling circuits, meant that the time for detailed tests in 2007 was limited. These problems have now been resolved allowing the SCT to be operated and participate in combined ATLAS Cosmic ray data taking runs. The results of these runs have been used to determine the hit efficiency of the modules as well as providing invaluable constraints for the detector alignment.

**Summary:**

The Barrel and EndCaps of the ATLAS SemiConductor Tracker have been installed in the ATLAS cavern since summer 2007. The in-situ noise performance of the Barrel was verified, showing that there was no significant degradation after detector installation. Tests with combined operation with the TRT showed no evidence of cross-talk. There were major problems with the heaters for the evaporative cooling system which prevented more extended operation in 2007. For the EndCaps, very quick tests without cooling were used to verify the continuity of the electrical and optical services.

The problems with the heaters used for the evaporative cooling system, will be briefly reviewed as well as the solution that has been implemented. This required the design of more robust electrical connectors. All the heaters have been modified and installed and operated without problems so far. The location of the heaters has been moved to a more accessible location so that they could be replaced during a winter shutdown if necessary. There have also been problems with leaks for two of the EndCap cooling circuits and ideas about how to fix these leaks will be discussed.

The Barrel SCT participated very successfully in the combined ATLAS Cosmic ray data taking. The procedures used to rapidly time-in the detector, relative to the Cosmic ray trigger will be described as well as the plans for the more detailed timing adjustments that will be made with the first pp data. The Cosmic ray data was used to determine module hit efficiencies and for detector alignment. The
Cosmic ray data taken on the surface showed that the detector assembly was performed to a very high precision. The recent Cosmic ray data taken in the ATLAS cavern, also showed similar quality results, confirming that the good build precision of the detector was maintained during the final transport and installation in the ATLAS cavern. This is an important result as it will greatly simplify the alignment procedures. Extensive threshold scans were used to verify the noise performance of the modules and the results were consistent with those from earlier stages in detector assembly. In addition tests of combined operation of the TRT showed no increase in noise. These results verify the design of the grounding and screening. Leakage current measurements have been made for all detectors with good results. The thermal performance of the modules has been monitored using the thermistors on the modules. We also anticipate having results from the EndCaps, and from combined tests with the pixel detector.

In conclusion the current SCT performance exceeds the design specifications and the detector is ready for the first physics runs this year. However several difficulties were encountered and the assembly and commissioning experience will be used to extract lessons for future silicon detector projects.

**POSTERS SESSION / 57**

**SKIROC : A front-end chip to read out the imaging Silicon-Tungsten calorimeter for ILC**

Christophe de La Taille, Frederic Dulucq, Gisèle Martin-Chassard, Julien Fleury, Ludovic Raux

Integration and low-power consumption of the read-out ASIC for the International Linear Collider (ILC) 82-million-channel W-Si calorimeter must reach an unprecedented level as it will be embedded inside the detector. Uniformity and dynamic range performance has to reach the accuracy to achieve calorimetric measurement. A first step towards this goal has been a 10,000-channel physics prototype of 18”x18” cm which is currently in test beam in Fermilab.

A new version of a full integrated read-out chip (SKIROC) has been designed to equip the technologic prototype to be built for 2009. Based on the running physics prototype ASIC (FLC_PHY3), it embeds most of the required features expected for the final detector.

The dynamic range has been improved from 500 to 2000 MIP. An auto-trigger capability has been added allowing built-in zero suppress. The number of channel has been doubled reaching 36 to fit smaller silicon pads and the low-noise charge preamplifier now accepts both AC and DC coupled detectors. After an exhaustive description, the extensive measurement results of that new front-end chip will be presented. The characteristics of the new features such as internal ADC, auto-gain select or self-trigger will be detailed. The results on the technological R&D concurrently conducted on the ultra-thin PCB hosting both the front-end electronic and the silicon detectors will also be described.

**Summary:**

A new front-end chip called SKIROC – standing for Silikon Kalorimeter Read-Out Chip – has been designed to read-out the upcoming generation of Si-W calorimeter featuring ILC requirements. The analogue core of SKIROC is based on the front-end electronic designed for that physics prototype. It has been enhanced in many ways using an intermediate prototype called ILC_PHY4. The Maximum input charge has been extended from 500 to 2000 MIP.

The number of channel has been doubled - reaching 36 - to fit a pad size reduction in the silicon detector design conducted concurrently. A stand alone working capability comes along with the full power pulsing feature. That means SKIROC does not need any external component such as decoupling capacitance or bias resistor involving a huge room saving. The wake up sequence duration of the power pulsing is around 2µs to ensure a lower than 1% duty cycle in an ILC-like beam structure, involving more than two order of magnitude of power saving.

Beyond the analogue core improvement, many features have been implemented in SKIROC. A channel by channel auto-trigger capability has been added allowing a built-in zero suppression. A multi-channel ADC is embedded. The trigger and gain selection threshold is set by an internal dual DAC. Voltage references used in the analogue core use a bandgap reference to get rid of temperature and supply variation. A digital core driving all the analogue features and the digital communication with the DAQ has been designed and is implemented in a FPGA to get debugged and improved before being embedded in the
next version. The SKIROC chips will be used to equip the 40,000-channel ECAL foreseen for 2009 that will validate the technological choices for the 82-million-channel final detector. Many of the final detector requested features have been embedded and the performance has been greatly improved compared to the physics prototype front-end chip. The production of that ASIC is foreseen in summer 2008 to be able to take data in 2009, before the engineering design report of the final detector planned for 2010 by the ILC Worldwide Study Bureau.

**TOPICAL 1 - LHC Upgrades / 85**

**SLHC Upgrade Plans for the ATLAS Pixel Detector.**

Clara Troncon

1 *Univ. + INFN*

The ATLAS Pixel Detector is an 80 M channels silicon tracking system designed to detect charged tracks and secondary vertices with very high precision. An upgrade is presently being considered for the ATLAS Pixel Detector, enabling to cope with higher luminosity at Super-LHC (SLHC). Options considered for a new detector are discussed, as well as some important R&D activities, such as investigations towards novel detector geometries and novel processes.

**Summary:**

The Large Hadron Collider (LHC) will be upgraded to the Super-LHC in 2016 to provide a ten-fold increased luminosity and data rate. The inner silicon tracking detectors of the ATLAS experiment will be replaced by even more powerful devices. The new detector will face unprecedented particle densities and radiation levels. The increased luminosity leads to increased radiation doses, particle fluences and occupancies (fraction of channels per collision hit by a particle). The radiation dose is proportional to luminosity, while occupancy depends on the collision rate as well. The extreme radiation levels at the SLHC lead to a number of specific design challenges for read-out integrated circuits, silicon sensors and optical signal transmission, which we believe will be met. The impact of radiation on the overall design is important and affects not only sensors and electronics design, but also the cooling system, which has to provide reduced sensor temperatures to minimize sensor leakage currents.

The increased occupancy has also a huge impact and effectively shapes the new tracker. The larger number and density of electronics channels lead to increased power consumption, more and/or larger hybrids, more cables and increasing detector mass. Power consumption, power distribution and detector mass are the critical areas that demand innovative solutions to make tracking at SLHC possible.

The overall layout of the future ATLAS tracker is not jet defined, but experience from LHC tracker construction suggests that the layout will most be determined by services (electrical and cooling). Understanding and minimizing the service volume will be crucial.

Options considered for a new detector are discussed, as well as some important R&D activities, such as investigations towards novel detector geometries and novel processes.

**POSTERS SESSION / 92**

**SPECS: a Serial Protocol for the Experiment Control System of LHCb**
The LHCb sub-detector electronics requires a configuration bus able to communicate efficiently and reliably over an up to 120-meter line, between a master, located in the counting room which is not exposed to radiation, and up to 32 slaves located on the detector close to electronics boards. The slaves have been developed in order to work properly in radiation exposed environment (up to 40 Krad of total dose). The SPECS system is composed of a master board, that hosts 4 SPECS masters, and slaves (mezzanine boards) which provides all the necessary service functions and offers different bus interfaces.

Summary:

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The LHCb sub-detector electronics is organized around the detector in crates or individual boards, which require a configuration access to load and read different types of information. These operations will be driven from computers located in the control room, roughly at a distance of 60 meters from the various front-end elements. Therefore, the experiment requires a configuration bus able to communicate fast and properly over an up to 120-meter line, with a unique master, and up to 32 slaves. In such a configuration, the master card will be located in the control room, which is not exposed to radiation, and the slave close to the detector electronics boards. The slave thus has to be both SEL and SEU immune, in order to work properly in radiation sensitive environments (up to 40 Krad of total dose).

The SPECS protocol is a 10 Mbit/s serial link designed for the configuration of remote electronics elements. SPECS is a single-master multi-slave bus. The protocol requires 4 or 8 copper links (4 lines or 4 pairs) in BLVDS technology with pole-zero cancellation at the emitter side. The 8-pin RJ45 connector was thus chosen for the interconnections. It is a cheap and compact standard, which can be associated with Ethernet cables (cat 6 type).

The SPECS frame is composed of a fixed-size header (8-bit words which contain information relevant to the transfer), a variable-size data block, and a fixed-size trailer with the checksum of the data block. The SPECS master board will host 4 SPECS masters. This board is implemented on a standard 3.3V 32-bit 33 MHz PCI board, which can be plugged into any PC. The board also includes a SPECS slave for JTAG and I2C output capability. The heart of the system is designed as a portable VERILOG code and integrated within an Altera Cyclone FPGA, the PCI interface being performed by a dedicated circuit (PLX9030).

The SPECS slave offers different interfaces: Point to point SPECS interface for long distance interconnections, Multi drop SPECS bus, Local bus parallel interface, 32 configuration I/O lines, JTAG master interface, long distance I2C master bus: For the JTAG and I2C outputs, 24 command signals allow the slave chip to drive up to 12 independent links.

An intermediate mezzanine board of 0.47 dm² houses the SPECS slave, and provides all the described functionalities using 2 SMC connectors. The mezzanine board also provides most of the necessary service functions for the sub-detector front-end electronics: long distance drivers, 6 channels ADC, local oscillator. The goal is indeed to avoid putting any unnecessary electronics in the radiation sensitive area: corresponding author.

Parallel session A2 - ASICs / 53

SPIROC (SiPM Integrated Read-Out Chip): Dedicated very front-end electronics for an ILC prototype hadronic calorimeter with SiPM read-out

Christophe de La taille 1 ; Frédéric Dulucq 1 ; Gisèle Martin-Chassard 1 ; Julien Fleury 1 ; Ludovic Raux 1 ; Michel Bouchel 1 ; Stéphane Callier 1

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SPIROC embeds cutting edge features that fulfill ILC final detector requirements. It has been realized in 0.35m SiGe technology. It has been developed to match the requirements of large dynamic range, low noise, low consumption, high precision and large number of readout channels needed.
SPIROC is an auto-triggered, bi-gain, 36-channel ASIC which allows to measure on each channel the charge from one photoelectron to 2000 and the time with a 1 ns accurate TDC. An analogue memory array with a depth of 16 for each channel is used to store the time information and the charge measurement. A 12-bit Wilkinson ADC has been embedded to digitize the analogue memory content (time and charge on 2 gains). The data are then stored in a 4kbytes RAM.

Summary:
The SPIROC chip is a dedicated very front-end electronics for an ILC prototype hadronic calorimeter with Silicon photomultiplier (or MPPC) readout. This ASIC is due to equip a 10,000-channel demonstrator in 2009. SPIROC is an evolution of FLC_SiPM chip used for the ILC analogue hadronic calorimeter physics prototype. It was submitted in June 2007 and the test started in September 2007. It embeds cutting edge features that fulfill ILC final detector requirements. It has been realized in 0.35 μm SiGe technology. It has been developed to match the requirements of large dynamic range, low noise, low consumption, high precision and large number of readout channels needed.
SPIROC is an auto-triggered, bi-gain, 36-channel ASIC which allows to measure on each channel the charge from one photoelectron to 2000 and the time with a 1 ns accurate TDC. An analogue memory array with a depth of 16 for each channel is used to store the time information and the charge measurement. A 12-bit Wilkinson ADC has been embedded to digitize the analogue memory content (time and charge on 2 gains). The data are then stored in a 4 kbytes RAM. A very complex digital part has been integrated to manage all these features and to transfer the data to the DAQ which is described on.
This new electronics readout is intended to be embedded in the detector. One important feature is the reduction of the power consumption. The huge number of electronic channels makes crucial such a reduction to 25 μWatt per channel using the power pulsing scheme, possible thanks to the ILC bunch pattern: 2 ms of acquisition, conversion and readout data for 198 ms of dead time. However, to save more power, during each mode, the unused stages are off. After an exhaustive description, the extensive measurement results of that new front-end chip will be presented.

Parallel Session B5 - Power / 67

Serial Powering of Silicon Strip Modules for the ATLAS Tracker Upgrade

Peter Phillips¹

¹ Particle Physics

The costs, difficulties and inefficiencies associated with the cabling of silicon detector systems are well known. Serial Powering is an elegant solution to these issues and is being actively pursued by the ATLAS Tracker upgrade community.

Demonstrator supermodules have been produced using the ABCD chip from the present ATLAS SCT together with serial powering circuitry built from commercial components. Two 6 module supermodules have been built, and construction of a third supermodule to a 30 module design is in progress. Recent results from these supermodules will be presented.

Elements of the serial powering scheme have been incorporated into new ASIC designs, and studies of system issues such as protection schemes have advanced greatly. Time permitting, these developments and their application to the next demonstrator supermodule will also be outlined.

Summary:
In the current generation of silicon detector systems for particle physics experiments, it has generally been considered best practice to power each detector module independently. For example, the present ATLAS SCT detector uses 4088 independent power supply channels and cable chains, one for each detector module. Physically routing the cables into the detector volume can be a major challenge in itself, and with return path cable resistances of order 4.5 ohms power efficiency is generally poor due to thermal losses in the cables.
Independent powering is not a practical solution for future detectors, where the total channel count may be expected to increase by a further order of magnitude. The ATLAS Tracker upgrade community are actively pursuing the serial powering alternative.

With serial powering, a number of detector modules are connected together in series to a constant current source. Each module has its own shunt regulator and power transistor combination to provide digital power and a linear regulator is used to provide analogue power. Each module will now be at a different potential with regard to the off detector readout electronics, so it is also necessary to provide AC or opto coupling for all clock, command and data signals.

Demonstrator "supermodules" have been produced to two designs using the ABCD chip from the present ATLAS SCT together with serial powering circuitry built from commercial components. The first design uses six modules, each with 4 chips coupled to 6cm strip sensors, together with an implementation of serial powering circuitry in the form of a small PCB. In the more recent design, which comprises (up to) thirty modules with 3cm strip sensors, the serial powering circuitry has been integrated into the 6 chip hybrid. Recent results from these demonstrator supermodules will be presented.

Looking ahead, elements of the serial powering scheme have been incorporated into the ABCn readout ASIC and the SPI serial powering chip. Protection schemes have been developed such that, in the event that a single module should fail, the remainder of the modules in the chain may continue to operate, and the design of a custom, constant current power supply has been started. Time permitting, these developments and their application to the next demonstrator supermodule will also be outlined.

OPTO ELECTRONICS WORKING GROUP / 167

Setting up optical links for ATLAS SCT

Parallel session B2 - Optoelectronics / 88

Single-Event Upsets in Photodiodes for Multi-Gb/s Data Transmission

Author(s): Jan Troska
Co-author(s): Alberto Jimenez Pacheco ; Christophe Sigaud ; Daniel Ricci ; Francois Vasey ; Luis Amaral ; Paschalis Vichoudis ; Stefanos Dris

A Single-Event Upset study has been carried out on PIN photodiodes from a range of manufacturers. A total of 22 devices of eleven types from six vendors were exposed to a beam of 63MeV protons. The angle of incidence of the proton beam was varied between normal and grazing incidence for three data-rates (1.5, 2.0 and 2.5Gb/s).

We report on the cross-sections measured as well as on the detailed statistics of the interactions measured using novel functionalities in a custom-designed Bit Error Rate Tester. Upsets lasting for multiple bit periods have been observed and the fraction of errors when a logical zero is transmitted has been measured to be less than one over a large range of input optical power.

Summary:

Single Event effects have been widely documented to occur in the photodiodes typically used in modern high-speed serial communications. At CERN, we are currently designing the next generation of optical data transmission link operating at multi-Gb/s rates for reading-out and controlling particle physics detectors to be operated at CERN’s upgraded Super Large Hadron Collider (SLHC). The innermost regions of the detectors will encounter a radiation environment with particle fluxes of $10^6 \text{ particles/cm}^2/s$. The control information flowing into the detectors from shielded control rooms is crucial for maintaining the synchronization of the data-taking system. It is therefore of critical importance that this control information be transmitted error-free and, with the knowledge that Single Event
Upsets (SEUs) will occur within a photodiode placed in such an environment, the use of Forward Error Correction (FEC) coding will be mandatory. Validation of any choice of FEC code depends upon a detailed knowledge of the statistics of the expected errors and the test reported in this paper aims to gather that knowledge.

We have performed a small survey of the radiation-response of several different devices. InGaAs PIN photodiodes operating at 1310nm, GaAs PIN photodiodes operating at 850nm were combined in this test with Receiver Optical Sub-Assemblies (ROSA) where the Transimpedance Amplifier (TIA) is mounted in the same TO-can as the photodiode. Again, both 1310nm InGaAs and 850nm GaAs ROSAs were included.

The irradiation was carried out at the PIF-NEB facility at the Paul Scherer Institut, Villigen, Switzerland using a 63MeV proton beam. Ten photodiodes were arranged on a rotating axle to be tested simultaneously. Data were taken at 0°, 10°, 80° and 90° angles of incidence with a flux of approx. $8 \times 10^8$ p/cm$^2$/s. A custom BERT was implemented in a Stratix II GX FPGA with embedded high-speed transceivers. The primary testing goal of measuring error statistics was achieved through the use of an error log memory that could hold up to 8K 20bit words containing the XOR of transmitted and received data in the case an error was detected anywhere in that word along with a timestamp corresponding to each error word. Firmware was developed that would allow operation at the three data rates used in the test (1.5, 2.0 and 2.5Gb/s) by simply supplying a different frequency base clock to the FPGA.

Measurements of the detailed statistics of error events due to proton strikes in PIN photodiodes will be presented. These show that multiple bit-errors do occur and will have to be mitigated using FEC coding in data-links for future particle physics detectors operating at CERN’s SLHC.

Bursts of errors lasting for multiple bit periods have been observed. The long length of bursts observed ROSAs could be due to upsets taking place in the TIA. A particle strike in a bias circuit of the TIA could dramatically reduce its gain, leaving the output in an fixed state and causing the receiver of the FPGA detect only noise at its input. In contrast, short bursts lasting for up to 20 consecutive bit periods seem to be related to upsets in the photodiodes, since we observe a dependence on the received power level.

To the best of our knowledge this kind of behaviour, where an SEU upsets several successive bits, has not been previously reported in SEU tests performed with photodiodes at other data rates.

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**Parallel session A2 - ASICs**

**Status Report on the LOC ASIC**

Jingbo Ye$^1$

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The LOC ASIC is a serializer for data transmission. This ASIC development is supported by US-ATLAS upgrade program, and is based on a 0.25 μm Silicon on Sapphire technology. Characterization tests on the technology and the first prototype LOC1 have been carried out both in lab and in irradiation tests. Measurement results on jitter and Bit Error Rate of the ASIC as well as the TID and SEE effects will be reported. Design considerations, specifications and simulation results on the second prototype LOC2 will be discussed.

**Summary:**

A test-chip has been designed and fabricated to evaluate a 0.25 μm Silicon-on-Sapphire technology for ASIC developments for detector front-end electronics. TID tests using gamma irradiation from a Co-60 source have been carried out on NMOS and PMOS transistors with different layouts on the test-chip. With a floating substrate, different leakage current sources are identified. Threshold voltage shifts are also observed. With an electrically biased substrate, one can “dial” up or down leakage currents in NMOS or PMOS with the potential applied to the substrate. When the substrate is grounded, the leakage currents in NMOS and PMOS are both very small, and the threshold voltage shifts are also reduced compared with the floating substrate case. A crude model has been proposed to explain the observations and a more precise simulation or modeling is needed. More tests are also needed. These tests and modeling work will be carried out in the time from 2008 to 2010.

The first prototype of the LOC ASIC, LOC1 has been measured in lab and in a 200 MeV proton beam at IUCF. The in-lab studies include jitter analysis, bit error rate scan (the bathtub curve) and the eye diagram measurement. In the jitter study, different jitter components are analyzed and their sources identified. The BER measurement of LOC1 is carried out with a 12G BERT and the best BER is found to...
be $5\times10^{-11}$ in the bathtub scan running at 2.5 Gbps. The eye diagram of the serial bit stream is measured, and from which the signal amplitude, rise and fall times are obtained. Many lessons in the design of LOC1 have been learned and that will help in the LOC2 design. Using TLK2500 as the de-serializer and running at 2.5 Gbps, SEE on LOC1 is measured with a 200 MeV proton beam and the preliminary result indicates that the proton induced SEE has a cross section less than $1\times10^{-10}$ cm$^2$/proton. Data analysis is still on-going. More tests are planned for the summer or fall of 2008. The SEE measurement results will be reported.

A LOC2 design specification is being reviewed in the ATLAS LAr and Inner Detector upgrade communities. This specification will be presented together with the LOC2 design. In the LOC2 design, we try to incorporate the Versatile Link as the LOC’s optical interface. Design simulation has been carried out and preliminary results indicate that we may be able to decrease the jitter and increase the serial data speed in LOC2. This design and simulation work is on-going and the latest results will be reported. A schedule on LOC2 will also be discussed.

**Parallel Session A5 - Installation & Commissioning / 94**

**Studies of the Assembled CMS Tracker**

**Author(s):** Kristian Hahn¹; Pieter Everaerts¹

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During the latter months of 2006 and the first half of 2007, the CMS Tracker was assembled and operated at the Tracker Integration Facility in Building 186 at CERN. During this time, several dedicated studies were carried out to validate the performance of the tracker after assembly, testing general noise performance, potential interference between subdetectors, and performance at high acquisition rates. We report on the results of these studies and their consequences for operation of the Tracker at the experiment.

**Summary:**

The CMS collaboration has designed and constructed a completely silicon-based tracking system for the initial running period of the Large Hadron Collider. This tracker by any measure is much larger than any tracker built previously, which required meticulous attention to detail during the design and construction process. As a result, the detector "as built" performance is more than adequate to produce the data quality required for success at the LHC. Building a good detector is a necessary but not sufficient condition to guarantee performance in operation, and silicon detectors have been known to exhibit unforeseen operational problems after construction, which are not amenable to repair due to the lack of accessibility. To guard against this possibility, the Tracker group made a large effort to test as much of the functionality of the tracker as possible during operations at the Tracker Integration Facility (TIF) before installation at the experiment.

The first tests at the TIF were functionality tests of each of the components after integration. These tests showed the high level of quality in terms of noise and bad channels established during construction persists after integration. However, the TIF also afforded a first look at the assembled tracker system. First, the final power supply components allowed the study of different grounding schemes. This is crucial for the Outer Barrel of the Tracker (TOB), which is susceptible to noise pickup on particular modules from a coupling of the power distribution to the front end electronics. The noise profiles for the TOB were studied as a function of different grounding schemes, producing an optimal final configuration for the experiment. Also, at the TIF for the first time one could run the Tracker Inner Barrel (TIB), TOB, and Endcaps (TEC) simultaneously, to assess any potential interference between one subdetector and another. These studies found no evidence of crosstalk between the different subdetectors.

The TIF also provided the opportunity to test at high readout rates expected during operations. To accomplish this, a small slice of the CMS Event Builder system was constructed, and data was taken at rates up to 100 kHz. These studies uncovered a source of increased occupancy not visible at low rate. The source was traced to the pickup in the APV front end electronics chip due to the interplay between simultaneous readout and acquisition for specific timing separations sampled at rates above
20 kHz. The signature of the effect is a simultaneous anticorrelated excursion from the pedestal for channel 0 and 127, where one goes low and the other high, resulting in a fake cluster similar to a MIP signal for the channel which swings high. The effect occurs in all APV chips and therefore all subdetectors simultaneously, but is localized to the edge channels, and the scale varies from chip to chip due to geometry. Thus, for particular timing intervals between two acquisitions the event occupancy is increased dramatically, which impairs downstream pattern recognition. Potential solutions for this problem are under development.

Parallel session B2 - Optoelectronics / 44

Study of radiation hardness of PiN diodes for Atlas pixel detector

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Co-author(s): Flera Rizatdinova ¹; Patrick Skubic ²; k.k Gan ³

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The ATLAS has started the upgrade project to address the upgrade of the LHC luminosity by factor of 10. ATLAS pixel tracker employs optical links for communication between the sensors and data acquisition. We study the radiation hardness of PiN diodes which are part of the optical link. These components were irradiated by 200 MeV protons up to 40 MRad and by gamma source up to 10 MRad. The responsivity, dark current of PiN diodes are measured as a function of the radiation dose.

Summary:

We discuss the radiation tolerance of the silicon and GaAs PiN diodes that will be part of the readout system of the ATLAS upgraded pixel detector. The components were irradiated by gamma source up to 10 MRad and by 200 MeV protons up to 40 MRad. We study the radiation hardness of PiNs as a function of the optical sensitive area and of their cut off frequency. The dark current of PiN diode candidates is measured before and after irradiation, and the response of the PiN diodes was monitored as a function of the radiation dose.

POSTERS SESSION / 23

Sub-Nanosecond Machine Timing and Frequency Distribution Via Serial Data Links

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Co-author(s): Andrea Borga ¹; Javier Serrano ²; Matt Stettler ²; Matthieu Cattin ²

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FERMI@ELETTRA is a 4th generation light source under construction at Sincrotrone Trieste. It will be operated as a seeded FEL driven by a warm S-band Linac which places very stringent specifications on control of the amplitude and phase of the RF stations. The local clock generation and distribution system at each station will not be based on the phase reference distribution but rather on a separate frequency reference distribution which has significantly less stringent phase stability.
requirements. This frequency reference will be embedded in the serial data link to each station and has the further advantage of being able to broadcast synchronous machine timing and clocking signals with sub-nanosecond temporal accuracy. This paper describes the design of new RF controls, and specifically the architecture used to distribute the frequency reference along with the precision machine timing and clocking signals.

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Subgroup A Report

Lessons learned and to be learned from the LHC
17:30 Lessons learned from CMS (10') Daniel Ricci (CERN)
17:40 Lessons learned from ATLAS (10') Anthony Weidberg (Oxford)
17:50 Discussion

Parallel Session B5 - Power / 20

System test with DC-DC converters for the upgrade of the CMS silicon strip tracker
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Due to the increase in granularity and higher complexity of the front end electronics needed at the SLHC, an upgrade of the CMS silicon strip tracker is expected to require even more power than the current CMS strip tracker. However, the space available for cables will remain the same as today. In addition, a further increase of the material budget due to cables and cooling is not acceptable from the physics point of view. Novel powering schemes such as serial powering or usage of DC-DC converters have been proposed to solve the problem.

Since custom DC-DC converters that satisfy the requirements of radiation hardness and magnetic field tolerance are not available yet, we have operated substructures of the current CMS strip tracker with off-the-shelf DC-DC converters. These devices have been integrated into the CMS tracker hardware and the system performance, in particular the noise behaviour, has been studied. The results of this first operation of CMS strip modules with DC-DC converters will be presented and discussed.

POWER WORKING GROUP / 161

Technologies for a DC-DC ASIC

POSTERS SESSION / 58

Testing and calibrating analogue inputs to the ATLAS Level-1 Calorimeter Trigger
The ATLAS Level-1 Calorimeter trigger is a hardware-based system which aims to identify high-pt objects within an overall latency of 2.5us. It is composed of a Preprocessor system which digitises 7200 analogue input channels, determines the bunch crossing of the interaction, and provides a fine calibration; and two subsequent digital processors.

The Preprocessor system needs various channel dependent parameters to be set in order to provide digital signals which are aligned in time and have proper energy calibration. The different techniques which are used to derive these parameters are described along with the quality tests of the analogue input signals.

Results from first collision data are expected.

Summary:

The high luminosity and bunch-crossing rate of the LHC poses an immense challenge for triggering. The ATLAS Level-1 calorimeter trigger processes 7200 trigger towers within a fixed latency of 2.5 us, reducing the event rate from 40 MHz to below 100 kHz. It is realised completely in hardware, including ASICs and FPGAs, in a VME-based system.

The Preprocessor of the Level-1 calorimeter trigger is a compact system which digitizes the detector signals, determines the bunch crossing number of the interaction and provides a fine energy calibration. The results are sent to two digital processors, the Cluster Processor (CP) and the Jet/Energy Processor (JEP). The JEP searches for electron/photon and tau candidates. The JEP identifies jets and computes total missing transverse energy sums. Both digital processors provide the information to the Central Trigger Processor which makes the overall Level-1 decision.

The Preprocessor is a highly modular system consisting of eight crates hosting a total of 124 preprocessor modules (PPMs). Each of these modules handles 64 channels in parallel. The main signal processing is done by the custom-built Preprocessor ASIC. It is placed on the multichip modules (MCMs) hosted on a PPM. Each MCM handles four input channels.

The Preprocessor system needs various channel dependent parameters to be set in order to provide digital output data which are aligned in time and have proper energy calibration. The analogue cables from the detector frontend have length differences which amount to channel-to-channel timing differences of up to 10 bunch crossings which is corrected for by means of input shift registers. In addition to this, the fine timing of the FADC clock needs to be set with ns accuracy in order to sample the analogue pulses on their maximum which guarantees proper signal reconstruction and the maximum dynamic range. The energy of the pulses is determined by means of a FIR filter in combination with a look up table for which the corresponding coefficients and values have to be determined in order to increase the signal to noise ratio and to achieve proper calibration.
During the commissioning phase of the experiment the Preprocessor system is also used to test the signal quality of the analogue input signals since it provides independent readout for all trigger towers in parallel.

This talk gives an introduction to the Level-1 Calorimeter Trigger with a focus on the preprocessor system. The different calibration methods are described along with the quality tests of the analogue input signals. Results from cosmic muon data are presented and if possible first results from proton collisions.

Parallel session A2 - ASICs / 89

The ABCN front end chip for ATLAS Inner Detector Upgrade

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We present the design of the ABCN front end chip implemented in CMOS 0.25um technology and optimized for short, 2.5cm, silicon strip detectors intended to be used for the upgrade of ATLAS Inner Detector tracker. A primary aim of this project is to develop an ASIC with full functionality as required for readout of short silicon strips in the SLHC environment in a cost-effective and proven technology. Efforts have been put on minimization of the power consumption and compatibility with new power distribution schemes being developed for future tracker detectors. The architecture of the chip as well as critical and novel design aspects will be presented. The ABCN ASIC will serve as a basic testing vehicle in extensive programs on developments of sensor and modules for the upgrade of Inner Detector.

Summary:

A primary challenge of the trackers being developed for SLHC environment is the high occupancy, which affects directly granularity of the detectors and the number of electronic channels, to be about 10 times higher compared to the present SCT. As a result, power consumption in the readout ASICs is one of the most critical issues on top of usual requirements concerning noise and radiation resistance. Optimizing the ASIC design with respect to power consumption is by itself not sufficient to solve the problem of power dissipation in the detector and alternative power distribution schemes are being investigated. The ABCN chip is a silicon strip binary readout chip which follows the architecture of the ABCD3T design implemented in BiCMOS DMILL technology and used in present ATLAS SCT detector. A new front-end circuit optimized for short strips has been developed with a primary goal to reduce the power consumption while maintaining the required noise and timing performance of the circuit. The preamplifier stage is built with a classical cascode stage with NMOS input transistor and an active feedback circuit employing PMOS transistor working in saturation and biased in moderate inversion region. Dimensions of the input transistor, 320um/0.5um, are optimized for an input capacitance of 5pF using the EKV model parameterization. The significant reduction in the overall power consumption of the front end part has been achieved by compromising the bias currents in the buffers, shaper and discriminator stages, which undesirably pronounced the influence of the parasitic capacitances on the overall shaping function of the front end. The final adjustment of capacitances in the filtering stages was done with Spice simulations, taking into account all parasitic capacitances extracted from the layout of the chip. The analogue gain at the discriminator input is 100mV/FC and the intrinsic peaking time of the circuit is 22ns what ensures 25ns peaking time including the effect of charge collection. The front end circuit can accept input signal of any polarity and provides good linearity up to +/-10fC input charges. For the nominal consumption of 0.7mW per channel, the calculated ENC for 5pF detector capacitance will be below 800e-, which allows the use of this front end with heavily irradiated silicon detectors having low charge collection efficiency and high leakage current. The functionality in the digital part of ABCN is very similar to the ABCD3T one, used in the present ATLAS tracker. Changes have been made to accommodate a simpler redundancy schema, which costs less
in number of tracks on the hybrid, and different readout rates. SEU detection and correction circuitry have been added. Because the power consumption of the digital part is becoming dominant, special features have been implemented to measure and control the power consumed by the functional parts. The new design includes on-chip power management circuitry to make it compatible with recent developments in the area of power distribution for the Inner Detector upgrade, namely DC/DC conversion schemes and serial powering scheme. On the ABCN chip we have implemented two prototypes of shunt regulators with scalable architecture capable to generate local power supply in case of serial powering of the detector modules. The on-chip any-capacitor stable linear voltage regulator provides the voltage supply for the sensitive front end part of the chip. It is optimized for high supply rejection ratio, achieving 33dB at 30MHz with 100nF decoupling capacitor. It provides immunity against the switching noise in case of the DC/DC converter power source, and separates the analogue voltage from the common voltage provided for both the analogue and digital circuits by the shunt regulator in the case of serial powering.

Parallel Session B3 - Machine-Experiment, BCM / 133

The ATLAS Beam Condition Monitor Commissioning

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The ATLAS Beam Condition Monitor (BCM) based on radiation hard pCVD diamond sensors and event-by-event measurements of environment close to interaction point \((z=\pm 184\text{ cm}, r=5.5\text{ cm})\) has been installed in the Pixel detector since early 2008 and together with the Pixel detector in the ATLAS cavern since June 2007. The sensors and front end electronics was shown to withstand 0.5 Mrad and \(10^{15}\) particles/cm\(^2\) expected in LHC lifetime. Recently the full readout chain, partly made of radiation tolerant electronics, still inside of the ATLAS spectrometer and partly in the electronics room, was completed and the system is now ready for the first LHC single beams as well as first collisions this summer.

Summary:

The ATLAS Beam Condition Monitor (BCM) is based on radiation hard polycrystalline chemical vapor deposition (pCVD) diamond sensors and off the shelf monolithic amplifiers both tested to withstand the harsh radiation environment in ATLAS close to interaction point. They were proven to be operational after large dose of 0.5 Mrad and flux of \(10^{15}\) particles/cm\(^2\) which is expected for the LHC lifetime. Eight modules were installed symmetric around the interaction point four on each side at \(z=\pm 184\text{ cm}\) and at \(r=5.5\text{ cm}\) equally spaced in polar angle around the beam-pipe at phi=0, 90, 180 and 270 degrees. It has been installed in the Pixel detector since early 2008 and together with the Pixel detector in the ATLAS cavern since June 2007.

The amplified signal from diamond sensors of sub ns rise-time and width of order of 2 ns is transformed into time-over-threshold measurement in electronic board based on NINO chip originally developed for ALICE experiment. The chip preserves the excellent timing characteristics of the input signal and encodes input signal amplitude into the output signal width. The signals are then taken over optical fibers to FPGA based readout board for further processing.

The ATLAS BCM primary goal is measurement of environment close to the interaction point in ATLAS spectrometer. It will distinguish normal interactions from background events caused by beam particles hitting collimators or beam gas on the basis of timing measurement and absolute rate measurement. The background events coming from one side will cause signals of different arrival times on one side of interaction point than on the other. One type will precede the other for 12ns, about half of bunch to bunch time spacing, due to position of the modules chosen.

In addition ATLAS BCM will be able to trigger interesting events that will happen in ATLAS at pseudo-rapidity of approximately 4. It fits its trigger information into 9 bits in the central trigger processor. Furthermore, each of triggered events in ATLAS will have also full record of eight BCM modules including the time of arrival of the particle at the sensor as well as the amplitude encoded in the width of the signal.
The noise performance of the full system was tested in situ and compared with reference results from test-beams and laboratory measurements. Parts of the system were previously tested successfully in various test-beams and through comprehensive QA procedures. The system is ready for the first single LHC beam measurements as well as for the first proton-proton collisions.

Parallel Session B3 - Machine-Experiment, BCM / 121

The ATLAS Radiation Dose Measurement System and its Extension to SLHC Experiments

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In LHC experiments, a precise measurement of the radiation dose at various detector locations is crucial. In ATLAS, this task is performed by a set of radiation monitors (RADMON) which are able to record Non-Ionising Energy Loss (NIEL), the Total Ionizing Dose (TID) and measure fluences of thermal neutrons. These measurements are vital for understanding the changes in detector performance during ATLAS operation, verifying simulations and optimising the operation scenario. The RADMONs are multi-sensor boards, containing several RADFETs, diodes and DMILL transistors. It is clear that a similar system will be of even greater importance for SLHC environments due to the increased radiation dose.

Summary:

In the ATLAS experiment, accumulated radiation doses are measured online at several locations in the detector. The measurement is provided by Radiation Monitor Sensor Boards (RMSB) that are realised as multi-sensor units. Different sensors are used to measure the Non-Ionising Energy Loss (NIEL), Total Ionizing Dose (TID) and fluence of thermal neutrons. The highest radiation levels will occur in the ATLAS Inner Detector (ID) around the pp-collision point.

In the ID, RMSBs will be placed at 14 locations and will provide on-line information of ionization dose in SiO₂, NIEL in silicon Radiation Field Effect Transistors (RADFETs) and damage to the DMILL bipolar transistors from which fluence of thermal neutrons can be estimated. Mainly due to the very uncertain temperature conditions at some locations in the ID, where the expected temperatures are between -20 and +20°C, the RMSBs were made of ceramics. They provide mechanical support and electrical connection for the sensors and the bottom side of the ceramics is covered with a thin layer of material with electrical resistance R = 320 Ohm which serves as the heater. The heater enables us to keep the board at a constant temperature a few degrees above 20°C.

Due to the large range of doses, very limited access, and relatively low number of RMSB locations due to limited space, RMSBs in the Inner Detector will host a number of radiation detectors which will cover the entire range of expected doses and provide a high level of redundancy. Outside the Inner detector the range of expected dose levels are smaller therefore TID and NIEL damage will be measured with simplified version of RMSBs containing only two sensors, one for each type of radiation damage (TID and NIEL). There are around 50 locations for RMSBs: 24 in the ATLAS calorimeters (6 in TILE and 18 in LAr), 10 for electronics at PP2, 16 in Muon forward detectors.

We will report on the status of the radiation monitoring project in ATLAS, and discuss a possible extension of the system to the radiation doses as expected for the experiments at the SLHC.

POSTERS SESSION / 105

The Alice Pixel Trigger Control and Calibration

Alexander Kluge; Cesar Torcato De Matos; Fernando Ribeiro; Gianluca Aglieri Rinella; Peter Chochula
The ALICE Silicon Pixel Detector (SPD) optical data stream includes 1200 Fast-OR signals indicating the presence of at least one pixel hit in each of the detector readout chips. The Pixel Trigger (PIT) extracts the Fast-OR signals from the data lines and processes them to contribute to the Level 0 trigger in the ALICE Central Trigger Processor (CTP).

We present here the design, the implementation and the first operational experience of the PIT Control and Calibration system.

The PIT control system includes original hardware and software solutions to implement coordinated operation of the PIT with the various ALICE systems to which it interfaces to.

Summary:

The ALICE Silicon Pixel Detector (SPD) comprises the two innermost layers of the ALICE inner tracker system. The SPD contains 120 detector modules each including 10 readout chips. Each of these pixel chips generates a digital Fast-OR output signal indicating the presence of at least one pixel hit in its pixel matrix.

The Pixel Trigger (PIT) System has been implemented to process the 1200 Fast-Or signals from the SPD and provides an input signal to the ALICE Central Trigger Processor (CTP) for the fastest (Level 0) trigger decision within a latency of 800 ns.

The PIT processor interfaces with several ALICE systems: it receives input data from the SPD, it accepts configuration commands from the CTP and sends status information to the Alice Experimental Control System (ECS).

The PIT control system required an accurate design of hardware and software solutions to implement coordinated operation of the PIT and the ALICE systems to which it interfaces to.

We present here the design, the implementation and the first operational experience of the PIT Control and Calibration system.

The hardware configuration and control are implemented via the ALICE Detector Data Link, on top of which a custom control system has been implemented.

A driver layer has been realized under stringent requirements of robustness and reusability. It qualifies as a general purpose hardware driver for electronic systems equipped with the ALICE DDL front end board (SIU).

Various testing and calibration procedures need to be performed on the SPD and the PIT systems in order to provide an optimized trigger signal to the CTP.

These include methods to compensate all signals propagation delays and automatic SPD DAC scans to tune the detector response.

The PIT control system has been tailored to implement automatically most of the former procedures, requiring coordinated and extensive information exchange between the interfacing systems.

POSTERS SESSION / 48

The Associative Memory for the Self-Triggered SLIM5 Silicon Telescope

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Co-author(s): collaboration SLIM5

Modern experiments search for extremely rare processes hidden in much larger background levels. As the experiment complexity and the accelerator backgrounds and luminosity increase we need increasingly complex and exclusive selections to be efficient selecting the rare events inside the huge background. We present a fast, high-quality, track-based event selection for the self-triggered SLIM5 silicon telescope. This is an R&D experiment whose innovative trigger will show that high rejection factors and manageable trigger rates can be achieved using fine-granularity, low-material tracking detectors. The system performances will be measured on a test beam, using noisy conditions to simulate high-occupancy.

This strategy requires massive computing power to minimize the online execution time of complex
tracking algorithms. Affordable latency and rates are provided by a dedicated device, the Associative Memory (AM). The time consuming pattern recognition problem, generally referred to as the "combinatorial challenge", is beat by the AM exploiting parallelism to the maximum level: it compares the event to precalculated "expectations" (pattern matching) at once. This approach reduces to linear the typical exponential complexity of the CPU-based algorithms. The problem is solved by the time data are loaded into the AM devices.

We describe the AM-based trigger and its performances.

Summary:

I. INTRODUCTION

Any L1 tracking strategy has to be conceived before the detector readout design is frozen because the possibility to trigger needs to be built directly inside the detector. The SLIM5 experiment [1] puts together many innovative techniques to demonstrate the feasibility of a low-material silicon telescope, provided of a continuous data driven readout [2] and a low-latency track-based trigger capability. The key device to provide reconstructed tracks in a very short time is the Associative Memory [3] (AM) that associates the silicon hits from the 6 telescope layers into high spatial resolution track candidates. The real challenge in a large detector is to make a large amount of tracker data available to the AM processor in a very short time. The latency strongly depends on the time necessary to load the data in the AM system. For this reason we send data to the trigger exploiting a parallel readout of the detector layers.

Any hit will be identified by a word defining both the position in the detector and the time-stamp (bunch crossing number). The engine is an AM chip where all possible tracks have been previously loaded. Each stored hit pattern is provided with the necessary logic to compare itself with the event.

We plan to use the AM chip developed for the CDF experiment [4]. It runs at 50 MHz with 6 parallel buses of 18 bits encoding each.

II THE TRIGGER ARCHITECTURE

The trigger system for SLIM5 is made of a single 9U VME board, called AMbslim. It is an evolution of two previous versions: it has (a) the very powerful input bandwidth of the first one (4 Gbit/s), developed with FPGA AM chips for an LHC online track processor [5], and (b) the much more powerful pattern bank of the second version [6] developed with standard cell AM chips for the CDF experiment.

The AMbslim has a modular structure, consisting of 4 smaller boards, the Local Associative Memory Banks (LAMB). Each LAMB contains 32 Associative Memory (AM) chips, 16 per face. The AM chips come in PQ208 packages, and contain the stored patterns with the readout logic. They are connected into four 8-chip pipelines on each LAMB. Found tracks flow down in the 4 pipelines and are collected and merged in a single stream by the GLUE chip placed on top of the LAMB.

The board has a flexible control logic placed inside a single, very powerful FPGA chip (Virtex II pro xc2vp100, with a 1696 pin package [7]). The FPGA flexibility allows the use of the same hardware in different applications characterized by short- or long-latency trigger decisions. In the case of long-latency very large associative memory banks can be obtained exploiting pipelining of boards and AM chips. For low-latency applications, instead, we use only the AM chips directly connected to the GLUE. It is possible to assign different events to different AM chips. SLIM5 needs a low-latency trigger decision, so we focus on this particular use of the AMbslim board.

III AMBSLIM PROTOCOL

The AMbslim board receives all the incoming Hits on the six input buses from the P3 connector, distributes them to all the AM chips on the board, collects and sends all the fired tracks to the output through the P3 connector. All the input hit buses and the output track bus go through the AM control chip that controls the event synchronization and format.

An End Event word signals the end of hits and tracks belonging to a particular event. Each board input is provided with a deep FIFO for event synchronization. If, occasionally, a FIFO becomes "Almost Full", a HOLD signal is sent to the upstream board, which suspends the data flow until more FIFO locations become available. The Almost Full threshold is set to give the upstream board plenty of reaction time. When the AMbslim starts to process an event, the hits are popped in parallel from the six hit input FIFOs. Popped hits are simultaneously sent to the four LAMBs. In the SLIM5 application the AMbslim clock is 40 MHz, equal to the AM chip clock and each hit is sent to all the LAMBs in the same clock cycle. However, for more demanding conditions it is possible to allocate different LAMBs to different events and distribute only the right hits to each LAMB. If for the incoming hit distribution we use an FPGA clock four times more aggressive (200 MHz) than the AM chip clock, we can process different events in parallel and increase the trigger performances.

Data from different streams are checked for consistency: upon detection of different event sequences, a severe error is asserted and the whole system needs to be synchronized again. As soon as hits are downloaded into a LAMB, locally matched tracks set the request to be read out from the LAMB (Data Ready). When the end-event word is received on a hit stream, no more words are popped from that FIFO.
until the end event word is received on all hit streams. Once the event is completely read out from the hit FIFOs, the LAMBs make the last matched tracks available within few clock cycles. When all tracks have been read out, the AM bank of the completed event is reset to be downloaded again with a new event.

Hits and tracks flow on a custom backplane through the P3 connector. We use the LVDS (Low Voltage Differential Signaling) Serializer-Deserializer DS90CR287/288A chips from National Semiconductor to decrease the number of necessary connections and to maintain a good noise rejection. 28 TTL signals are serialized by each chip into 4 LVDS signals (8 connector pins) and transmitted together with the synchronous clock to the receiving board.

IV CONCLUSION

The SLIM5 trigger system provides track reconstruction in a six layer silicon detector telescope, exploiting the detector full resolution, with a very low latency. We present the trigger architecture and performances.

V REFERENCES


POSTERS SESSION / 82

The CMS Low Voltage System

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The power system for the on-detector electronics of the CMS Experiment comprises approximately 12000 low voltage channels, with a total power requirement of 1.1 MVA.

The radiation environment inside the CMS experimental cavern combined with an ambient magnetic field reaching up to 1.3 kGauss at the detector periphery severely limit the available choices of low voltage supplies, effectively ruling out the use of commercial off-the-shelf DC power supplies. Typical current requirements at the CMS detector front end range from 1A-30A per channel at voltages ranging between 1.25V and 8V. This requires in turn that the final stage of the low voltage power supply be located on the detector periphery.

Power to the CMS front-end electronics is stabilized by a 2 MVA UPS located in a CMS surface building. This UPS isolates the CMS detector from disturbances on the local power grid and provides for 2 minutes of autonomy following a power failure, allowing for an orderly shutdown of detector electronics and controls.

This talk will describe the design of the CMS Low Voltage system, review the process of its installation and commissioning, and present the first results of noise measurements performed on the detector.

Summary:

The power system for the on-detector electronics of the CMS Experiment comprises approximately 12000 low voltage channels, requiring 1.1 MVA of power at the entrance to the CMS facility at CERN.
The radiation environment inside the CMS experimental cavern combined with an ambient magnetic field reaching up to 1.3 kGauss at the detector periphery severely limit the available choices of low voltage supplies, effectively ruling out the use of commercial off-the-shelf DC power supplies. The preparation for data-taking at the LHC experiments required a dedicated development effort by manufacturers specializing in equipment for high-energy physics, in coordination with the electronics design staff of the individual experiments.

Typical current requirements at the CMS detector front end range from 1A-30A per channel at voltages ranging between 1.25V and 8V. This requires in turn that the final stage of the low voltage power supply be located within ~10m of the front-end electronics, that is, on the detector periphery.

The CMS detector has a diameter of 15m and a length of 21.5m. It is built around an iron yoke weighing 12500 tons. The central section supports the cryostat of a 4 Tesla superconducting solenoid. The yoke functions as the main structural element of CMS and serves as the flux return path for the solenoid.

The detector is segmented into 13 sections. The central section (which supports the solenoid) is stationary, while the others can move up to 10m in the longitudinal direction. This allows the detector to be opened up for access to subdetector assemblies mounted on and inside the yoke. All cables to the 12 movable sections pass through flexible cable chains in trenches beneath the detector. The cable paths between the on-detector electronics and the power distribution area in the service cavern (adjacent to the CMS detector and shielded from it by concrete) are typically 100m-140m in length.

Power to the CMS detector is supplied through these cables at voltages of 385VDC or 230VAC and 380VAC three phase, depending on the system. No neutral is distributed for the three-phase AC systems. The on-detector power supplies, in turn, provide an output voltage between 1V and 8V for the detector front-end electronics.

Power to the CMS front-end electronics is stabilized by a 2 MVA UPS located in a CMS surface building. This UPS isolates the CMS detector from disturbances on the local power grid and provides for 2 minutes of autonomy following a power failure, allowing for an orderly shutdown of detector electronics and controls.

Following the UPS stage, power is fed to the underground power distribution area, which contains isolation transformers, static compensators, distribution switchgear and banks of rectifier units providing 385VDC, as well as electronics for monitoring and control of the system.

This talk will describe the design of the CMS Low Voltage system, review the process of its installation and commissioning, and present the first results of noise measurements performed on the detector.

POSTERS SESSION / 32

The Common Infrastructure Control of the Atlas experiment

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ATLAS is the largest particle detector at the new accelerator Large Hadron Collider (LHC), scheduled to start operations in summer 2008 at CERN in Geneva, Switzerland. ATLAS will study proton-proton collisions at the unprecedented energy of 14TeV. In order to guarantee efficient and safe operation of the ATLAS detector, an advanced Detector Control System (DCS) has been implemented. With more than 150 PCs, the DCS is a highly distributed system, hierarchically organized for operating the detector. An important role is played by the Common Infrastructure Control (CIC), supervising the experimental area. The CIC provides monitoring and control for the environment in the cavern and in the counting rooms, all common services like cooling and ventilation, electricity distribution, gas and cryogenic systems. Distributed I/O concentrators, called Embedded Local Monitor Boards (ELMB), have been developed to operate under the special conditions of the experiment such as strong magnetic field and ionizing radiation. They are used for a variety of applications and are geographically distributed over the whole experiment. The communication is handled via the Controller Area Network (CAN) fieldbus using the CANopen protocol. Data is managed by the CIC control station where a commercial Supervisory Control And Data Acquisition (SCADA) package
runs. Information and high level control is available to the users by a Finite State Machine (FSM) software running in the control room and information is also available on the web. The technical infrastructure of ATLAS is already continuously supervised during the commissioning phase by the CIC and ensures safe operation.

**POSTERS SESSION / 16**

**The Data Acquisition System of the MAGIC-II Telescope**

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The MAGIC telescope is the world’s largest gamma ray telescope, designed to look at the light emitted by air shower by Cherenkov effect. It is operating since 2004 at the Roque de Los Muchachos observatory, La Palma, Canary islands. MAGIC-II is the upgrade of the project, consisting of a twin telescope frame with innovative features like new photon detectors to lower the threshold energy further and an ultrafast signal sampling to reduce the effect of the diffuse night sky background. The new acquisition system is based upon a low power analog sampler (Domino Ring Sampler) with frequency ranging from 1.5 to 4.5 GHz and data are digitized with a 12 bit resolution ADC. The analog sampler, originally designed for the MEG experiment, has been successfully tested on site and showed a very good linearity and single photon discrimination capability. Data management are performed by 9U VME digital boards called PULSAR (PULser And Recorder) which handle the data compression and reformatting as well. Every board has 32 analog channels plus auxiliary digital signals for trigger and monitor purposes. For a kHz trigger rate and a 2 GHz frequency sampling, the data throughput can be as high as 100MB/s thus being a challenge for modern data transmission and storage solutions. The data are transferred to PCI memory via Gbit optical links using the CERN S-Link protocol and to the mass storage system. The Data Acquisition system design is described in detail.

**Plenary Session 2 - OPENING / 147**

**The European XFEL Project**

Ulrich Trunk

1 DESY

The European XFEL project is a 4th generation photon source to be built in Hamburg. Electron bunches, accelerated to 17.5GeV by the XFEL linac, are distributed to three SASE long undulators. There photon pulses with full lateral coherence and wavelengths between 0.1nm and 4.9nm (12.4keV and 0.8keV) are generated for three beamlines. It will deliver around 1012 photons within each 100fs pulse, reaching a peak brilliance of 1033 photons s 1mm 2 mrad 2 (0.1%BW)-1. Thus it will offer unprecedented possibilities in photon science research including nano-object imaging and studies (e.g. by coherent X-ray scattering) and ultra fast dynamic analysis of plasma and chemical reactions (e.g. by X-ray photo correlation spectroscopy). The detector requirements for such studies are extremely challenging: position sensitive area detectors have to provide a dynamic range of ≥104, with single-photon sensitivity, while withstanding radiation doses up to 1GGy (TID). Furthermore the detectors have to record data from “trains” of up to 3000 photon pulses, delivered at 5MHz, which repeat every 100ms. Three consortia have picked up the challenge to build pixel detectors for the European XFEL: DepFet, HPAD and LPD. Besides the European XFEL source and the related experimental techniques, the concepts and specialities of the DepFet, HPAD and LPD detectors are discussed.
Parallel Session A5 - Installation & Commissioning / 36

The LHCb Silicon Tracker: lessons learned (so far)

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The LHCb Silicon Tracker is part of the main tracking system of the LHCb detector. It covers the full acceptance angle in front of the dipole magnet in the Trigger Tracker station and the innermost part in the three Inner Tracker stations downstream of the magnet.

We report on final elements of the production, the installation and commissioning process in the experiment. Focusing on electronic and hardware issues we describe the lessons learned and the pitfalls encountered. First experience of detector operation is presented.

Summary:

The LHCb Silicon Tracker is part of the LHCb main tracking system and provides data for region of high track densities. For the tracking station TT in front of the main dipole magnet, the Silicon Tracker covers the full acceptance angle of the experiment, while for the stations T1-T3 after the magnet, the Silicon Tracker only covers the region directly around the beam pipe. The analogue hit information of the silicon strip detectors, which is amplified by the Beetle readout chip, is transmitted via copper cables to the Services Boxes, which are located outside the acceptance area. This does not only reduce the amount of material inside the detector but in addition relaxes the requirements to the Service Box electronics concerning radiation tolerance. The Service Boxes hold the Digitizer Boards, on which the analogue signals from the Beetle frontend chips is digitized and encoded into a Gigabit data stream for transmission via VCSEL diodes and 120 m of multi-ribbon optical fibre to the counting house. In the counting house, the optical ribbons can be directly connected to TELL1 preprocessor boards equipped with two multi-channel optical receiver cards.

We present final results from the production of the detector modules and the readout electronic boards. At this point, problems encountered during the production and lessons learned for future projects are shown. After describing the installation procedure, we report on the commissioning of the Silicon Tracker with particular focus on hardware and electronic issues.

Parallel session B1 - Trigger 1 / 114

The Level 0 Pixel Trigger System for the ALICE Silicon Pixel Detector: implementation, testing and commissioning.

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The ALICE Silicon Pixel Detector transmits 1200 Fast-OR signals every 100 ns using its 120 optical readout channels. They indicate the presence of at least one hit in the pixel matrix of each readout chip. The ALICE Level 0 Pixel Trigger system extracts, processes them and delivers an input signal to the Central Trigger processor for the first level trigger decision within a latency of 800 ns.

This contribution will describe the tests and measurements made during the qualification and commissioning phases of the system. These included Bit Error Rate tests on the Fast-OR data path, the measurement of the overall process latency and the recording of
calibration data with cosmic rays. Furthermore, the first results of the operation of the Pixel Trigger system with the SPD detector in the ALICE experiment will be presented.

Summary:

The ALICE Silicon Pixel Detector (SPD) data stream includes 1200 digital signals (Fast-OR) promptly activated on the presence of at least one pixel hit in each of the detector readout chips. This information is used in the ALICE first level (Level 0) trigger decision to improve background rejection in pp interactions and event selection in heavy ions runs. Various trigger algorithms based on topology or multiplicity of Fast-OR signals have been investigated. All of them can be implemented as boolean logic functions of the 1200 SPD Fast-OR signals on Field Programmable devices.

The Pixel Trigger system receives the entire SPD data stream on 120 optical input channels. It extracts the Fast-OR signals, processes them and delivers the result to the ALICE Central Trigger Processor for the Level 0 trigger decision. The design and the development of the Pixel Trigger system have been previously published. The Pixel Trigger system is now installed in the ALICE experiment.

This contribution will describe a set of tests and measurements realized on the Pixel Trigger system during its qualification and commissioning. Bit Error Rate measurements were made on the complete Fast-OR data path from the detector to the system processing unit. Several tests were done on the system operated together with the SPD detector. These allowed the measurement of the overall processing latency and the acquisition of cosmic ray data for calibration purposes, using the Pixel Trigger system to self-trigger the SPD on its Fast-OR outputs. The results of the first months of operation of the Pixel Trigger system with the SPD detector in the ALICE experiment will be presented.

The output of the Fast-OR processing algorithm must be provided to the Central Trigger Processor within 800 ns from the interaction. A large fraction of this time is needed for the generation, serialization and transmission of the Fast-OR signals. Only 225 ns are available for the extraction and processing of the signals in the Pixel Trigger system.

The Pixel Trigger system is based on ten optical receiver boards (OPTIN) and one processing board (BRAIN). All boards are equipped with field programmable devices (FPGA). The ten OPTIN boards connect as mezzanine boards on the processing board. The 1200 Fast-OR signals are extracted in the OPTIN boards, time multiplexed and transferred to the processing board. The processing FPGA processes them and transmits the results to the Central Trigger Processor. Different algorithms can be implemented and executed in parallel.

A secondary FPGA on the BRAIN board communicates with all the processing devices of the Pixel Trigger system and interfaces them to the control computers by the ALICE optical Detector Data Link (DDL).

The Pixel Trigger system architecture supports various user selectable algorithms. The selection of a different algorithm is allowed in between data taking runs and might require the
The Liquid Argon Jet Trigger of the H1 Experiment at HERA

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The Liquid Argon Jet Trigger, installed in the H1 experiment at HERA, implements in 800 ns a real-time cluster algorithm by finding local energy maxima, summing their immediate neighbors, sorting the resulting “jets” by energy, and applying topological conditions. It operated since the year 2006 and drastically reduced the thresholds for triggering on electrons and jets.

Summary:

We present the Jet Trigger, an upgrade of the H1 experiment Liquid Argon first level trigger.

After the luminosity upgrade of the HERA machine in the years 2000-2001 (HERA-2), a significant increase of the background rates was expected and indeed observed. While parts of the H1 detector were upgraded during the year 2001 as well, the H1 data logging rate to permanent storage (about 10 Hz) remained a stringent constraint for the data acquisition system. The aim of the upgrade of the digital part of the LAr trigger, the Jet Trigger, was to complement the existing global LAr calorimeter trigger with a system that performs real-time clustering to avoid summing-up noise distributed over large parts of the calorimeter, thus allowing for triggers on even lower energy depositions while keeping the trigger rates within the required bounds.

The Jet Trigger identifies the localized energy depositions of electrons, photons and bundles of hadrons in the LAr calorimeter, and uses these energy clusters (“jets”), including their topological information, for a fast event selection. The “jets” are found by identifying trigger towers with a local energy maximum. Around this maximum the immediate neighboring towers are summed and added to the center. The resulting local “jets” are the basis of the trigger decision. Such a local concept improves the sensitivity for low-energy depositions in the calorimeter. The “jets” are then sorted by energy in decreasing order. The 16 highest energy “jets” are used to provide flexible and optimized triggers based on discrimination of individual jet energies, counting jets with energies above certain thresholds, and determination of topological correlations between the jets.

The realization of the above algorithm was implemented in the following way. The input of the jet trigger is 1200 analog trigger towers received at the 10 MHz HERA bunch crossing rate. The clock generation is performed by a Clock Distribution and Configuration Card with adjustable phases to minimize the overall system latency. The ADC-Calculation-Storage unit digitizes the 1200 input towers to 8 bit accuracy each, transforms the energies into transverse energies, and sums the electromagnetic and hadronic energies. The resulting 440
outputs are transferred via a bit-serial link to the so-called Bump Finder Unit. This unit searches for local maxima of energy and sums them with their immediate neighbors. This search and summing is done, for each input tower, in a completely parallel fashion. The resulting 116 energy maxima are sorted by decreasing energy first quadrant-wise, then detector-wise, by the Primary and Secondary Sorting Units. The programmable Trigger Element Generator applies conditions on the 16 highest energies and their locations. These conditions are local (energy and polar angle criteria on each individual jet, azimuthal and polar angle differences between jets), and global (total energy and missing energy in the event).

In total, the Jet Trigger consists of about 550 FPGAs with 75 M Gates, computing 300 G operations/s. The 12 Gb/s raw data rate is reduced to 16 trigger element bits per bunch cross, corresponding to a data reduction factor of 600. Each unit performs its function within 1 to 3 bunch crossings. The total latency is 800 ns.

The Jet Trigger operation started in the summer of 2006 and accumulated about 100 pb⁻¹ of luminosity until the end of the HERA-2 program in July 2007. It opened the phase space for events containing a single forward jet of at least 8 GeV at low angle below 30 degrees. The energy-sorted jet information was combined with track-based triggers to successfully perform b-tagging with a track threshold of 1.5 GeV. The Jet Trigger was used to successfully decrease the electron triggering threshold from 6 GeV down to 2 GeV and to perform the world’s first measurement of the longitudinal structure function $F_L$ of the proton.

Parallel Session B4 - Interconnects / 60

The Origami Chip-on-Sensor Concept for Low-Mass Readout of Double-Sided Silicon Detectors

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Modern front-end amplifiers for silicon strip detectors offer fast shaping but consequently are susceptible to input capacitance which is the main contribution to the noise figure. Hence, the amplifier must be close to the sensor which is not an issue at LHC, but a major concern at material budget sensitive experiments such as Belle or the ILC detector. We present a design of a silicon detector module with double-sided readout where thinned front-end chips are aligned on one side of the sensor which allows efficient cooling using just a single, thin aluminum pipe. The connection to the other sensor side is established by thin kapton circuits wrapped around the edge - hence the nickname origami.

Summary:

The current Belle Silicon Vertex Detector (SVD) at the high-luminosity KEK-B accelerator pushes the limits in terms of occupancy. The sensors are read out with the low-noise, but slow-shaping (Tp≈800ns) VA1TA front-end chip, and due to the large background, track finding becomes increasingly difficult as the occupancy exceeds the 10% level in the innermost layer. At increasing trigger rate, another issue is dead time which occurs since the VA1TA has no pipeline and thus is blind during the readout which takes about 25µs.

Already for several years, there are plans to upgrade the Belle SVD and these have evolved from replacing the innermost layer only to an entirely new and significantly larger subdetector for the Super-Belle experiment. Coming from CMS, we proposed their front-end chip, the APV25, as it perfectly meets the
requirements of Belle: It has a shaping time of just 50ns and an analog pipeline of 192 cells in order to avoid any dead time.

However, this fast shaping inevitably comes along with higher noise figures for both the constant term and the capacitance slope. Hence, one has to take great care to minimize the load capacitance presented at the inputs of the front-end amplifiers. The Belle SVD has a limited angular coverage (17° to 150° azimuth) and currently is read out from the sides, which implies long flex fanouts. For the innermost layer, which is composed of only two sensors per ladder, this concept also works with the APV25. However, capacitance will not allow that scheme for outer layers. In comparison to the LHC, KEK-B is a low-energy machine (3.5GeV for positrons and 8GeV for electrons) and thus material budget is a critical issue for the vertex resolution, which is a key parameter at Belle. Consequently, one has to minimize material as far as possible, which will also be a critical point for the International Linear Collider (ILC).

This was the motivation to develop a chip-on-sensor concept for double-sided readout with lowest possible material budget, yet including cooling for the front-end chips, and minimum noise figure, which means smallest possible load capacitance. We achieve this goal by using a thin kapton "hybrid" placed on the sensor but separated by a Rohacell (styrofoam) layer thinning the APV25 chips to 100µm (or less) using a single thin aluminum pipe for water cooling connecting the sensor strips to the APV25 inputs by thin kapton circuits.

All APV25 chips are aligned on the hybrid such that they can be cooled by a single aluminum pipe. The central chips are connected to the strips on the same side using a kapton fanout, where the outer APVs are attached to flex circuits which will be wrapped around the sensor edges and connected to the strips on the other side.

We already successfully demonstrated the chip-on-sensor concept for one sensor side with a prototype module in 2006, achieving excellent signal-to-noise in beam tests. In summer 2008, we will build an origami module as described above and by the time of the TWEPP workshop, we will already have source measurement results. A beam test will follow later this year.

We prefer a poster presentation which will include not only photos, drawings and results of the origami module, but also a 3D mechanical model attached to the poster.

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Parallel Session B5 - Power

The Power System Detector Control System of the Monitored Drift Tubes of the ATLAS Experiment

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The Detector Control System (DCS) of the power supply of the Monitored Drift Tubes (MDT) detector of the ATLAS experiment at CERN will be presented. The principal task of DCS is to enable and ensure the coherent and safe operation of the detector. The interaction of detector experts, users or even shifters with the detector hardware is performed via DCS. This is the responsible system of monitoring the operational parameters and the overall state and status of the detector, the alarm generation and handling, the connection of hardware values to databases and the interaction with the Data Acquisition system. The MDT subdetector was treated as a Finite State Machine hierarchy while the operation is done on a top level human interface.

The Power System (PS) for the High & Low Voltage of the DCS in ATLAS is implemented using the SY1527 power system with the Easy crate configuration from CAEN. The readout was done via an OPC server.
The Radiation Tolerant Electronics for the LHC Cryogenic Controls: Basic Design and First Operational Experience

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Co-author(s): Gonzalo Fernandez Penacoba; Miguel Angel Rodriguez Ruiz

CERN

The LHC optics is based in the extensive use of superconducting magnets covering 23 km inside the tunnel. The associated cryogenic system for keeping the magnets in nominal conditions is hence distributed all around the 27 km LHC tunnel and the cryogenic instrumentation submitted to the LHC radiation environment is composed of close to 18,000 sensors and actuators.

Radiation Tolerant (RadTol) electronics was designed and procured in order to keep the signals integrity against electromagnetic interference and to reduce cabling costs required in case of sending the analog signals into the 30 radiation protected areas.

This paper presents the basic design, the qualification of the main RadTol components and the first operational results.

Parallel Session B5 - Power / 106

The SPI as an integrated power management device for serial powering

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For future hep experiments, especially for LHC upgrades new powering schemes are required. The SPI001 (Serial Powering Interface) chip has been designed and fabricated to explore the serial powering approach.

Main features of the chip are a programmable shunt regulator (handling at least 1A) and two linear regulators providing module voltages, current mode ADCs monitoring shunt and linear regulator current, overpower protection and AC coupled communication interfaces. Bump bonding techniques are used for chip on board assembly to enhance connectivity and thermal issues.

The concept and design details of the chip are presented and first results are shown.

Summary:

It is widely accepted that due to material budget and power dissipation issues LHC upgrade experiments cannot be operated in a standard parallel powered mode. More efficient powering schemes are needed and serial powering, where a current is used to power modules in series, is one very promising alternative proposal.

Various approaches are presently discussed where error amplifier and regulator transistor are implemented either internally (meaning as part of ROC), externally or by mixing both scenarios. First studies have already proven the basic principle and modules have been successfully operated serial powered using commercial components.

However, these setups cannot satisfy all needs and an increase urge for an integrated solution using radiation tolerance CMOS technology existed. The SPI chip, fabricated using TSMC 025MM process, addresses this need. It is versatile allowing exploration and evaluation of different SP schemes.

The chip offers a programmable shunt element to provide a module voltage between 1.5 to >2.5V out of the supply current. The shunt is designed to sustain currents of at least 1A at full voltage, higher currents have to be verified in field tests. Simulations show that a dynamic impedance of the shunt element in the order of 100mOhm can be achieved which would exceed the performance of discrete
setups by more than two orders of magnitude. A separate error amplifier on the chip can be used to operate a set of external shunt transistors (distributed shunt concept). These shunt transistors can preferably be integrated in the readout chips on the module (as planned for the ABCn). Compared to a conventional shunt-per-chip approach this concept reduces dispersive effects significantly.

In addition, two independent linear regulators offer separate supply voltages covering a range of ~1.2 to 2.5 V. An idle feature is implemented as a first step towards pulsed powered schemes as anticipated for the ILC machine.

Furthermore the SPI chip provides a bank of 7 AC-LVDS comports. AC coupling is needed as the DAQ system and the module are at different DC potential. 6 bit flash ADCs using current mirror techniques are implemented to probe the shunt and linear regulator currents. The LSB of the ADCs is adjustable so that the full dynamic range of the regulators or a smaller range with increased accuracy can be probed.

A programmable threshold can be set to trigger an over-current alarm which can be used to power the chip down. In this case the chip functionality is reduced to a mere switch in order to bypass the current to other modules in the power queue and maintain their operation. Such power down techniques are essential in worst case scenarios where major module components fail.

Each SPI chip can be addressed individually using a 5 bit chip ID and is using a common bus in a multi drop configuration. By doing this up to 30 chips can be controlled using only 3 control lines.

To minimize any connection impedance and to provide the most reliable connection solder bump bonding of the chip is anticipated and in-house assembly is investigated.

The design and the features of the SPI chip are presented in detail and first results are shown.

Parallel Session A6 - Trigger2 / 118

The Sector Collector of the CMS DT Trigger System: Installation and Performance

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Drift Tubes chambers are used for muon detection in the central region of the CMS experiment at LHC. Custom electronics is used for reconstructing muon track segments and for triggering the CMS readout. The trigger Sector Collector modules collect muon segments identified by the on-chamber devices, synchronize the data received from different chambers and convert from LVDS to Optical for transmission to the off-detector electronics. Installation and integration tests were developed for tuning both firmware and hardware of the Sector Collector system: results will be reviewed. The system performance during CMS data taking with cosmic rays and LHC beam (if available) will be discussed.

Summary:

The CMS experiment at LHC is equipped in the central region with Drift Tubes chambers, providing muon detection. The DT chambers are also used by the CMS trigger system in order to reconstruct track segments and measure transverse muon momentum. Electronics for local trigger data generation is installed on the chambers, while track finding algorithms are implemented on off-detector devices. The trigger Sector Collector (SC), installed in racks placed on the towers surrounding the experiment, acts as link between on-detector processors and the off-detector ones. The SC collects reconstructed segments from the DT chambers of a 30 degrees azimuthal sector of the detector, performing reduction and synchronization of the data. The trigger segments are transmitted to the track finding devices through optical fibers.

The SC modules consist of several units: a VME 9U motherboard, hosting a board controller; four mezzanine cards, receiving data from the four chambers in a sector via 8-to-1 LVDS links on copper cables; a fifth mezzanine card, hosting serializers (GOL chips at 1.6 Gbit/s) and optical drivers; an optical receiver card, placed in the counting room, whose main task is to deserialize high-speed transmitted data and inject them in the track finding devices. Spy features on the SC modules allow trigger data flow to
be monitored by injecting part of them into the DAQ stream, so providing us a useful tool for system monitoring and diagnostic.

Several custom processing units have been implemented on FPGA devices using VHDL programming. Flash-based FPGAs have been used for the electronics installed in the tower rack, where the environment is expected to be highly radioactive during LHC operation.

All electronics has been tested before installation, with a custom test jig, mimicking the whole data transmission path, from on-chamber devices to counting room modules. Then, after installation and integration in the CMS trigger and data acquisition systems, the SC became part of the CMS trigger facility for providing cosmic muon triggers for the commissioning of the CMS sub-detectors.

A technical trigger based on coincidences on muon detected on each DT chamber has been developed. It provides triggers on cosmic muons used for electronics synchronization (adjust timing of data coming from different sectors) as well as for data taking of CMS sub-detectors during the beam stop periods.

The technical trigger provides us a flexible tool to be used still for synchronization studies with the very first LHC beam when, for instance, a trigger rate of about 500 Hz is expected for luminosity of $10^{31}$ cm$^{-2}$ s$^{-1}$.

In parallel, complete and reliable control software was developed, taking advantages from the facilities already implemented in the overall CMS-trigger framework. It is designed for handling a multi-crate environment with fully parallel access and maximal flexibility. Databases are used for retrieving both software and board configurations as well as for recording on-line monitoring information.

Long periods of data-taking led us to design powerful and easy-to-use diagnostic tools such as summaries of the hardware status and plots showing the trend of the temperatures, as monitored by sensors hosted in the electronic modules.

**POSTERS SESSION / 42**

**The TOTEM Roman Pot Motherboard**

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The TOTEM Roman Pot Motherboard (RPMB) is the main component of the Roman Pot front-end electronic system. It is mounted on the Roman Pot between detector hybrids and patch panel. The RPMB main objectives are to acquire on-detector data and trigger information from up to 10 hybrids, to perform data conversion from electrical to optical format and to transfer it to the next level of the system. It also distributes the control information to the hybrids and collects different types of information like temperature, pressure and radiation inside the pot. The TOTEM Roman Pot Motherboard, its components and connectivity are presented in this paper.

**Summary:**

The TOTEM experiment has three sub-detectors: Roman Pots (RP) with silicon strips, T1 detector with Cathode Strip Chambers (CSC) and T2 with Gas Electron Multiplier detectors (GEM). All detectors use the VFAT chip for tracking and trigger generation mounted on different hybrids. A Roman Pot hybrid contains four VFAT chips. The set of ten hybrids is build for every Roman Pot. The RPMB is connecting to this set via flex connections and glued to the flange. The presentation will give a detailed overview of the design and functionality of the RPMB components as a part of the front-end electronics in Roman Pot for TOTEM experiment.

**Parallel Session B6 - Programmable Logic, boards, crates and systems / 123**

**The TOTEM T1 detector electronic system**

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**Co-author(s):** Antonio Magri$^2$; Enrico Robutti$^1$; Fabrizio Ferro$^1$; Filippo Capurro$^2$; Maurizio Lo Vetere$^2$; Paolo Musico$^1$; Stefano Cerchi$^1$

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Totem is an experiment located at CERN and devoted to the measurement of the proton-proton elastic and total cross section at LHC. TOTEM and CMS foresee a program of common measurements on diffractive physics.

This presentation will be focused on the design of T1 detector, devoted to the measurement of the inelastic rate, made of Cathod Strip Chambers.

We will present the complete electronic readout chain of the Cathode Strip Chambers: the anode and cathode front-end boards, the readout-control card and the trigger unit. Key features of this system are high radiation tolerance and data path, slow control, fast command and trigger compliant with the CMS standards.

Summary:

The TOTEM T1 detector is a dual arm telescope, made by Cathode Strip Chambers (CSC), located in the very forward regions of the CMS detector at LHC. Each telescope arm is composed by 5 CSC planes spaced 0.5 meters apart. Each CSC is read-out by one plane of wires (anodes) and by two planes of strips (cathodes), thus giving three coordinates for each particle interacting with the detector.

Detailed studies have been carried out in order to characterize the signals coming out from the CSC and to choose the most suitable electronics for reading them out. In total about 11000 anodes and 16000 cathodes signals will be handled.

After a brief introduction to the design of the detector, an overview of the entire DAQ chain will be given and a more detailed description of the anode front-end card (AFEC), cathode front-end card (CFEC) and the read-out card (ROC) circuits will then follow.

The electronic system has been developed keeping into account the hostile environment from the point of views of both radiation and magnetic field. Dedicated VLSI circuits have been extensively used in order to optimize space and power consumption.

A key component of this system is the ROC. It receives the slow control and configuration data from the standard CMS slow control system, collects data and trigger information provided by VLSI custom chips and forward them to the counting room using optical links.

A dedicated T1 trigger card in the counting room will allow the generation of T1 trigger primitives to be sent to the global trigger logic, permitting both individual TOTEM and TOTEM/CMS integrated runs.

Extensive tests have been carried out on the complete system to characterize both the chambers and the electronics.

POSTERS SESSION / 130

The VFAT production test for the TOTEM experiment.

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Co-author(s): James Rouet; Jan Kaspar; Josef Kopal; Juha Petäjäjärvi; Paschalis Vichoudis; Valentina Avati; Walter Snoeys; Wojciech Bialas

VFAT is the front-end ASIC designed for the charge readout of silicon and gas detectors within the TOTEM experiment of the LHC.

A stand alone portable Totem Test Platform (TTP) with USB interface has been developed for the systematic testing of the TOTEM hybrids equipped with VFAT chips. This paper is divided into 3 sections; the first describes the hardware features of the TTP, the second describes the software routines for the control and systematic testing of VFATs, the third presents the production test results including yield.
The commissioning status and results of ATLAS Level1 Endcap Muon Trigger System

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The ATLAS Level1 endcap muon trigger selects interesting events containing muons with Pt greater than 6GeV/c from 40MHz proton-proton collisions. This system consists of 3,600 Thin Gap Chambers (TGCs) and the total number of readout channels is 320,000. This trigger logic is based on the coincidence between 7 layers of TGCs. All processes are performed on fast electronics within 2.5 micro seconds. To be ready for the first beam scheduled in 2008, we have succeeded in sending trigger signal of cosmic-ray muons with the synchronous operation at 40MHz and a fine signal timing adjustment. We will report on status of the commissioning and results from combined runs with other ATLAS detectors.

Summary:
The ATLAS Level1 trigger system selects interesting events from the large amount of events produced with proton-proton collision. This system works as a pipeline trigger system with the 40MHz operation clock which is synchronous to the LHC proton-proton collision. The processing latency is required to be less than 2.5 micro seconds. The reduction power is 100kHz from 40MHz.

The Level1 endcap muon system selects the interesting events which contains muons with Pt greater than 6 GeV/C. Every trigger module has delaying functionalities in each input port for timing adjustment, especially between layers.

By the end of April 2008, the TGCs and almost all infrastructures have been installed in ATLAS cavern, including the 100m long cable connections. All trigger modules are operated in the synchronous operation to 40MHz, which is send to all the system as global operation clock.

For the first beam commissioning runs scheduled in 2008, various hardware bugs have been found, and fixed. In combined runs with other ATLAS detectors, the scheme for the TGCs and Level1 endcap muon trigger system has been established with final infrastructures.

The electronics of ALICE Dimuon tracking chambers

Valerie Chambert

1 IPN Orsay

The Alice Muon Spectrometer tracking system is composed of five stations (ST) with two wires chambers each. IPN Orsay is responsible for the electronics design and production for the tracking (1.1M channels), for the readout electronics software and for the ST1 design and building. We will describe the readout architecture based on dedicated Front-End boards, embedded digital crates, and a Trigger crate. We will explain the process to reach the final electronic design. We will describe the electronics production, specially the tests for the 20000 Front-End boards. We will focus on ST1 integration at CERN, EMC issues and commissioning.

Summary:
At CERN LHC energies, the formation of a quark-gluon plasma (QGP) is expected. One of the main signature of this formation is the quarkonia suppression. The ALICE muon spectrometer is designed to study this QGP observable. The Muon Spectrometer tracking system is composed of five stations with two wires chambers each. IPN Orsay is responsible for the electronics design and production for the tracking (1.1M channels), for the readout electronics software and for the ST1 design and building.

The chambers pads signals are processed by a MANAS (Multiplexed ANAlog Signal) ASIC embedded on MANU (MAnas NUmérique) boards which insure the digital conversion and the data transmission through a MARC (Muon Arm Readout Chip) ASIC. Sets of MANU boards are connected together on a
data Patch Bus (Protocol for Alice Tracking Chamber) line managed with a token. Data go to a digital CROCS (Concentrator Read-Out Cluster Unit System) crate insures the data tagging and their concentration. It can send calibrating signals to the front-end electronics with a dedicated board. All the Spectrometer CROCS receive the trigger signals through a dispatcher Trigger Crate.

During the electronics design, we performed electronics radiation hardness tests. The ST1 first tests allowed us to tune the impedance matching of each Patch Bus what is a key point, because most of the MANU boards on the line are not impedance matched. We tuned the current in some Bus patch to be able to read them in a safe way. The detector readout sequence was tested and required many FPGA additional programs. We implemented a Jtag chain on the CROCS boards so that all the CROCS FPGA programs can be modified and reloaded from Alice control room.

About 20000 MANU boards were produced, numbered with a barcode and tested in industry. A dedicated test bench was developed and transferred to industry with a go no go function and a diagnostic option for repairing. It produces a test sequence for the power supplies and for the transmission protocols. It also tests the MANAS circuit: pedestals, gains, calibration internal capacitor value. A data file for each MANU board was delivered to the collaboration. We designed, produced and tested 600 link boards, 22 full CROCS crates (375 boards, 4 types) and 2 TCI crates.

Each MANU board location on the chambers was numbered with a barcode, so we built a full ST1 map. The 9 ST1 chambers were fully tested with a cosmic rays test bench. We had to fulfill CERN safety requirements like using Halogen Free and amagnetic materials. After its building at Orsay, each quadrant was carried to CERN, tested in a surface building before being commissionned in the Alice cavern. We choose to be very careful with EMC questions. We designed special mechanical parts for grounding. We also designed and installed power supplies high frequency filtering boxes. ST1 and ST2 successfully participate to the first Alice Commissioning runs in December 2007.

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**Transmission-Line Readout with Good Time and Space Resolutions for a Planicon MCP-PMT**

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Time-of-flight techniques with resolution of a one to several picoseconds would allow the measurement of 4-vectors of relativistic particles at high energy colliders, the association of photons with collision vertices, and the construction of spectrometers with which to study muon cooling without magnetic spectrometers.

In order to take advantage of photo-detectors with intrinsic single photo-electron resolutions of tens of picoseconds to build large-area time-of-flight systems, one has to solve the problem of collecting signal over distances large compared to the time resolution while preserving the fast time resolution inherent in the small feature size of the detectors themselves. The solution also has to have a manageable number of electronics channels and low total power. We present here the design of a transmission-line readout for a Photonis Planicon micro-channel plate photomultiplier tube (MCP-PMT) that has these characteristics. The MCP-PMT is characterized by single pulse rise times in the order of 200 ps and transit time spreads (TTS) in the order of 30 ps, and an anode 32 by 32 array of pads (1024 total). The readout is implemented on a Rogers 4350B printed circuit board with 32 parallel 50-ohm transmission lines on 1.6 mm centers, each traversing one row of pads. The board is soldered to the 32 by 32 array; each transmission line being read out on each end.

We have simulated the electrical properties of the transmission-line readout board with Hyperlynx and Spice simulators. The simulations predict that the readout transmission-lines can achieve a
signal bandwidth of 3.5GHz, which should not significantly degrade the time and spatial resolutions intrinsic to the MCP-PMT signals.

Results from the simulation and tests will be presented.

Summary:
The ultimate goal in the front-end electronics is to develop a custom ASIC that incorporates fast sampling of the MCP pulses. This design is in progress. As an intermediate step, we will test the transmission-line architecture using a 40-GS/sec digital oscilloscope as well as Ortec constant-fraction discriminators and time-to-digital converters having 3.1 pSec resolution. The system will first be tested using the Argonne laser test stand. A first test of the assembled system with relativistic particles is scheduled in the Fermilab Mtest test beam for June 2008. Results from the simulation and tests will be presented.

TOPICAL 1 - LHC Upgrades / 25

Upgrade of the ATLAS Monitored Drift Tube Detector for the SLHC

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The upgrade of the LHC towards higher luminosity needs to be matched by an upgrade of the detector performance. In the case of the ATLAS Monitored Drift Tube (MDT) detectors, higher luminosity will result in increased neutron and gamma background rates leading to a reduction of spatial resolution and tracking efficiency as well as to an increase of the required readout bandwidth. In the regions of highest background rates (forward region) a modified detector and readout concept will probably be necessary to maintain tracking efficiency and to limit the data volume due to background hits. We will present an overview of the upgrade options for the MDT chambers and their readout electronics.

Summary:
The muon spectrometer forms the outer shell of the ATLAS experiment and is designed to measure the momentum of muon tracks with high accuracy. It is instrumented with precision tracking chambers, the monitored drift tube chambers (MDT), which consist of layers of drift tubes with tube diameters of 30 mm, using Ar/CO2 (93/7) at 3 bar as drift gas.

A serious problem for MDT chamber operation, already at nominal LHC luminosity, is the presence of high neutron and gamma radiation levels in the experimental hall creating Compton electrons in the tube walls and extra ionization in the tubes. This background hit rate largely exceeds the one expected from muon tracks. In the forward region of the detector (eta > 1.5) the hit rates due to neutron background go up to 300 kHz/tube, while rates in the barrel region (eta < 1) are an order of magnitude lower. High hit rates in the tubes lead to accumulation of space charge in the gas volume degrading position resolution. They also mask hits from subsequent muon tracks, reducing detection efficiency and, finally, pose problems to the readout bandwidth which is designed for up to about 400 kHz per tube. Beyond this value a certain fraction of hits will have to be suppressed to limit readout latency.

These problems will aggravate with an upgrade of the LHC luminosity beyond the nominal value of 1034 cm-2 s-1, and a replacement of the present readout electronics will have to be envisaged. For a redesign of the electronics the main technical issues are: (a) efficiency, signal processing and dead time at the frontend, (b) storage capacity and data transmission speed between TDC and on-chamber processor, (c) bandwidth for data transmission speed to the readout drivers (ROD’s) and (d) radiation tolerance of the on-chamber components.

In the forward region (eta > 1.5), where about 15% of the MDT are located, the replacement of the present readout electronics will have to be envisaged. For a redesign of the electronics the main technical issues are: (a) efficiency, signal processing and dead time at the frontend, (b) storage capacity and data transmission speed between TDC and on-chamber processor, (c) bandwidth for data transmission speed to the readout drivers (ROD’s) and (d) radiation tolerance of the on-chamber components.

In the forward region (eta > 1.5), where about 15% of the MDT are located, the replacement of the electronics may not be sufficient, and a detector type with higher rate capabilities will have to be selected to limit the degradation of resolution and efficiency. A feasible option for this upgrade would be MDT chambers with smaller tube diameter. The hit rate recorded by a 15 mm diameter drift tube is only about one tenth of the presently used 30 mm tube due to the combination of reduced...
tube size and higher drift velocity in the Ar/CO2 gas. The smaller size will also allow to increase the number of tube layers per detector volume, increasing the number of coordinate measurements along the track. We will present first test results of this tube type and discuss some aspects of MDT chamber construction from small tubes.

Depending on the neutron rates actually observed at LHC (present predictions are uncertain by a factor of 5) and on the definitive radiation shielding for the SLHC, a smaller or larger fraction of the MDT chambers will have to be replaced by chambers of the new design. Assuming a fraction of 15 – 20 %, construction of about 150 – 200 chambers would have to be foreseen. We will present a preliminary estimate for the resources needed for an upgrade program of the MDT.