

# Design Considerations for High Step-Down Ratio Buck Converters

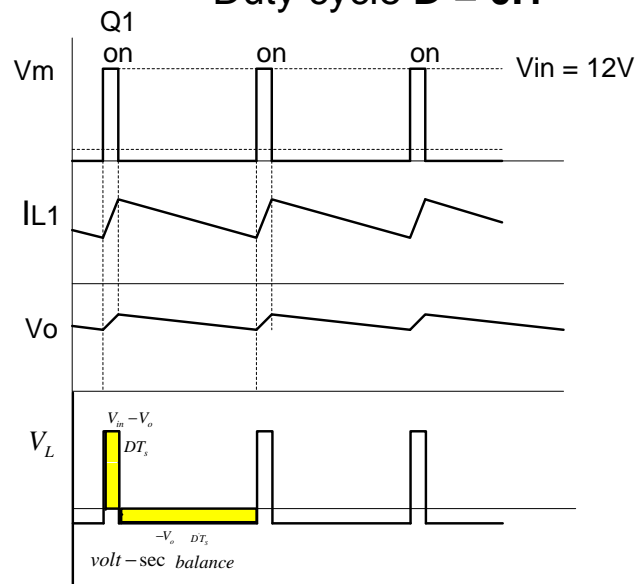
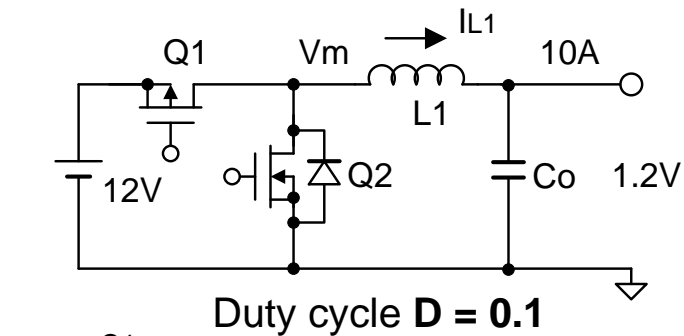
Ramesh Khanna – National Semiconductor, Richardson, TX

&

Satish Dhawan – Yale University, CT, USA



# Buck converter



In Non-Synchronous buck converter  
Q2 is replaced with diode

Q1 on & Q2 off

Q1 off & Q2 on

$$V_L = V_{in} - V_{out}$$

$$D = \frac{T_{on}}{T_s}$$

$$V_L = -V_{out}$$

$$D' = (1 - D) = (1 - \frac{T_{on}}{T_s})$$

$$(V_{in} - V_{out})T_{on} = (V_{out}T_{off})$$

$$(V_{in} - V_{out})DT_s = V_{out}(1 - D)T_s$$

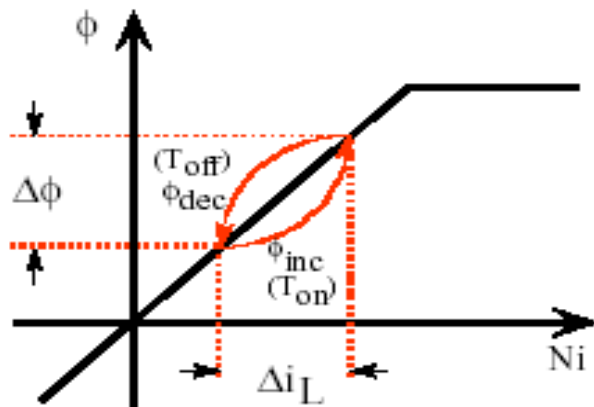
$$\frac{V_{out}}{V_{in}} = D$$

DC gain

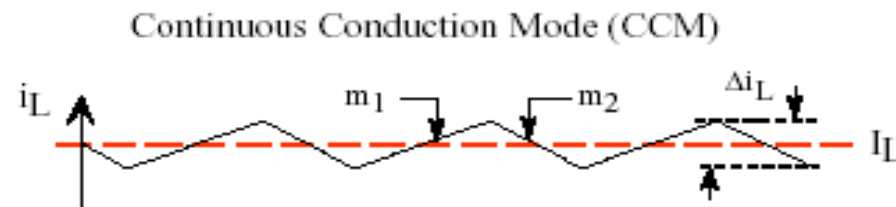
# Continuous vs Discontinuous mode of Operation

When Q1 is turned on Input source charges the inductor and supplies the Output load

When Q1 turns-off Voltage across the inductor changes polarity and forward biases the sync diode, Q2 is allowed to turn-on. Energy stored in the inductor is supplies to the load.

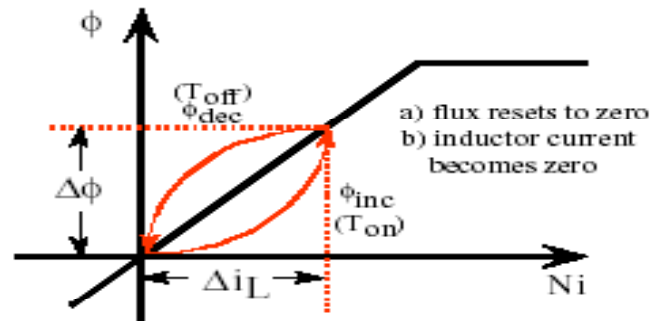


Flux characteristics for CCM operation

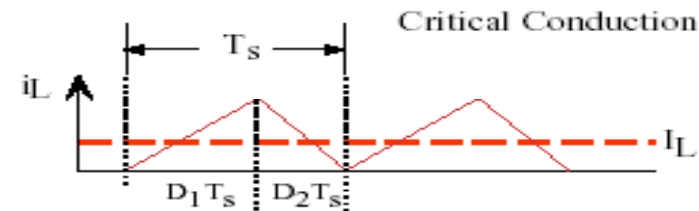


For CCM, the inductor current never goes to zero. There is always energy stored during the when switch is on or off.

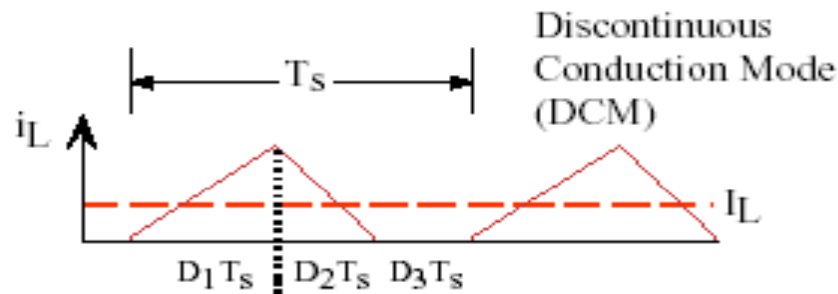
# Buck converter in Discontinuous mode



Flux characteristics for Critical and DCM mode of operation



During the critical conduction mode, the inductor current reaches zero just before the switch turns on again. The inductor never stays in discharged state, but charges up again instantaneously.



In the discontinuous mode, the inductor has discharged to zero and remains in that state for finite time before it gets charged again. In this case, the current through the inductor is never continuous.

# Specifications / Design considerations

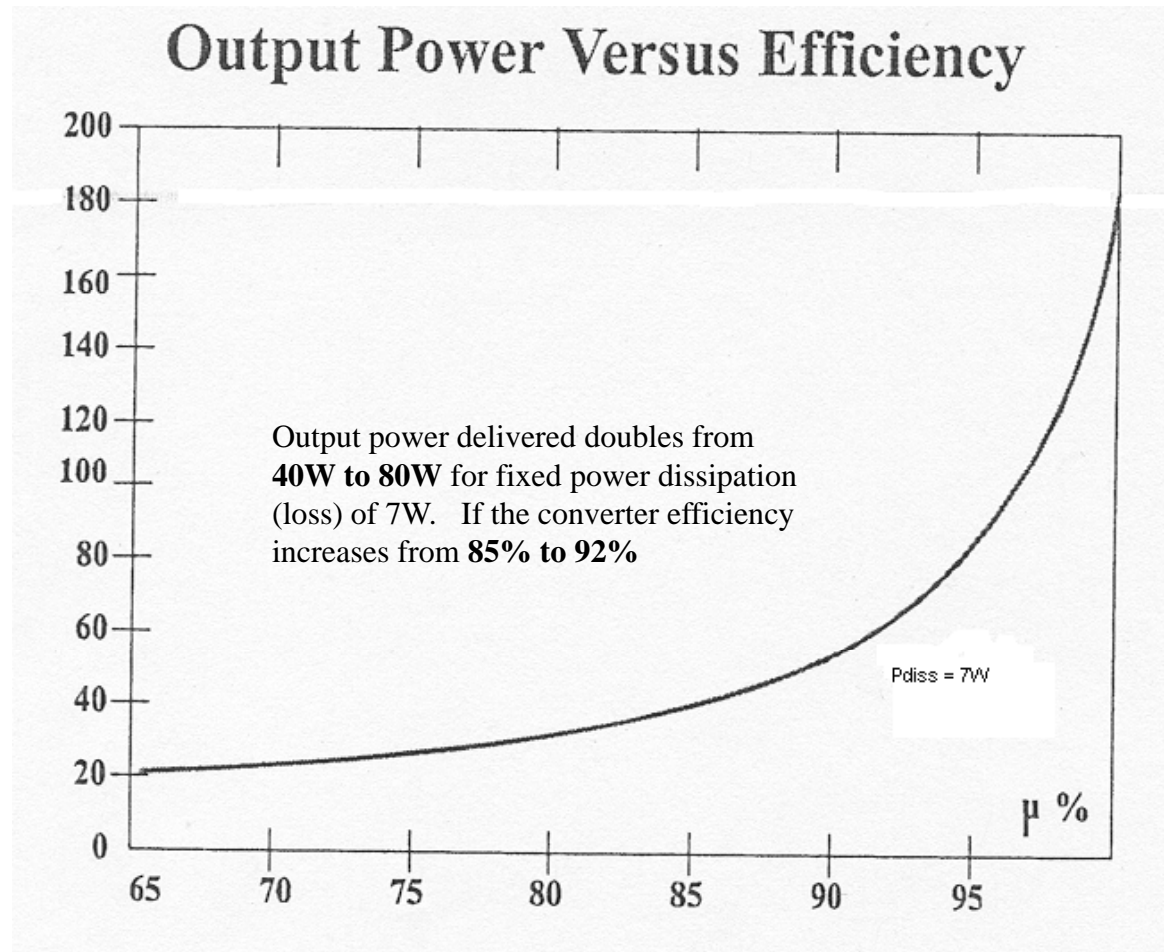
	Min	Max	Tolerance	Req'd
Vin	3.3	15		
Vout	1.8		+/-3%	
Output Ripple		50mV		
Efficiency	85%			
Transient		100A/usec		
Ambient Temp		55C		
Size		H x L x W		
Enable				x
Tracking				x
OV Protection				x
Current Limit				x
Cost Target				



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# Need for Efficiency Improvement



Efficiency Improvement is critical for any designs.

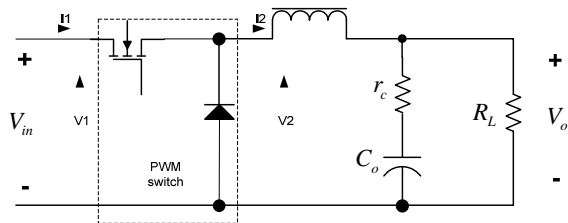
In order to maintain same heat dissipation improving efficiency from

85% to 91.9% doubles the output power.

- Less issues with regards to thermal management
- Improved reliability.

# Small Signal Model of Buck Converter

## • PWM Switch

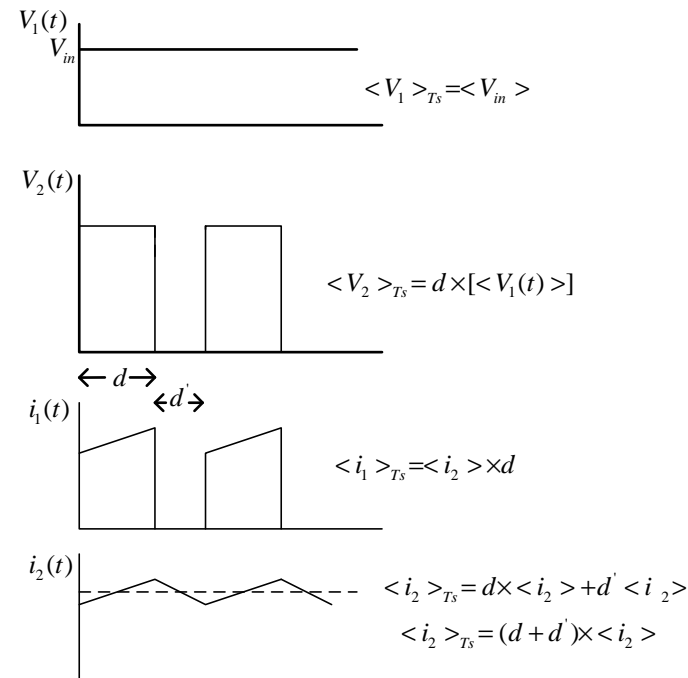


$V_2 \rightarrow$  **dependent variable**

$I_1 \rightarrow$  **dependent variable**

$V_1 \rightarrow$  **independent variable**

$I_2 \rightarrow$  **independent variable**



Express dependent sources  $\langle V_2(t) \rangle$  and  $\langle I_1(t) \rangle$  as a function of independent sources  $\langle V_1(t) \rangle$ ,  $\langle I_2(t) \rangle$  and  $d$  duty cycle

# PWM switch model

- Next step we perturb and linearize the equations, where we assume average voltage consists of constant “dc” component and small signal “ac” variation around the dc component.

$$\langle v_1(t) \rangle_{Ts} = V_1 + \hat{v}_1(t)$$

$$\langle i_1(t) \rangle = I_1 + \hat{i}_1(t) \quad d(t) = D + \hat{d}(t)$$

$$\langle v_2(t) \rangle_{Ts} = V_2 + \hat{v}_2(t) \quad d' = D' - \hat{d}(t)$$

$$\langle i_2(t) \rangle = I_2 + \hat{i}_2(t)$$

$$\langle v_2(t) \rangle_{Ts} = \langle v_1(t) \rangle_{Ts} \times d(t)$$

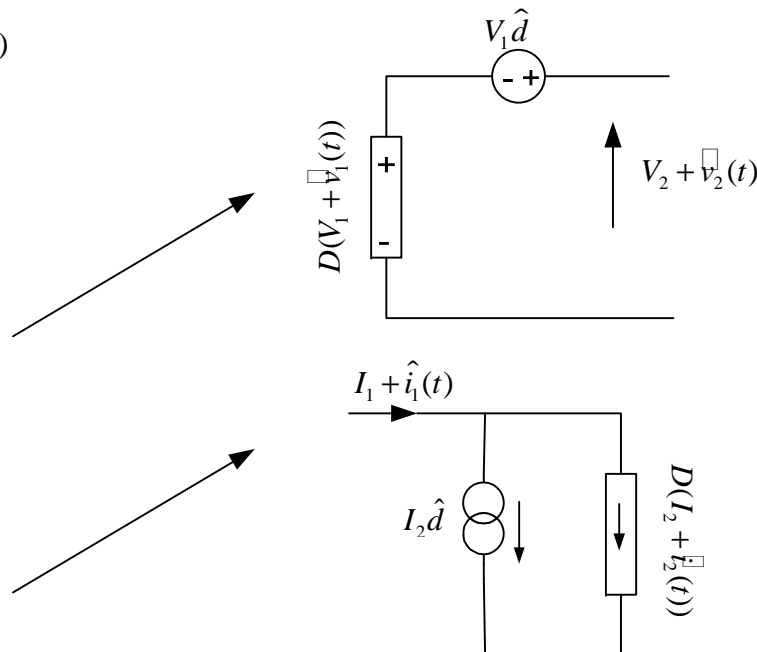
$$V_2 + \hat{v}_2(t) = (D + \hat{d}(t)) \times (V_1 + \hat{v}_1(t))$$

$$V_2 + \hat{v}_2(t) = D(V_1 + \hat{v}_1(t)) + \hat{d}(t) \times V_1$$

$$\langle i_1(t) \rangle_{Ts} = d \times \langle i_2(t) \rangle$$

$$I_1 + \hat{i}_1(t) = (I_2 + \hat{i}_2(t)) \times (D + \hat{d}(t))$$

$$I_1 + \hat{i}_1(t) = D \times (I_2 + \hat{i}_2(t)) + I_2 \times \hat{d}$$



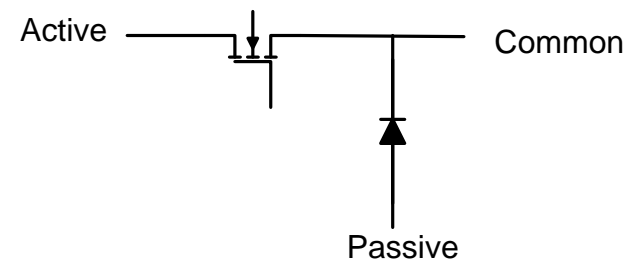
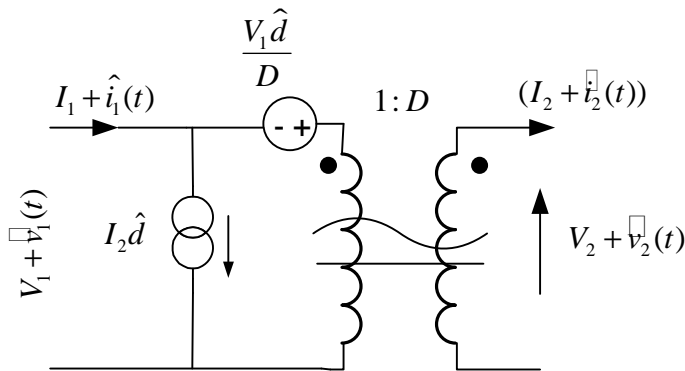
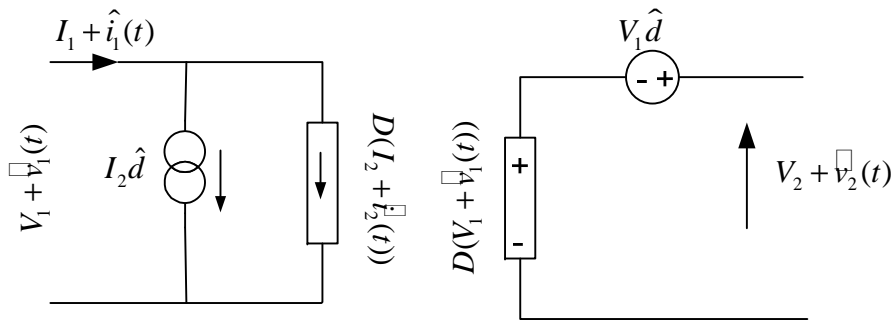


# PWM switch model

- Combining the two sections, we have the small signal mode of PWM switch

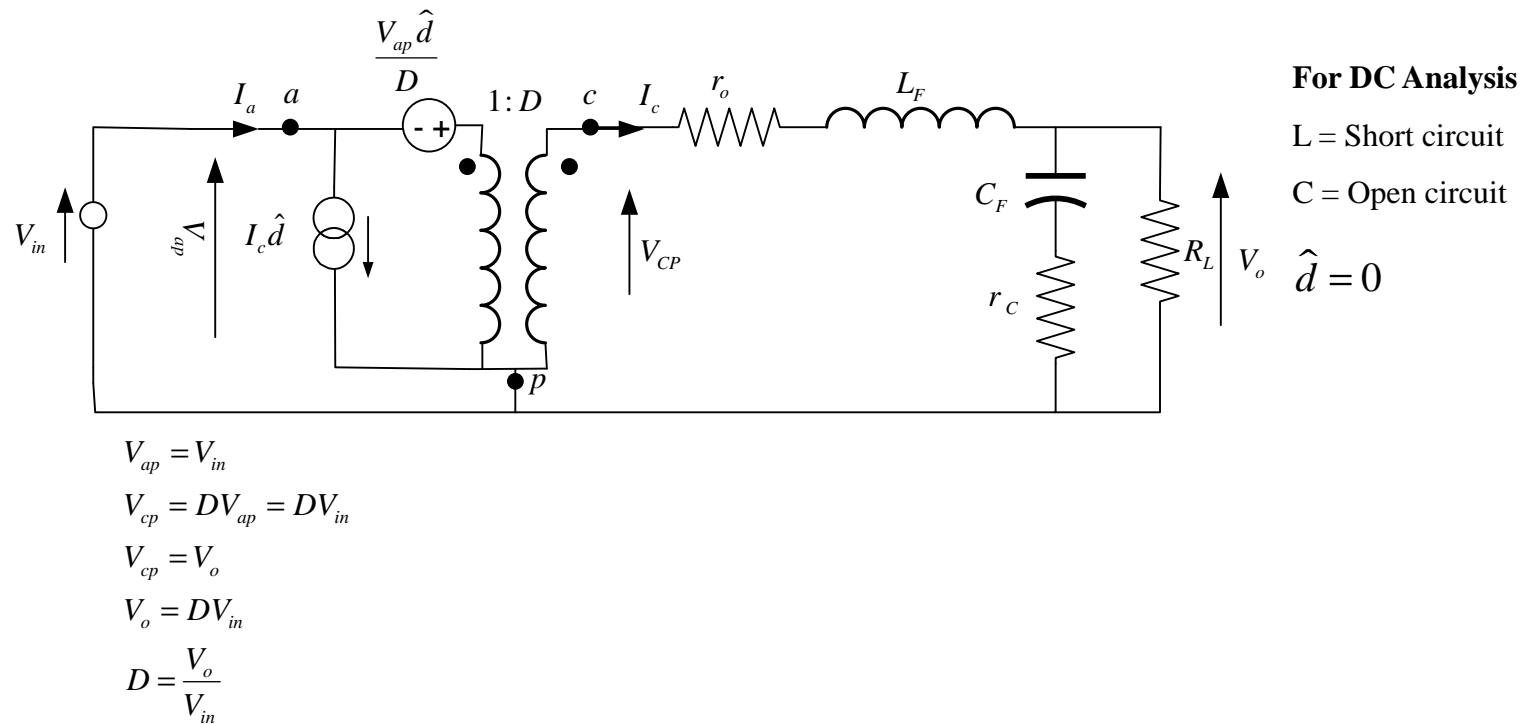
$$I_1 + \hat{i}_1(t) = D \times (I_2 + \hat{i}_2(t)) + I_2 \times \hat{d}$$

$$V_2 + \hat{v}_2(t) = D(V_1 + \hat{v}_1(t)) + \hat{d}(t) \times V_1$$



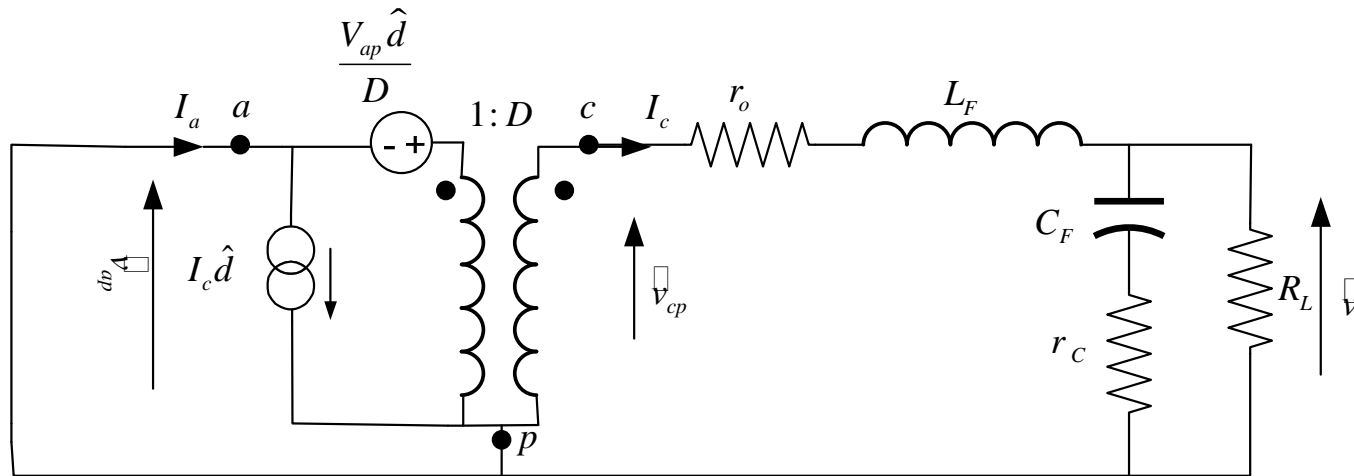
# Incorporating PWM switch in Buck Circuit

- **Small signal model of Buck converter - DC Analysis**



# Incorporating PWM switch in Buck Circuit

- Small signal model of Buck converter – AC Analysis
- For AC analysis we short the input source



$$Z_x = \frac{R_L(sC_o r_C + 1)}{(1 + sC_o(r_C + R_L))}$$

$$Z_L = r_o + sL$$

$$\frac{\hat{v}_o}{\hat{v}_{cp}} = \frac{Z_x(s)}{Z_x(s) + Z_L(s)}$$

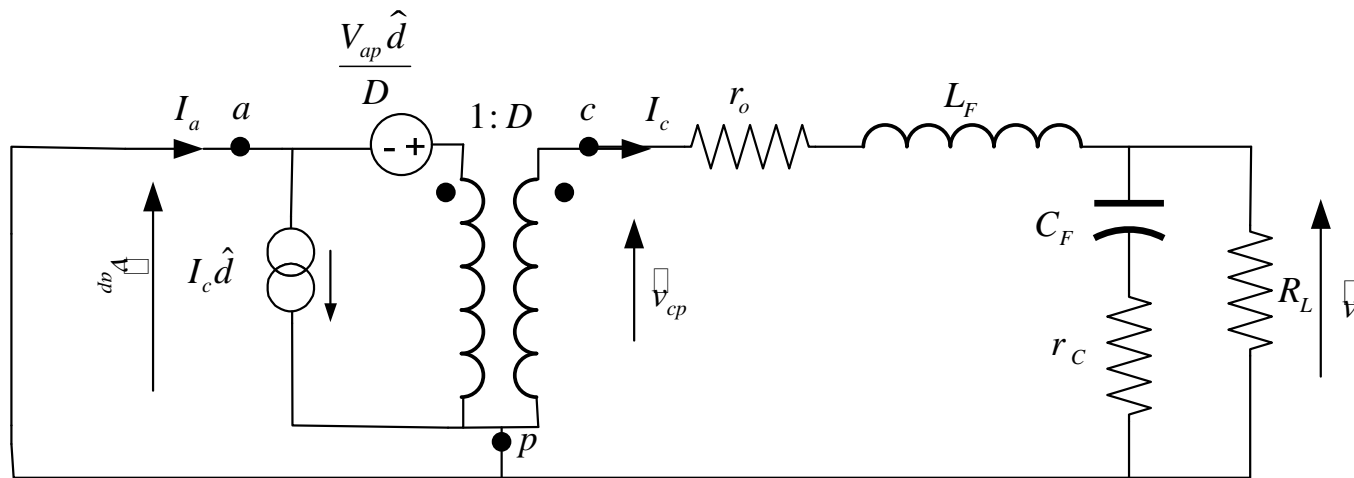
$$\frac{\hat{v}_{cp}}{\hat{d}}(s) = V_{in}$$

$$\frac{\hat{v}_o}{\hat{d}}(s) = \frac{\hat{v}_{cp}}{\hat{d}}(s) \times \frac{\hat{v}_o}{\hat{v}_{cp}}(s)$$

Control to output is the most important transfer function as it is necessary for the design of stable feedback loop.

# Incorporating PWM switch in Buck Circuit

- Small signal model of Buck converter – AC Analysis Alternate Approach
- For AC analysis we short the input source



Write differential equation for Voltage across inductor  $L_F$

Write differential equation for Current thru the output capacitor  $C_F$

$$L \frac{di_L}{dt} = i_L (-r_o - Den) - Den \frac{V_c}{r_C} + V_{ap} \hat{d}$$

$$C \frac{dv}{dt} = i_L \left( \frac{Den}{r_C} \right) + v_c \left( \frac{1}{r_C^2 Den} - \frac{1}{r_C} \right)$$

$$Den = \frac{R_L}{(1 + \frac{R_L}{r_C})}$$

# Incorporating PWM switch in Buck Circuit

- Write the two equations in matrix form
- Solve matrix using cramers rule to obtain control to output transfer function.

$$\begin{pmatrix} \frac{di_L}{dt} \\ \frac{dv}{dt} \end{pmatrix} = \begin{pmatrix} \frac{-r_o - Den}{L_F} & \frac{-Den}{r_C L_F} \\ \frac{Den}{C_F R_L} & \frac{1}{C_F} \left( \frac{1}{r_C^2 Den} - \frac{1}{r_C} \right) \end{pmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{pmatrix} \frac{V_{ap}}{L_F} \\ 0 \end{pmatrix} \hat{d}$$

$$Den = \frac{R_L}{(1 + \frac{R_L}{r_C})}$$

$$sX(s) = AX(s) + Bd(s)$$

$$sIX(s) = AX(s) + Bd(s)$$

$$(sI - A)x(s) = Bd(s)$$

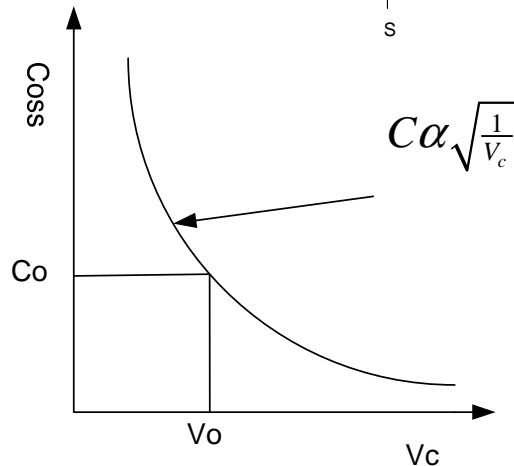
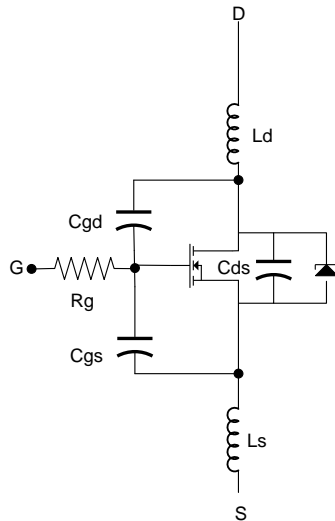
$$(sI - A) \frac{x(s)}{d(s)} = B$$

$$\begin{pmatrix} s + \left( \frac{-r_o - Den}{L_F} \right) & \frac{Den}{r_C L_F} \\ -\frac{Den}{C_F r_C} & s - \left[ \frac{1}{r_C^2 Den} + \frac{1}{r_C} \right] \end{pmatrix} \begin{bmatrix} \frac{i_L(s)}{d(s)} \\ \frac{v_o(s)}{d(s)} \end{bmatrix} = \begin{pmatrix} \frac{V_{in}}{L_F} \\ 0 \end{pmatrix}$$

$$\frac{v_o(s)}{d(s)} = \frac{\Delta \left( \frac{v_o}{\hat{d}} \right)}{\Delta}$$

# MOSFET Selecton

- MOSFET – switching model**



Model highlights the MOSFET critical parameters

$$C_{GD} = C_{RSS} \quad \text{Miller Capacitor}$$

$$C_{GS} = C_{ISS} - C_{RSS}$$

$$C_{DS} = C_{OSS} - C_{RSS}$$

Junction capacitors of semiconductor devices are non-linear

$$C = f(V_c) = C_o \sqrt{\frac{V_0}{V_c}}$$

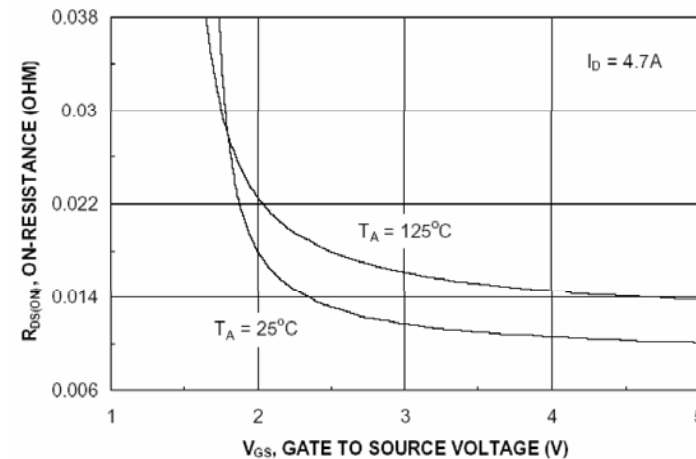
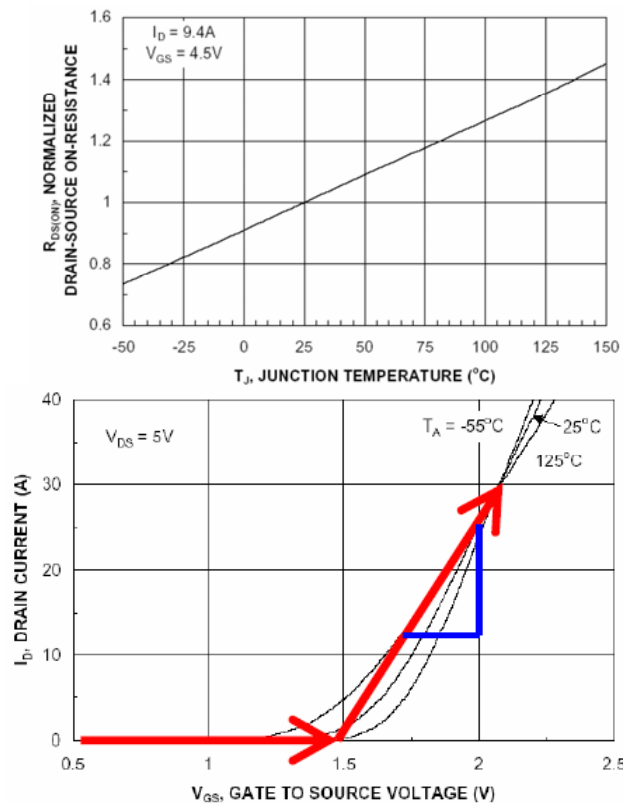
At  $V_c$  there is twice the charge that a linear capacitor of value  $C_o$  would have at  $V_0$

$$C_{gd}(V_{in}) = 2C_{rss\_spec} \sqrt{\frac{V_{ds\_spec}}{V_{in}}}$$

$$C_{oss}(V_{in}) = 2C_{oss\_spec} \sqrt{\frac{V_{ds\_spec}}{V_{in}}}$$

# Critical MOSFET parameters

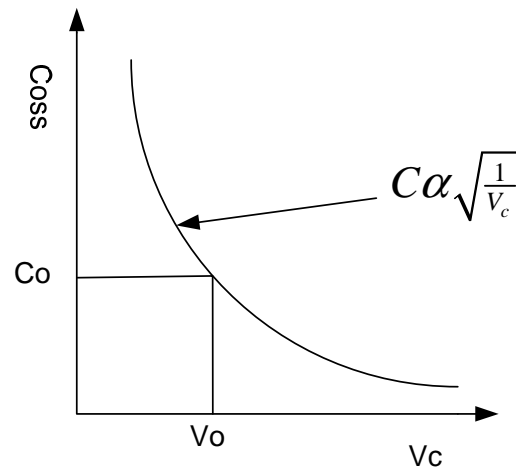
- $R_g$  – MOSFET gate resistor along with gate driver resistance are extremely critical for high speed applications.
- MOSFET gate resistance is temperature dependent thus increases with temperature - vendors provide curves  $R_{ds(on)}$  vs temperature for better approximation.



$$g_{fs} = \frac{dI_D}{dV_{GS}}$$

Forward Transconductance and has units of (mho) Siemens

# Non-Linear junction capacitor in MOSFET



$$C_{GD} = C_{RSS} \quad \text{Miller Capacitor}$$

$$C_{GS} = C_{ISS} - C_{RSS}$$

$$C_{DS} = C_{OSS} - C_{RSS}$$

Junction capacitors of semiconductor devices are non-linear

$$C = f(V_c) = C_o \sqrt{\frac{V_o}{V_c}}$$

At  $V_c$  there is twice the charge that a linear capacitor of value  $C_o$  would have at  $V_o$

$$Q = \int_0^{V_c} C_o \sqrt{\frac{V_o}{V_c}} dV_c$$

$$Q = C_o \sqrt{V_o} \int_0^{V_c} \frac{1}{\sqrt{V_c}} dV_c$$

$$Q = C_o \sqrt{V_o} [2\sqrt{V_c} - 2\sqrt{0}]$$

$$Q = 2C_o \sqrt{V_o} \sqrt{V_c}$$

$$V_c = V_o$$

$$Q = 2C_o V_o$$

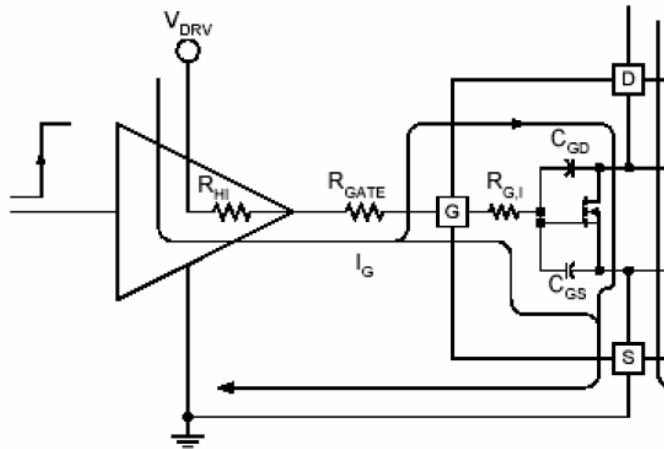
$$C_{gd}(V_{in}) = 2C_{rss\_spec} \sqrt{\frac{V_{ds\_spec}}{V_{in}}}$$

$$C_{oss}(V_{in}) = 2C_{oss\_spec} \sqrt{\frac{V_{ds\_spec}}{V_{in}}}$$

$$C = \frac{dQ}{dV_c}$$



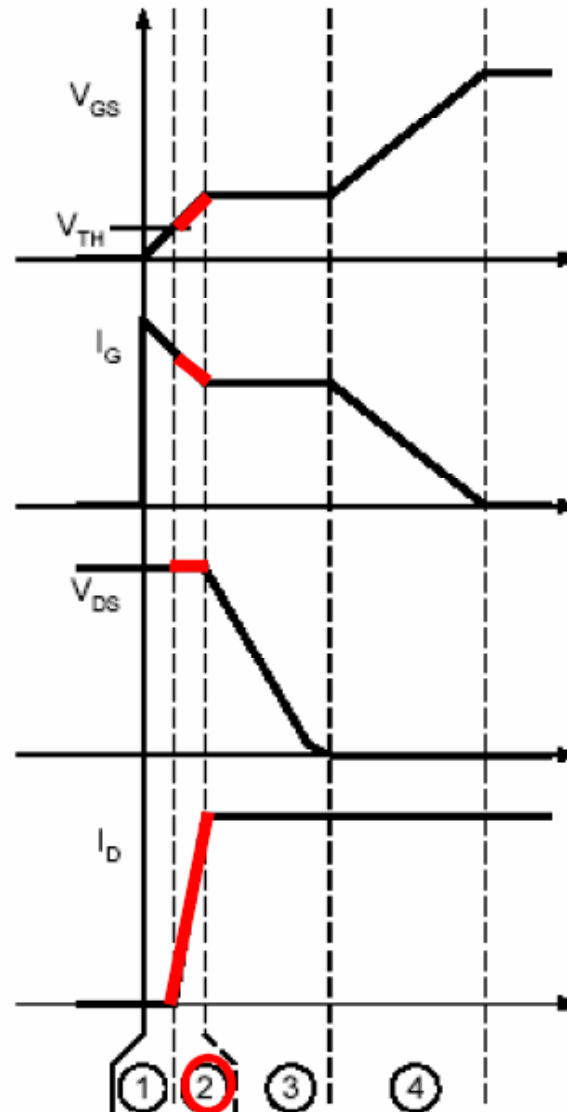
# MOSFET Switching Behavior : Turn-on



MOSFET Turn-On 4 stages

Reduce transition time during stage 2 to minimize switching losses

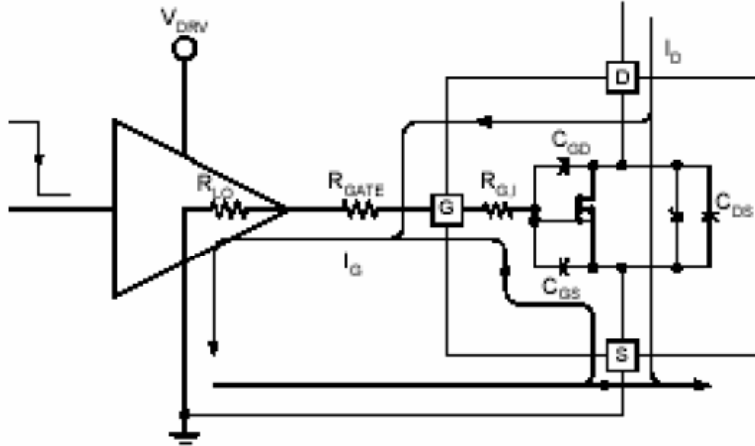
Critical Gate Drivers ability to source current



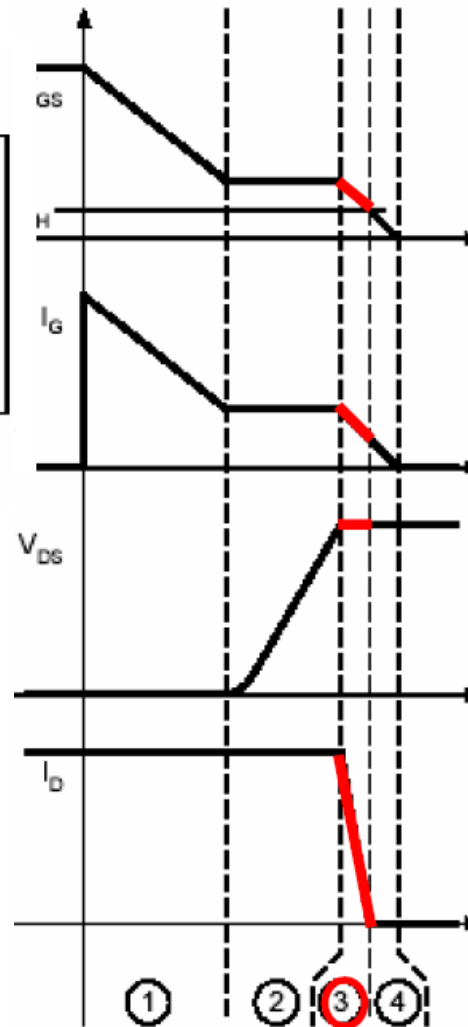
1. Turn-On Delay –
  - Input capacitor is charged from 0V to  $V_{th}$ .
2. Linear Operation
  - $V_g$  increases from  $V_{th}$  to Miller Capacitor
  - Mosfet is carrying the entire Inductor current.
3.  $V_{gs}$  is Steady
  - Driver current diverted to discharge  $C_{gd}$
  - Drain Voltage falls
4.  $V_{gs}$  increased from  $V_{miller}$  to  $V_{final}$ 
  - Mosfet fully enhanced
  - $C_{gs}$  and  $C_{gd}$  charged
  - $R_{ds\_on}$  reduced.



# Mosfet Switching Behavior : Turn-Off



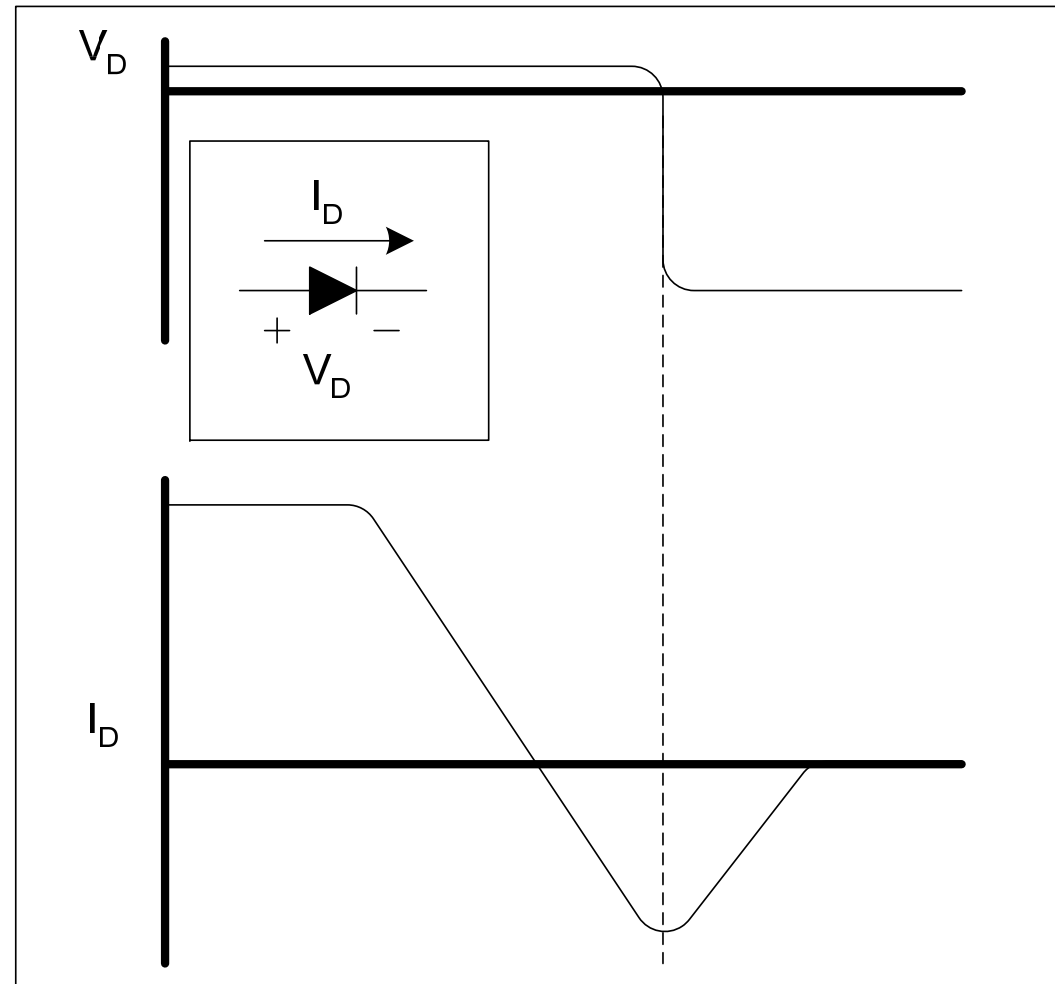
MOSFET Turn-Off 4 stages  
Reduce transition time during stage 3 to minimize switching losses  
Critical Gate drivers ability to sink current.



1. Turn-off Delay
  - Ciss is discharged from initial value to Miller Plateau.
2. Vds rises
  - Gate current is charging Cgd
  - Gate in its Miller Plateau
3. Mosfet in Linear mode
  - Vg falls from Miller to Vth
  - Cgs capacitor is started to discharged
4. Turn-off Stage
  - Vgs is further decreased with current coming out of Cgs capacitor.

# Diode Reverse recovery

- Current can flow from cathode to anode until diode turns off.
- This can produce
  - High peak currents
  - High dissipation:
    - In the diode
    - In other circuit components



# High Side Fet Losses

- Conduction and Switching Losses**

$$P_{conduction\_HS} = I_{q_{rms\_HS}}^2 R_{ds_{on}} = I_0^2 R_{ds_{on}} D$$

Switch conduction losses

$$P_{sw} = (1/2) V_{in} f_{sw} \{ [I_{q_{min}} t_2] + [I_{q_{max}} t_3] \}$$

Switching losses during turn-on and turn-off

$$P_{sw\_drv} = V_{drv} f_{sw} Q_g$$

Driver losses

$$P_{cos s} = 0.5 C_{oss} f_{sw} V_{in}^2$$

Capacitor drain-source losses

$$P_{Qrr} = Q_{rr} V_{in} f_{sw}$$

Reverse recovery losses

$$Q_{g\_sw} = Q_{gd} + 0.5 Q_{gs}$$

$$t_{sw} = Q_{gsw} / I_g$$

$$I_{g\_t2} = \frac{V_{drv} - (V_{th} + (I_{q_{min}} (1 / g_m)))}{R_g + R_{gext} + R_{drv}}$$

$$I_{g\_t3} = \frac{V_{th} + I_{qpk} (1 / g_m)}{R_{gfet} + R_{gext} + R_{drv}}$$

# Low Side Losses

- Profile of Loss in High side and Low side are quite different especially for Low output voltages.
- Low side losses are dominated by conduction losses
- High side conduction and switching losses

$$P_{conduction\_LS} = I_{q_{rms\_LS}}^2 R_{ds_{on}} = I_o^2 R_{ds_{on}} (1 - D)$$

**Select HS Mosfet for low Qg**

**Select LS Mosfet for low Rds\_on**

# Magnetic Materials

- **There are two classes of materials**
- **1. Alloys of iron, which contain silicon (Si), Nickel (Ni), Chrome (Cr) and Cobalt (Co)**
- **2. Ferrites – ceramic materials mixture of iron, Manganese (Mn), Zinc (Zn), Nickel (Ni) and Cobalt (Co)**

# Inductor Losses ( Conduction and Core)

## DCR losses

$$Inductor\_PL = I_{LF\_RMS}^2 r_0$$

$$r_0 = Inductor\_DCR$$

- Core losses
- Core losses can be calculated based upon flux density, frequency of operation, core volume
- Core vendors provide core loss data vs frequency used to estimate core losses
- For Ferrite cores: Steinmetz equation defines core losses

$$PL = K \beta^a \left(\frac{f}{10^6}\right)^b \left(\frac{V_e}{1000}\right)$$

$\beta = \text{flux\_density}$

$V_e = \text{core\_volume(cm)}$

$f = \text{frequency(khz)}$

Operating Magnetizing Force:

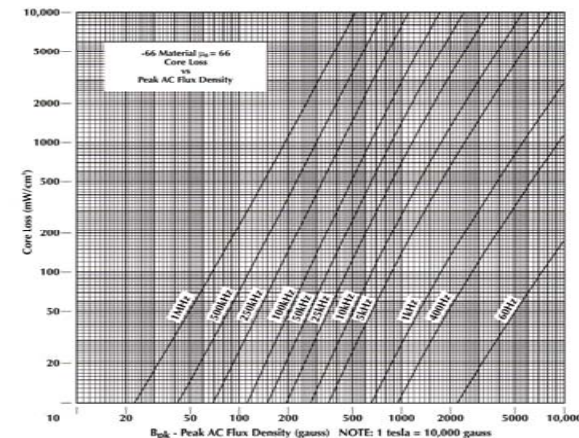
$$H_{dc} := \frac{0.4 \cdot \pi \cdot N \cdot I_L}{l_e}$$

DC Flux Density:

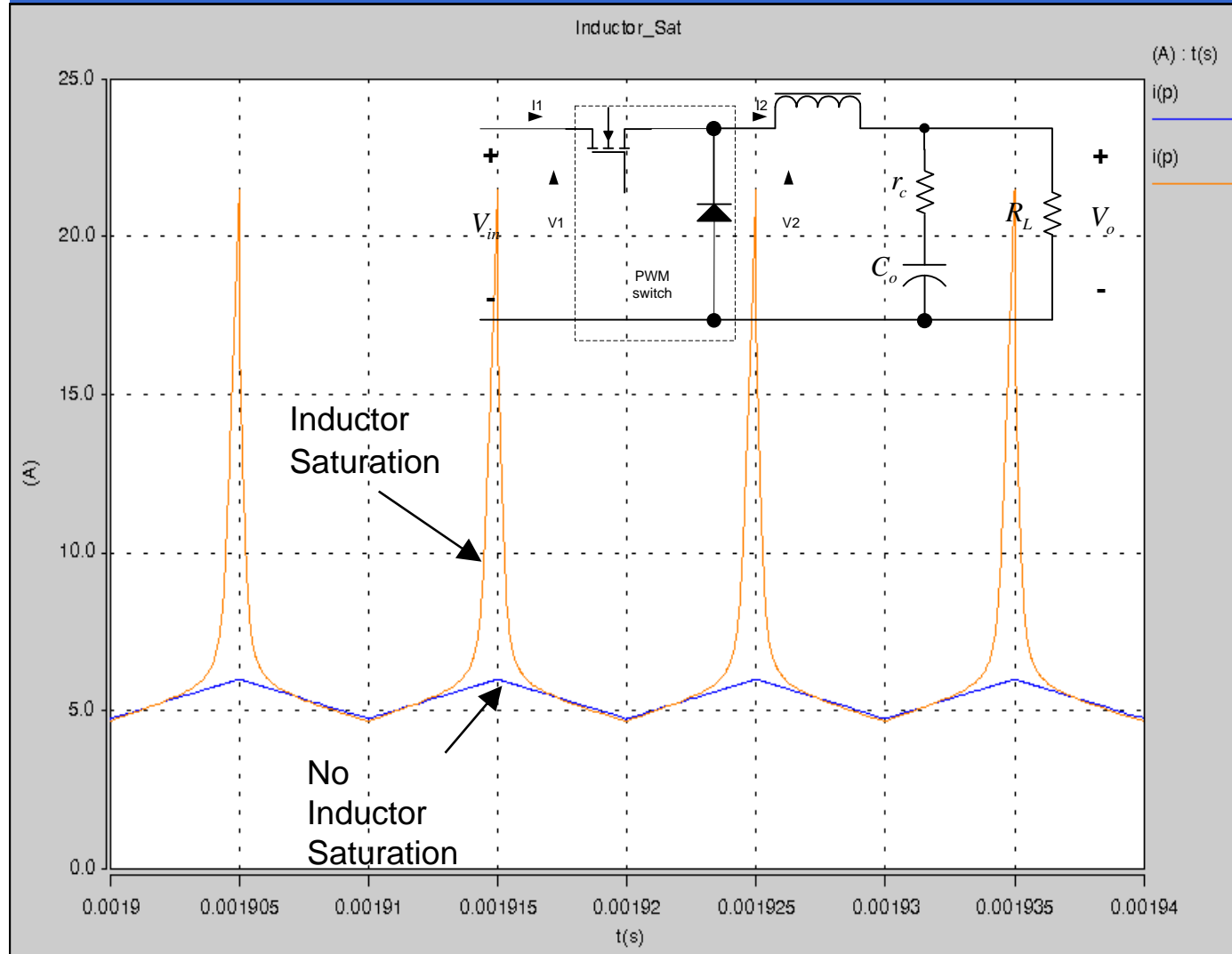
$$B_{dc} := \frac{L \cdot I_L \cdot 10^8}{A_e \cdot N}$$

Peak to Peak Flux Density:

$$\Delta B := \frac{V_o \cdot t_{off} \cdot 10^8}{A_e \cdot N}$$



# Output Inductor saturation behavior

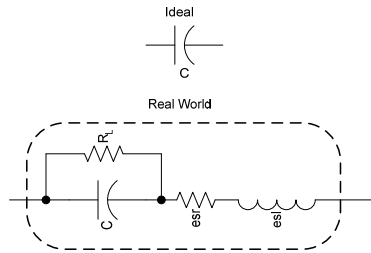


Waveform shows output inductor waveform in

- 1) normal operation
- 2) Inductor is saturated.
- 3) Saturation is reduction in inductance as function of current, which can destroy the MOSFET

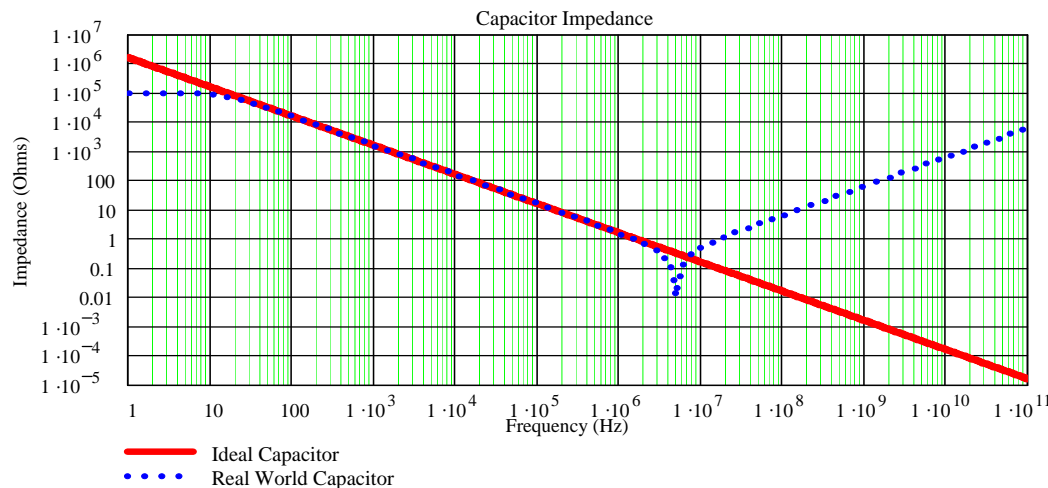


# Capacitor - Input / output



**Ideal Capacitor**

**Real World Capacitor**



**Input Capacitor selection criteria is to meet:**

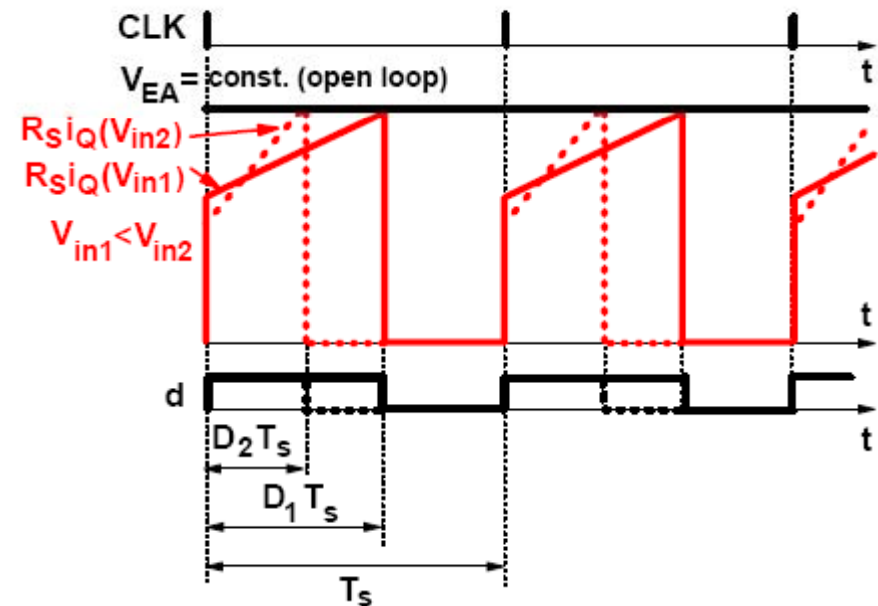
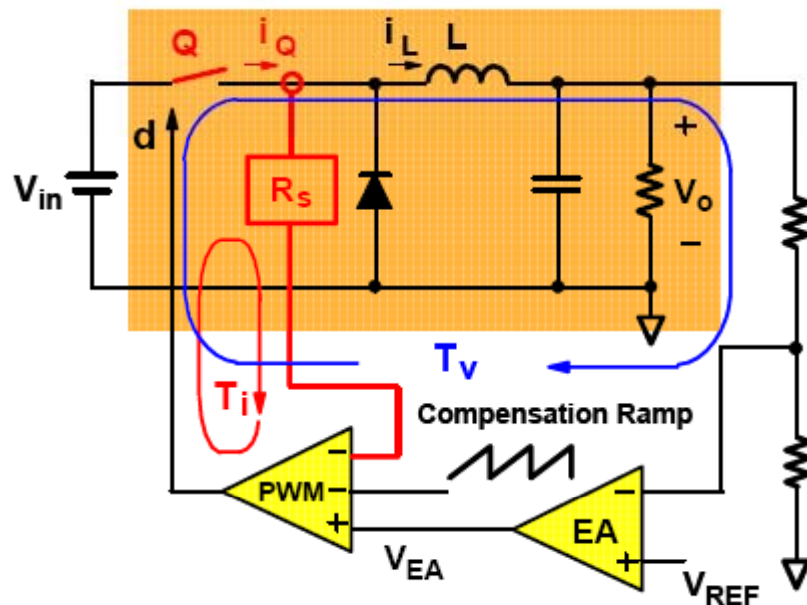
- Input capacitor rms ripple current rating

**Output Capacitor selection criteria is based upon**

- esr of the capacitor ( in order to meet o/p ripple voltage specification)
- Bulk capacitance to ensure it meets maximum overshoot/ undershoot during transient conditions.

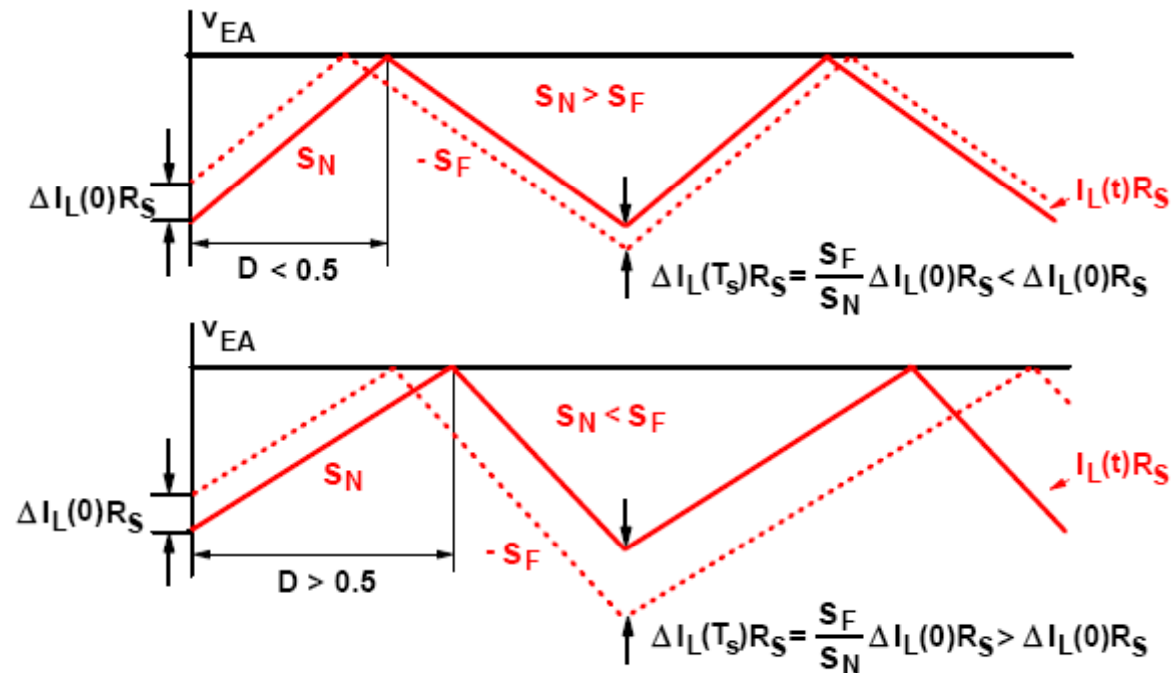
# Current Mode Control

- **Current mode Control has two loops**
  - Inner current loop
  - Outer voltage loop



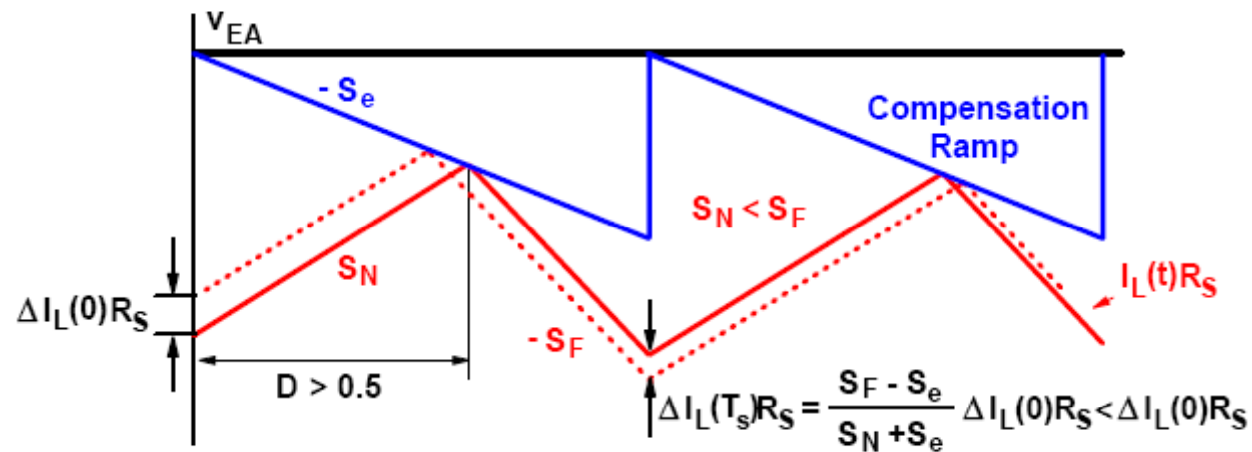
# Current mode control

- Current loop stable for duty cycle less than 50% for  $V_{in}=12V$   $V_{out} = 1.2V$  Duty cycle is 10%
- Current loop un-stable for duty cycle greater than 50% - requires slope compensation



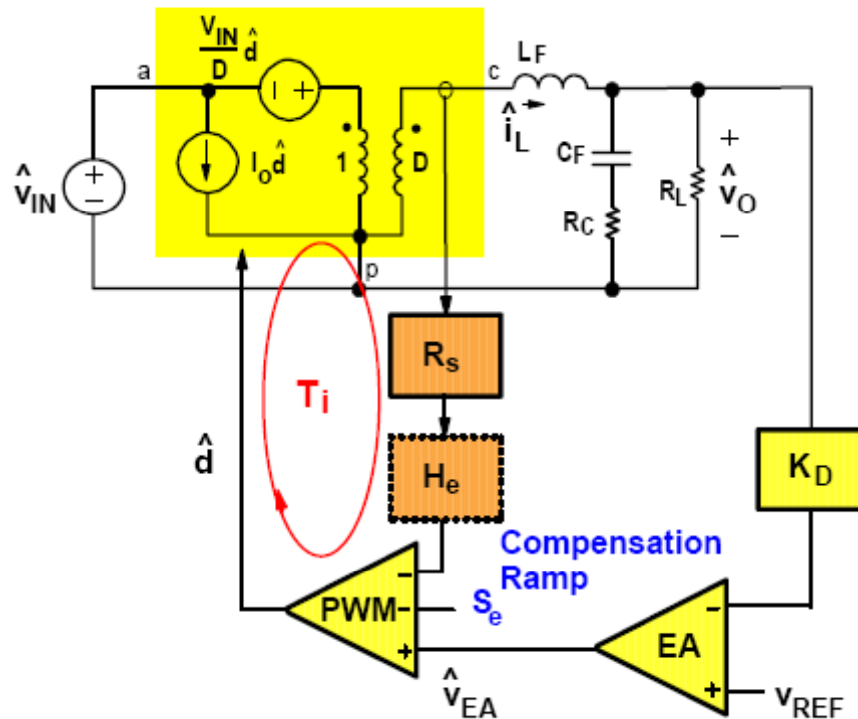
# Adding slope compensation

- For duty cycle  $> 0.5$  slope compensation required.
- Minimum slope required is  $\frac{1}{2}$  downslope of inductor current



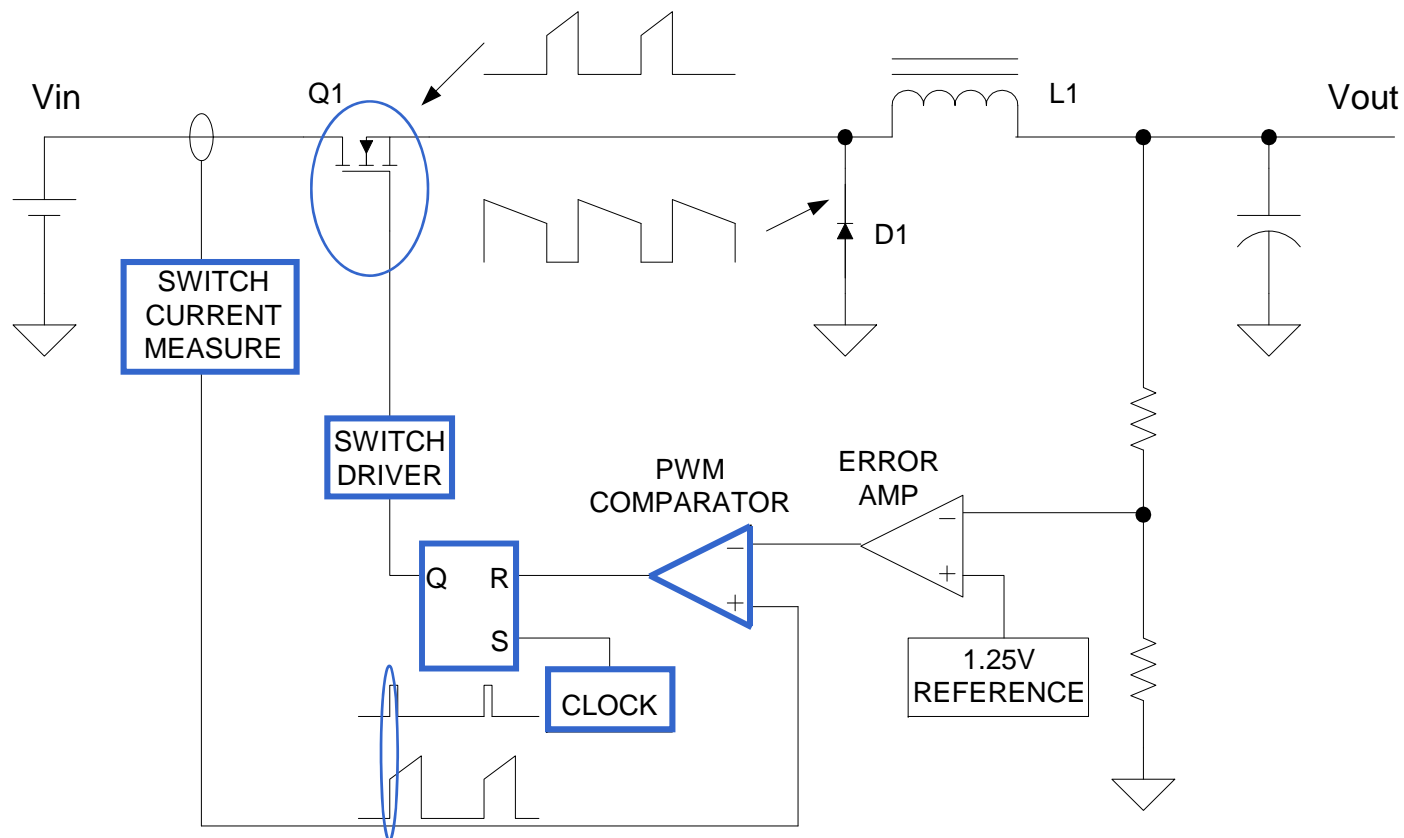
# Current loop

- Current loop is sampled data loop
  - Peak inductor current is sampled and held until next switching cycle
  - Transfer function  $H_e$  models sampling nature of current loop



$$H_e(s) = \frac{sT_s}{e^{sT_s} - 1}$$
$$H_e(s) \approx 1 + \frac{s}{\omega_n Q_z} + \frac{s^2}{\omega_n^2}$$

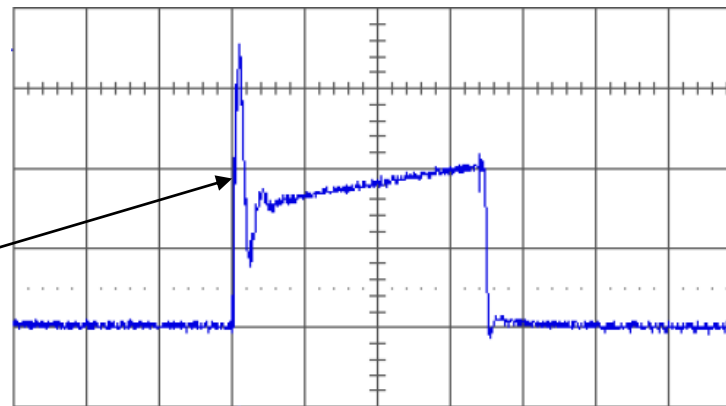
# Buck Regulator with Current Mode Control



# Why Emulated Current Mode?

- Step down switching regulators designed for high input voltages must control very short minimum on-times to operate at high frequencies.
- The maximum switching frequency (and size of the inductor and output capacitor) are function of the minimum on-time.
- The on-time of conventional current mode controllers is limited by current measurement delays and the leading edge spike on the current sense signal. When the Buck FET turns on and the diode turns off, a large reverse recovery current flows, this current can trip the PWM comparator. Additional filtering and / or leading edge blanking is necessary to prevent premature tripping of the PWM. The emulated current signal is free of noise and turn-on spikes.

**Leading edge spike,  
conventional current  
mode control.**



# Current Mode Control Advantages / Disadvantages

## ADVANTAGES

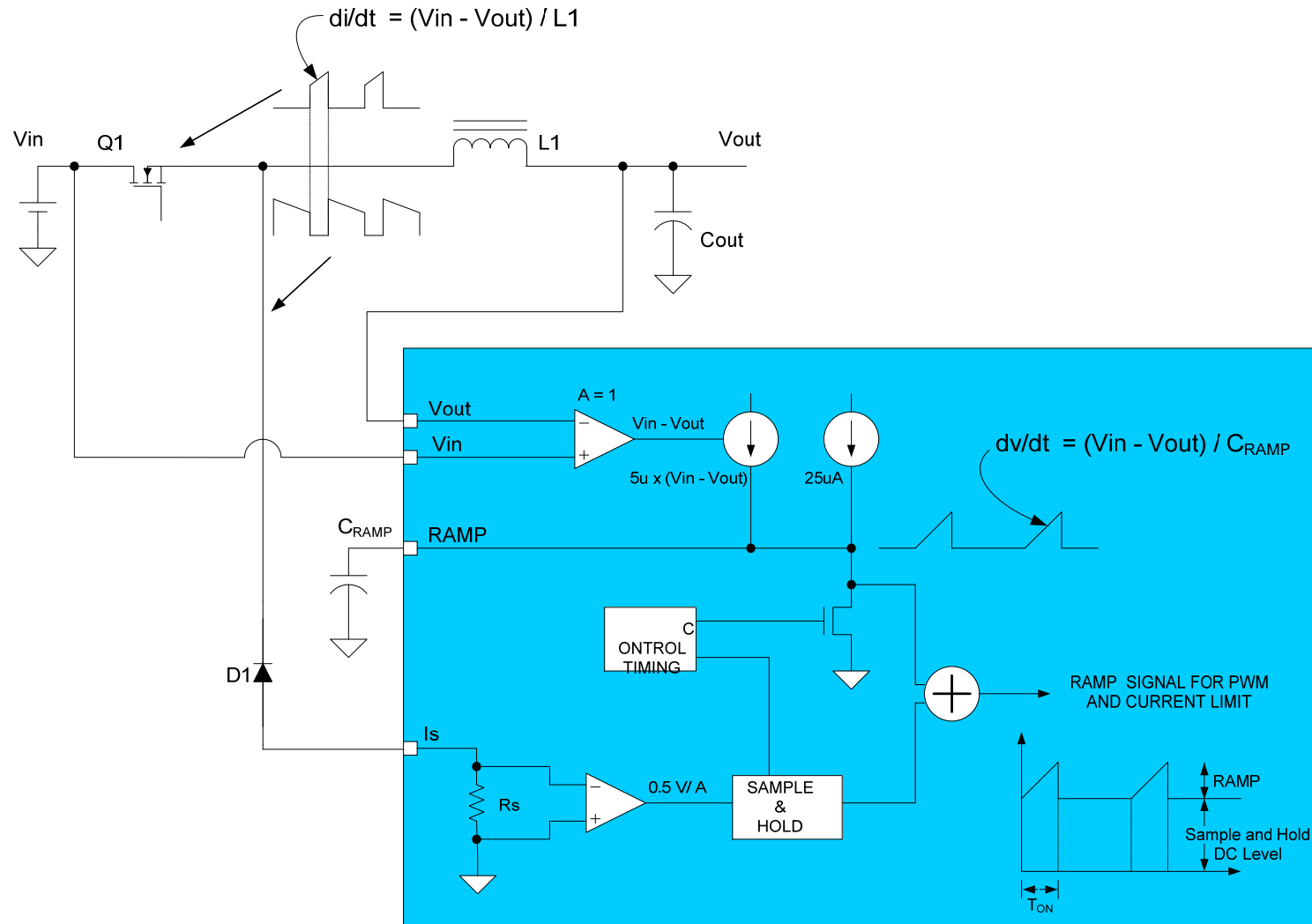
- Current mode control is a single pole system. The current loop forces the inductor to act as constant current source.
- Current mode control remains a single pole system regardless of conduction mode (continuous mode or discontinuous).
- Inherent line feed-forward since the ramp slope is set by the line voltage.
- By clamping the error signal, peak current limiting can be implemented.
- Ability to current share multiple power converters.

## DISADVANTAGES

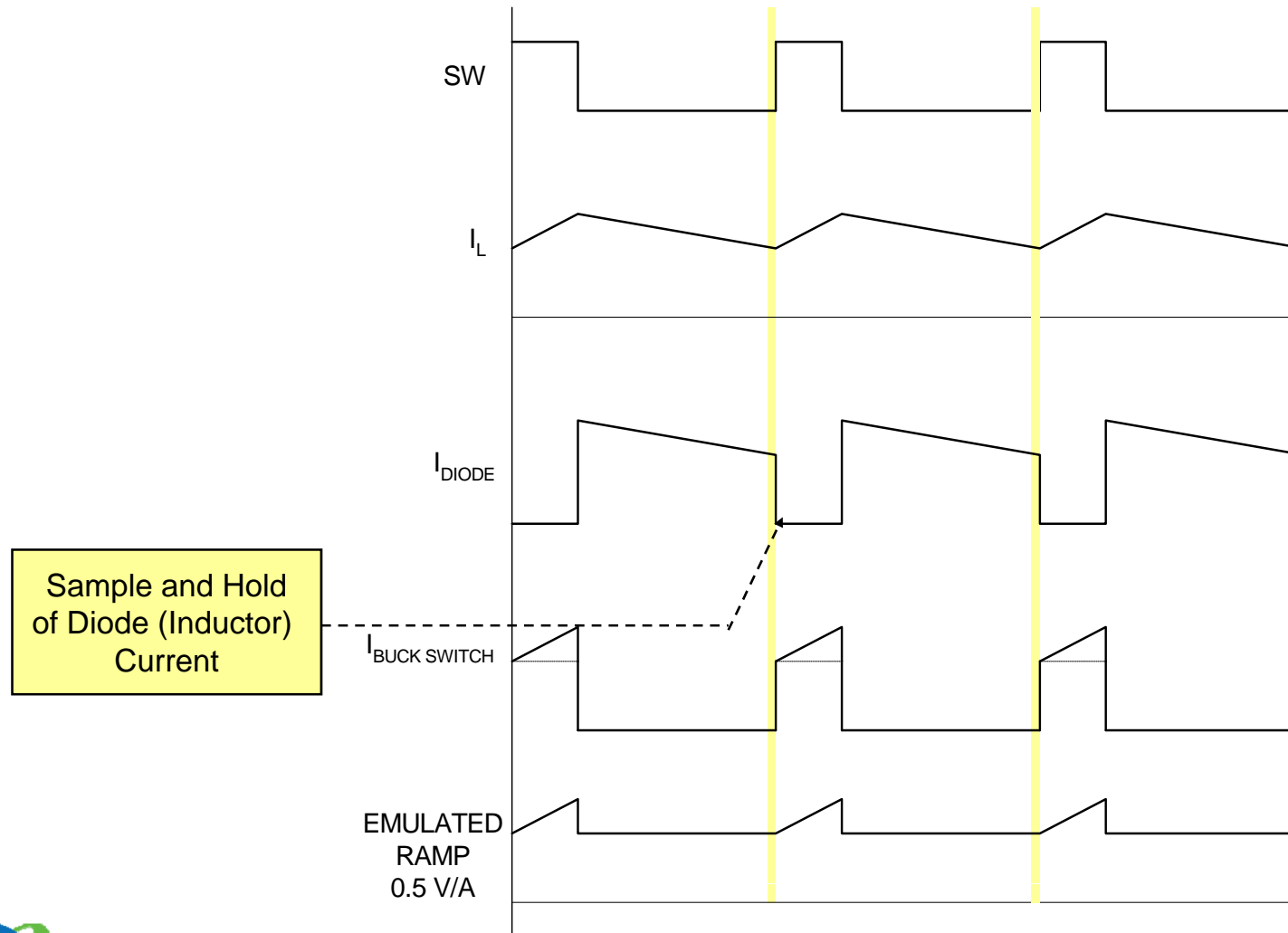
- Susceptibility to noise on the current signal is a very common problem, reducing the ability to process small on-times (large step-down ratios).
- As the duty cycle approaches 50% current mode control exhibits sub-harmonic oscillations. A fixed slope ramp signal (slope compensation) is generally added to the current ramp signal.



# Emulated Current Mode, How Does it Work?

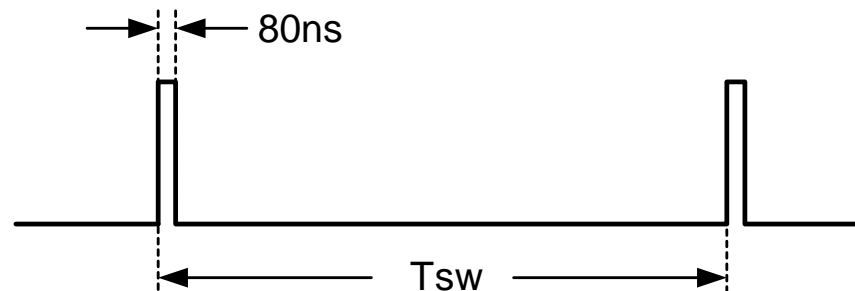


# Emulated Current Mode Waveforms



# Maximum Input Voltage vs Operating Frequency

- For a minimum on-time capability of 80ns, the minimum duty cycle is therefore 80ns x Fsw. For low output voltage, high frequency applications the maximum switching frequency may be limited. If  $V_{in\_MAX}$  is exceeded pulses will have to skip.



To calculate the maximum switching frequency use:

$$F_{sw\_MAX} = \frac{V_{out} + V_D}{V_{in\_MAX} \times 80ns}$$

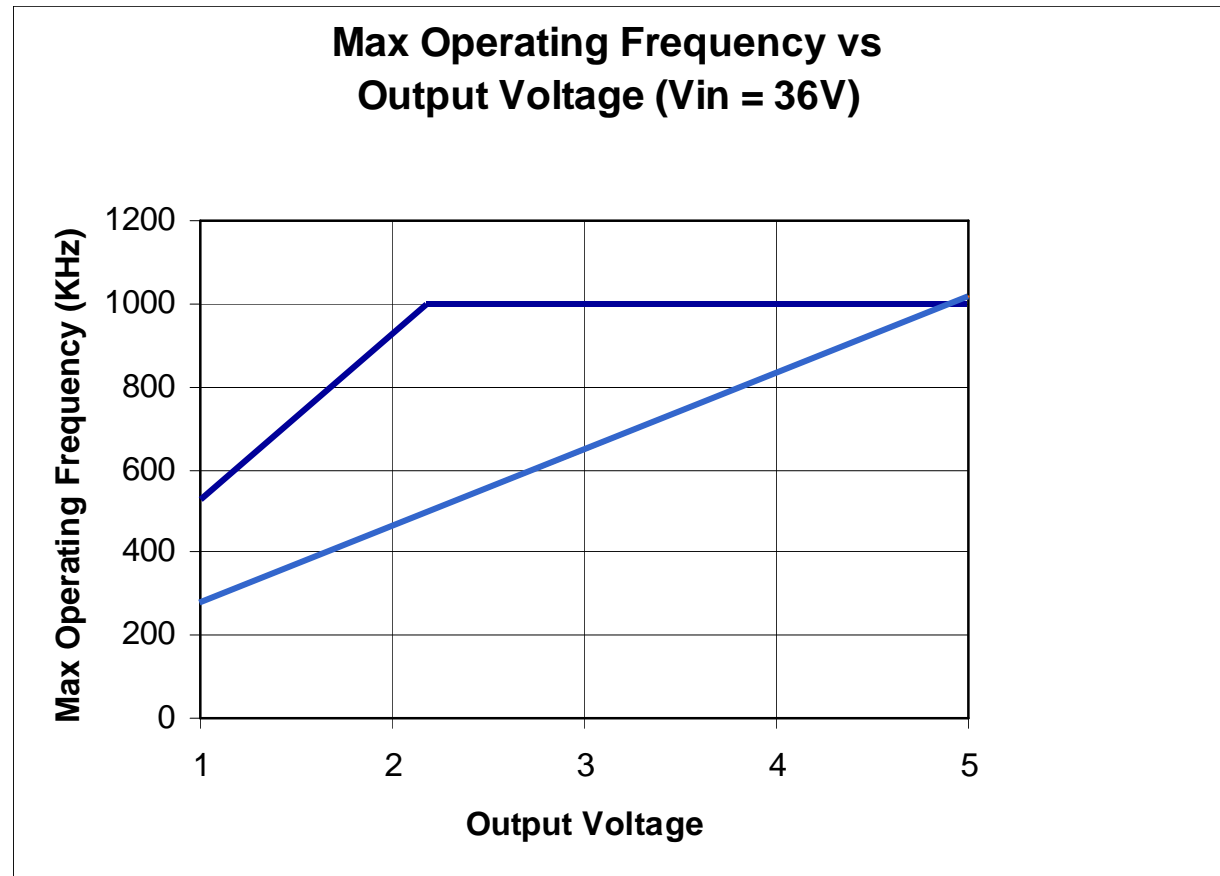
Where  $V_D$  is the diode forward drop

# Maximum Operating Frequency vs Output Voltage

For high input voltage applications the real maximum operating frequency is determined by the minimum on-time ( $T_{ON(MIN)}$ ) of the controller.  
$$F_{sw} = (V_{out} + V_d) / (T_{ON(MIN)} \times V_{in})$$

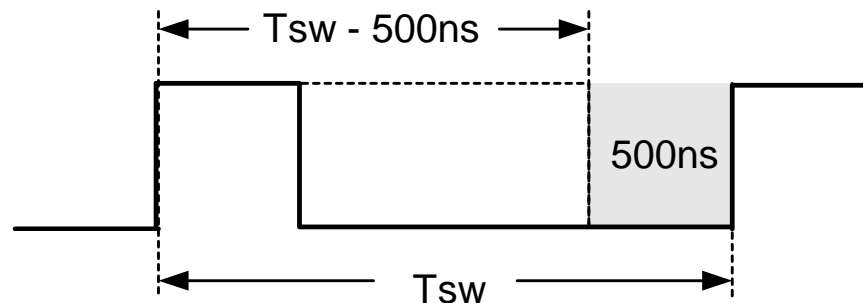
Max operating frequency vs output voltage for the LM2557X family.  
( $T_{ON(MIN)} = 80\text{ns}$ )

Max operating frequency vs output voltage for a “2.8MHz” device.  
( $T_{ON(MIN)} = 150\text{ns}$ )



# Minimum Input Voltage vs Operating Frequency

- A forced off-time of 500ns is implemented each cycle, to allow time for the sample & hold of the diode current. The maximum duty cycle is therefore limited to;  $1 - (500\text{ns} \times F_{\text{sw}})$ . For high frequency applications the minimum input voltage may be limited. If  $V_{\text{in}}$  is less than  $V_{\text{in}_{\text{MIN}}}$  the output voltage will droop.



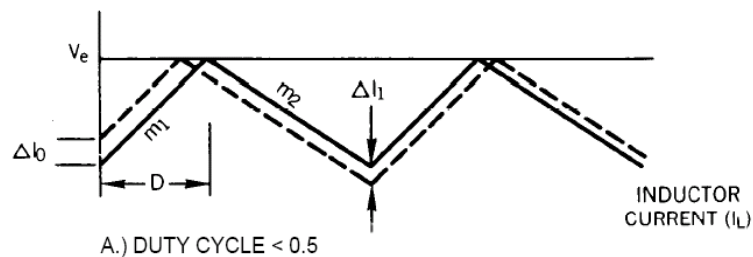
To calculate the minimum input voltage use:

$$V_{\text{in}_{\text{MIN}}} = \frac{V_{\text{out}} + V_D}{1 - F_{\text{sw}} \times 500\text{ns}}$$

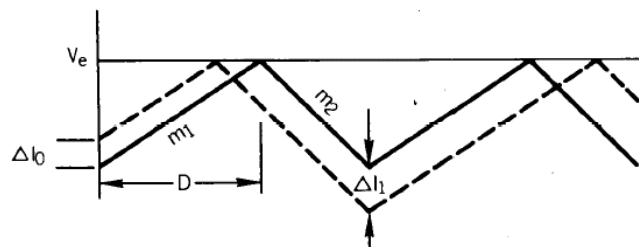
Where  $V_D$  is the diode forward drop

# Slope Compensation

**Background:** Current mode controlled power converters operating at duty cycles  $>50\%$  are prone to sub-harmonic oscillation. Disturbances in peak rising current ( $\Delta I$ ) increase at the end of the cycle.

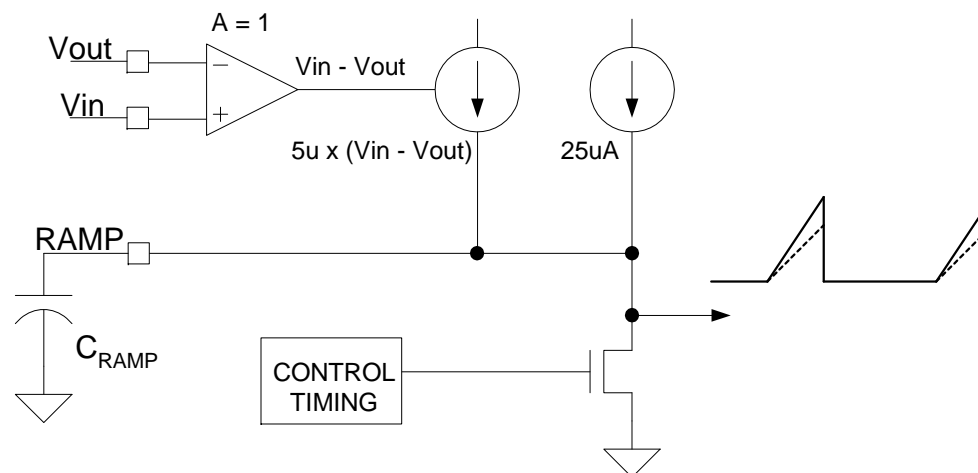


A.) DUTY CYCLE  $< 0.5$



B.) DUTY CYCLE  $> 0.5$

**Solution:** A  $25\mu\text{A}$  offset in the RAMP current source provides additional slope for the emulation ramp.



# Emulated Current Mode Advantages / Disadvantages

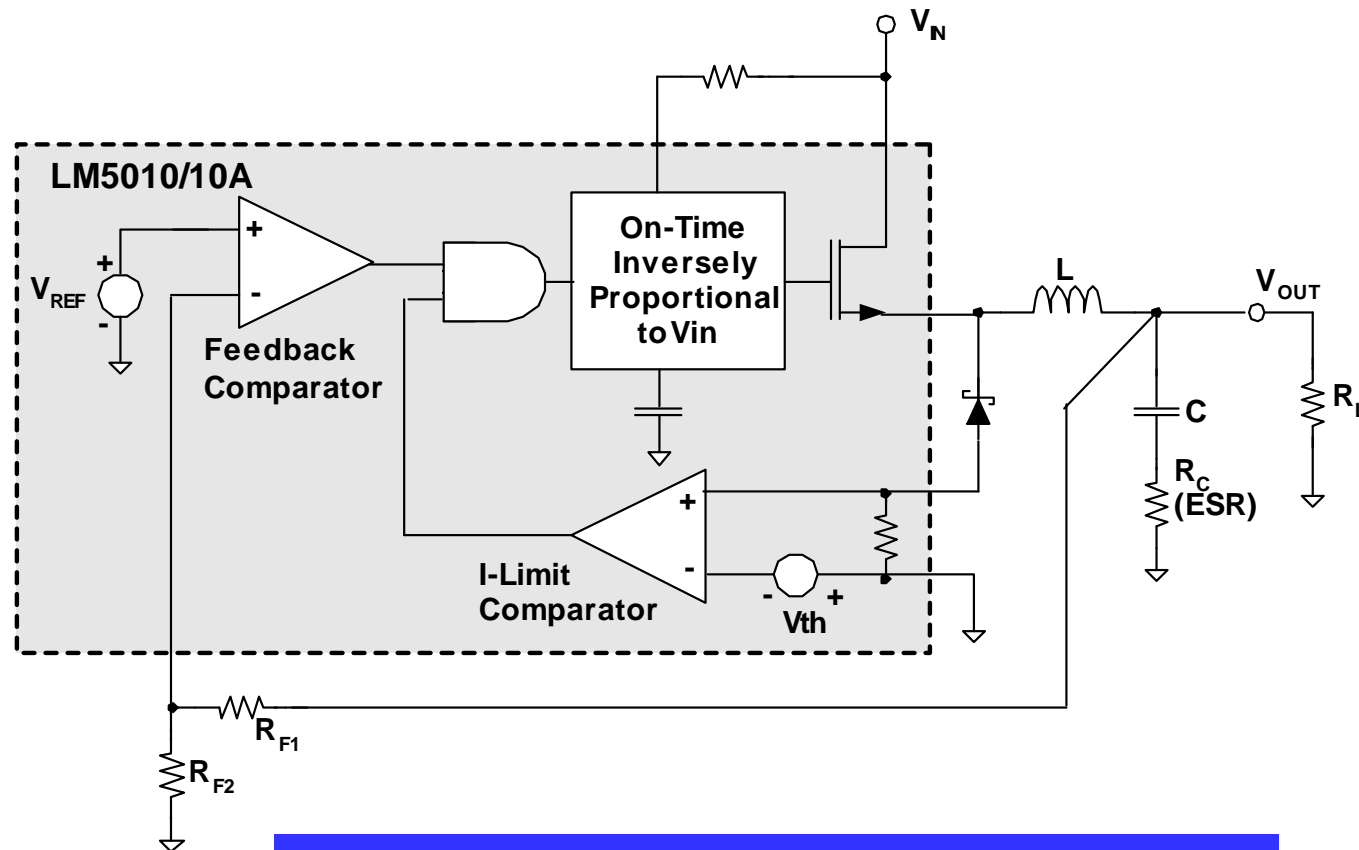
## ADVANTAGES

- Reliably achieves small on-times necessary for large step-down applications.
- All of the intrinsic advantages of current mode control are retained without the noise susceptibility problems often encountered from; diode reverse recovery current, ringing on the switch node and current measurement propagation delays.
- During short circuit overload conditions there is no chance of a current run-away condition since the inductor current is sampled BEFORE the buck switch is turned on. If the inductor current is excessive, cycles will be skipped until the current decays below the over-current threshold.

## DISADVANTAGES

- The maximum duty cycle is limited to less than 100% since off-time is required for the sample and hold measurement of the diode current.
- If the inductor saturates, it will not be detected.

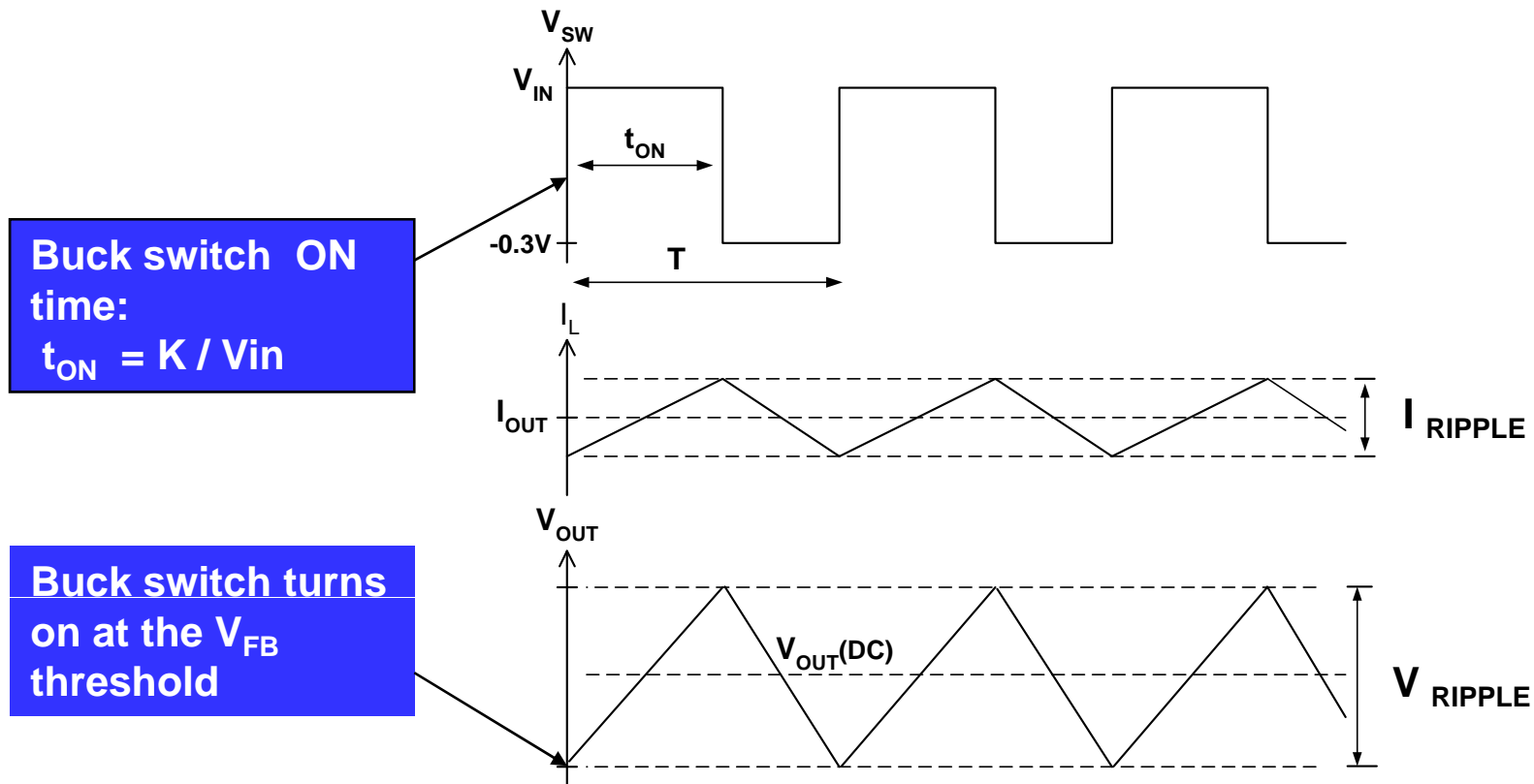
# Constant Frequency, COT Switching Regulator



Nearly constant operating frequency plus all of the benefits of the conventional Constant On Time regulator.



# Constant Frequency COT Regulator Waveforms (CCM)



$$\text{Freq} * t_{ON} = V_{out} / V_{in}$$

$$\text{but } t_{ON} = K / V_{in}$$

$$\text{Freq} * K / V_{in} = V_{out} / V_{in}$$

$$\text{Freq} = V_{out} / K = \text{constant for given } V_{out}$$

# Summary

- **Synchronous Buck converter is reviewed**
- **All critical Component and their selection criterias are highlighted.**
- **Small-signal model of converter is developed**
- **Various control architectures are reviewed for high-step down voltage ratios.**





Backup



# LM5010A High Voltage Step Down Switching Regulators

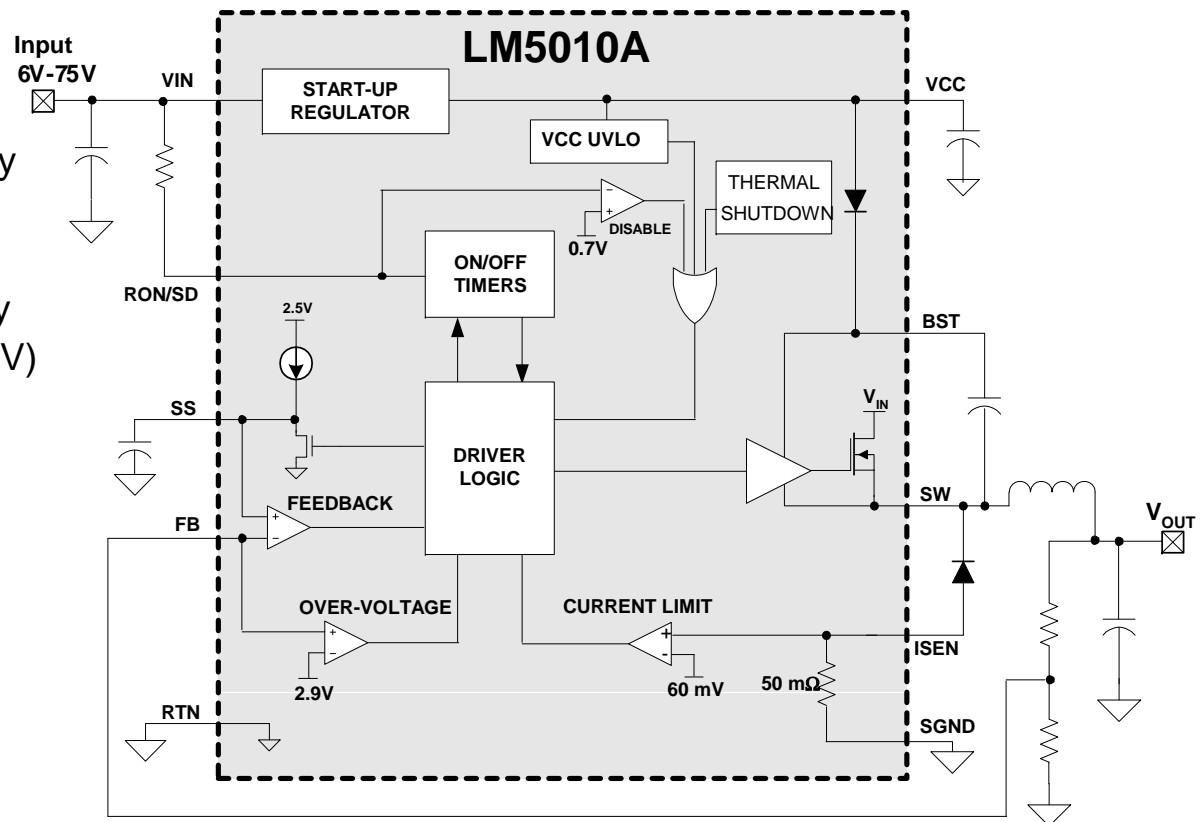
## Features

- Delivers 1A Continuous to Load
- Operates from 6V to 75V Input Supply
- Constant On-Time Control
- No Control Loop Compensation
- Nearly Constant Switching Frequency
- Adjustable Output Voltage (2.5V – 65V)
- Adjustable Soft-start
- Precision 2.5V Feedback Reference
- Low Bias Current (350uA, typ.)
- Adjustable Valley Current Limit
- Thermal Shutdown
- 125C Max. Junction Temperature

## Package

TSSOP – 14EP (4mm x 5mm)

LLP - 10 (4mm x 4mm)



# Operating Frequency vs Input Voltage (CCM)

