Contribution ID: 132

Design Considerations for High Step Down Ratio Buck Regulators

Wednesday 17 September 2008 15:05 (25 minutes)

Buck topology is the workhorse in most of the power electronic devices. Buck converter is step-down DC to DC converter. It utilizes two switches (two FETS or one FET and one diode) along with an output inductor and output capacitor.

Whether you look at the large computer server, personal computer Desktop or laptop, cell phone or GPS unit all will contain a buck topology design in one form or the other.

Summary

As the name implies Buck converter reduces the input voltage. The simplest way to reduce the input voltage is to use a voltage divider circuit, but this is very inefficient and as the excess voltage is wasted as heat. An alternate method that would not waste energy and be reasonably efficient in the range of 90 +% efficiency. This can be achieved by using two FETS which are turned on/ off at a specific frequency resulting in chopping the input voltage and followed by the output inductor and capacitor (which is a low pass filter) the resulting chopped DC voltage is filtered by the output LC providing a clean stepped down DC voltage. The switch connects the source voltage to the inductor, where the energy is stored and in 2nd phase inductor is discharged into the load.

Buck converter is the basic building block that drives the power electronics. There are various forms of stepdown converters, non-isolated or isolated versions of the same topology namely, push-pull, forward, flyback, active clamp forward are all isolated versions of step-down converters.

Prior to selecting the design approach, it is critical to understand the system needs/specs and design limitations The paper with go thru the small signal analysis of buck converter using Vaporian's switch model. This is a very powerful tool allowing one to analyze / simulate the circuit.

Considering the switching behavior of MOSFET is critical portion in order to evaluate the conduction and especially the switching losses associated with the topology. Both high side and low side MOSFET switching losses are analyzed. The drive circuitry along with the drive voltage plays a critical role in determining the switching losses. The paper will address these issues.

Primary authors: Mr KHANNA, Ramesh (National Semiconductor Corp.); Dr DHAWAN, Satish (Yale University)

Presenter: Mr KHANNA, Ramesh (National Semiconductor Corp.)

Session Classification: Parallel Session B5 - Power