Design, production and first operation of the ALICE Silicon Pixel Detector system

A. Kluge[a,*], G. Aglieri Rinella[a], F. Antinori[b], M. Burns[a], I.A. Cali[a,d], M. Campbell[a], M. Caselle[d], C. Cavicchioli[a], R. Dima[b], D. Elia[d], D. Fabris[b], M. Krivda[e], F. Librizzi[c], V. Manzari[d], G. Marangio[d], M. Morel[a], S. Moretto[b], F. Osmic[a], G.S. Pappalardo[c], A. Pepato[b], A. Pulvirenti[c], P. Riedler[a], F. Riggi[c], R. Santoro[d], G. Stefanini[a], C. Torcato Matos[a], R. Turrisi[b], H. Tydesjo[a], G. Viesti[b]

[a] CERN, Geneva, CH-1211 Geneva 23, Switzerland
[b] Dipartimento di Fisica dell'Universita' and Sezione INFN di Padova, Italy
[c] Dipartimento di Fisica dell'Universita' and Sezione INFN di Catania, Italy
[d] Dipartimento di Fisica dell'Universita' and Sezione INFN di Bari, Italy
[e] Comenius University, Bratislava, Slovakia

[*] alexander.kluge@cern.ch

Abstract

The ALICE Silicon Pixel Detector (SPD) constitutes the two innermost barrel layers of the ALICE experiment. The SPD is the detector closest to the interaction point, mounted around the beam pipe with the two layers at r=3.9 cm and 7.6 cm distance from beam axis. In order to reduce multiple scattering the material budget per layer in the active region has been limited to ≈1% X_0. The SPD consists of 120 hybrid silicon pixel detectors modules with a total of ~10^7 cells. The on-detector read-out is based on a multi-chip-module containing 4 ASICs and an optical transceiver module. The readout electronics, located in the control room, is housed in 20 VME boards; it is the interface to the ALICE trigger, data acquisition, control system and detector electronics. In this contribution the SPD detector components design and production are reviewed. First operation results are reported.

I. SPD detector overview

The SPD [1] consists of 120 detector modules, the half-staves, which are arranged in two cylindrical layers at 3.9 and 7.6 cm from the beam axis. Each detector module comprises two ladders; a ladder consists of 5 pixel chips [2] with 8192 pixel cells each, bump bonded to a sensor using Sn-Pb bumps of 20 μm diameter [3]. In order to achieve the lowest material budget, the pixel chips are thinned to 150 µm and the sensor thickness is 200 µm. In total the SPD contains 9.83 x 10^6 pixels. At the end of each half-stave a multi chip module (MCM) [4] reads out the 10 pixel chips. The MCM contains 4 ASICs, the rx40 [5] to receive an LHC synchronous clock and serial data on optical fibers, the digital pilot chip [6] to configure and read-out the pixel chips, the 800 Mbit/s serializer chip GOL [7] to send the data on one optical fiber from the detector to the control room and the analog pilot chip [8] to provide bias voltages to the pixel chip. The electrical connection between the pixel chip and the MCM is done via a aluminum based multi-layer flat cable, the pixel bus [9]. An aluminium-kapton foil, the grounding foil, is electrically separating the half-stave from the carbon fiber support structure. Cooling pipes are directly integrated into the carbon fiber structure [10]. Copper and kapton flat cables deliver electrical power to the half staves.

II. SPD system components

A. *Pixel ASIC*

The pixel ASIC [2, 11] contains 256 x 32 pixels and the read-out is based on a binary concept, where the full matrix is shifted out on a 32 bit bus in 256 consecutive 10 MHz clock cycles. Each pixel chip generates a pulse (fast-Or) whenever at least one pixel cell detects a particle signal above threshold. The fast-Or is used to implement a prompt trigger which contributes to the ALICE L0 trigger.

The functionality of the ASIC from the first engineering run proved to be acceptable. Three production runs were carried out between 2001 and 2003. The ASIC working parameters can be adjusted via internal DACs, remotely programmable. The optimization was done using a dedicated MCM emulator test system based on a waver prober developed for that purpose. The same system was also used to test the ladders.

B. *Multi-chip module ASICs*

The ASICs mounted on the MCM are all produced in 0.25 μm CMOS using radiation tolerant layout techniques. Triplication of sensitive logic cells performs SEU protection. A VME and FPGA based prototype was used to define and verify the functionality of the digital pilot chip. This VME board was also used in the pixel chip and ladder acceptance test system. The first version of the pilot chip was designed in 2002 and successfully tested. In 2003 a modified version was produced which included the functionality to transmit the fast-Or signals off the MCM. The fast-Or output of the pixel chip indicate the presence of at least one hit in the pixel matrix. The analog pilot was designed and tested during 2003. For the digital and the analog pilot chips dedicated test boards were produced. The full quantity of both chips was produced in multi project wafer runs. The rx40 and GOL chips were produced in common LHC projects and were used without modification.

C. *Multi-chip module*

The first prototype was based on a 5 layer FR4 PCB. This version used the rx40 block inside the digital pilot. However,

later tests later showed that the internal rx40 picked up clock switching noise in the pilot chip. A smaller version of the MCM containing an rx40 chip was produced in 2003. The FR4 PCB technology did not allow to compress the required traces in the available space. One prototype generation of the MCM was implemented using ceramic hybrids. However, they were abandoned as the yield of the hybrids was low. Finally a kapton based hybrid was used in Sequential Build Up (SBU) technology with trace widths of 80 μm and via sizes of 150 μm.

A dedicated VME based test system was developed which emulated the pixel chips and directly connected the off detector electronics (link receiver) to the MCM. All MCMs were temporarily wire bonded to a test card which was plugged into the test system [12]. The requirements on the optical transceivers included dimensional (< 1.5 mm package thickness) and radiation constraints that could not be met by commercially available components. A custom made optical component containing two PIN diodes and one laser diode was developed [4].

All MCMs went through an automated acceptance tests and a temperature cycling procedure (10 cycles in 10 hours from 15 to 50 degree). The temperature limits were defined by the dew point and the maximum temperature for the optical component.

D. Pixel bus design flow and test systems

The connection between the pixel chips and the MCM is done with a 5-layer aluminum kapton based flat cable, the pixel bus. The pixel bus is 166 mm x 13.8 mm x 0.35 mm in size.Aluminum was chosen as conductor in order to reduce the material budget of the half-staves to a minimum [4]. No commercial processes for such components could be found. The CERN printed circuit workshop developed a custom process and produced the full quantity.

Two layers are reserved for power and ground connections. The pixel chip has separate connections for analog and digital supply. However, tests showed that the two supply connections can be connected together outside the chip without loss of performance. Three planes were used for the transmission of signals, the 32-bit data bus, the 10-bit fast-Or bus and the 25-bit control bus.

The bus manufacturing principle [9] is to glue three aluminium kapton foils together which form the first two 50 μm layers containing ground and power lines and the first 10μm thick signal layer. Then a kapton foil is attached and the vias to the preceding layer are generated. For layer 4 and 5 10 μm aluminium is deposited via vacuum evaporation, onto a kapton foil and again the vias to the preceding layer are formed. As the production of aluminum vias is a delicate process and in order to reduce the number of vias each layer was made accessible for wire bonding on the edge of the bus by reducing the width by 500 μm compared to the layer below.

The R&D process for the bus was started with a 7 layer copper based prototype where the analog and digital power supplies were still separated. The first prototype bus and two ladders were glued next to each other and wire bonded. This required the bus connections to be swapped compared to the final design where the ladders are sitting below the bus. On this mirrored bus electrical acceptance tests were conducted taking the different resistivity between aluminum and copper into account. The next prototype step involved fully functional 5 layer copper busses where also the mechanical dimensions have been adapted to real needs and the first detector half-stave was assembled. In the last stage aluminum prototypes and production series were constructed. The major difficulties were to find the correct process parameters for the aluminum deposition and etching of the vias. While the edging process for copper micro vias is well known, the chemical process parameters for aluminum needed to be determined. As the process is run in many sequential steps where each step is potentially destructive, each new layer was tested for short circuits or interruptions.

The final bus was equipped with SMD decoupling capacitors, pt1000 temperature sensors and pullup resistors. As PCB tester machines are not suited to test automatically PCBs with mounted SMD components and are also incompatible with the fragile aluminum bonding pads, each bus was temporarily wire bonded onto a carrier card which was connected to a test system emulating the pixel chips and MCMs, thus testing each line on the pixel bus. This cumbersome test procedure was required to avoid attaching a defective bus to the expensive detector module components, as this assembly is hardly reworkable.

The R&D process started in 2001, the first mirrored/non-mirrored copper busses were delivered 2002/2004, the first aluminum busses were delivered 2005 and the full production was finished in 2007.

E. SPD off-detector read-out electronics

The 120 half staves are controlled and read-out via 20 VME based electronic boards, the router cards, which are sitting in the control room located at about 100 m from the detector. Each of the router cards houses 3 daughter cards (link receiver) which communicate with two half staves. The routers multiplex the data from the link receiver cards and send them via the ALICE detector data link (DDL) to the DAQ. Furthermore the routers form the interface to the ALICE central trigger processor via the TTC interface and detector control system via a VME connection.

One of the challenges during the production of the router cards was to gain experience with the mounting of large ball grid arrays (BGA) and produce 9U VME cards with a flatness compatible with BGA mounting. The router cards contain BGA packages with 1020 pins. The acceptance test are based on boundary scan methods allowing to pin point directly faulty solder connections using a board wide JTAG chain. In certain cases FPGAs with few soldering faults were found, in other cases the soldering faults were so severe that not even the

JTAG port was accessible. The boundary scan feature was of great value as X-ray tests of the solder joints would not always show the faulty connection. However, after unmounting the component it was visible that some solder pads still were not even wetted by solder.

The general testing of the router and link receiver printed circuit boards was rather straightforward. The electrical functionality was verified using the JTAG boundary scan method. The processor functionality, the functionality of the optical components and the FPGA firmware of the link receiver cards were verified using a dedicated hardware test bench which emulates the components connected to the link receiver card. In general the basic commissioning of the FPGA firmware was simple as the entire system including the detector ASICs and PCB board connections was simulated using HDL system simulations prior to board fabrication. This allowed the verification of the interfaces to the DAQ, the trigger, the ALICE DCS and the SPD detector modules already before the system installation. It is difficult to simulate rare cases of high occupancies in the multi event buffers due to the extremely long simulation times. During the SPD pre-commissioning time the entire detector system has been built up on the surface which allowed on-line tests. Later-on, after the system installation in the cavern, dedicated system runs were performed to provoke rare conditions.

The R&D phase for the routers and link receivers started in 2002 and took until 2005, when the full production of 20 router boards and 72 link receiver cards was launched.

F. Pixel trigger processor

The SPD pixel chip has a digital output, the fast-Or output, which is activated if at least one out of the 8192 pixels has been hit. The fast-Or output of each pixel chip is transmitted on the optical fiber to the pixel trigger processor (PIT). The PIT extracts the 1200 fast-Or bits and applies the pixel trigger algorithm in order to provide a L0 input trigger signal to the ALICE central trigger processor CTP within 800 ns [13, 14]. The PIT system comprises one 9U sized mainboard with one Xilinx Virtex4, 1513 pin FPGA acting as the trigger processor. The main board carries 10 daughter cards which receive 12 optical fibers each, extract the fast-Or bit information and send it to the main board. As the system is very compact in design initial concerns about cooling issues where studied using cooling simulation models. The design and production of the boards were straightforward and both the prototype and production boards were working immediately. This was possible due to the learning phase during the production of router and link receiver cards and again the intensive use of simulation verification on board level prior to the production of the boards.

The R&D phase for the system started early 2006 and the production was finished in end 2007.

G. Surface detector system test

The full detector system including read-out, DAQ, DCS, trigger, cooling, optical and electrical cabling and power supplies was integrated and tested in a dedicated area in the CERN Departmental Silicon Facility during several months for most components. Functionality tests of the full detector were performed. A burn-in of the off- and on-detector electronics was carried out. At the same time as much as possible of the read-out electronics was commissioned. The progress in the test and integration of the hardware and software systems was constrained by the deadlines for the installation of the SPD in the experiment. The test period went from mid 2006 to mid 2007 [3].

H. Installation of electronics, power supplies, electrical and optical cables

The SPD off-detector read-out electronics is installed in the surface control room in 2 VME crates and thus easily accessible for maintenance. The low voltage system is based on CAEN EASY 3000 [15] system. The control main crate is located in the surface control room and the LV supply modules are located in the cavern. 20 A3009 modules serve the detector. Each module has 12 floating channels with differential sense lines for 6 half-staves without local regulation - 1.8V for the pixel chip supply and 2.5V for the MCM supply. The maximum length of the LV power supply cables is about 38 m. The bias voltage for the silicon sensors is provided from the control room using CAEN 1519 modules housed in the main control crate. 12-channel coax cables run from the control room all the way to the sensors. The cable length is about 100 m.

The two optical input lines of the MCM carrying clock and serial data are routed from the control room to the 120 half-staves in about 110 m. The data lines of the half-staves go to the pixel trigger crate in the cavern on a 38 m long path on the A side of the detector (36 m on the C side). There the fibers are split, one branch goes to the trigger processor, the other continues to the control room. The length of the fibers from the splitter to the control room is about 70 m. All fibers in the system have been matched in their length with a precision of 30 cm for the different sections. This ensures that the phases of all half-staves are aligned to each other without the need of individual delay tuning. For the data lines from the half-staves to the PIT the cable path has been designed to be as short as possible such that the fast-Or signal is delivered to the pixel trigger processor in the shortest possible time.

Due to the layout of the ALICE experiment between the control room and the half-staves patch panels have been installed creating 5 break points. These break points have a strong impact on cost and reliability. The test of the detector with power on could only be carried out once the cables and cooling pipes were installed. Some patch-panels were then no longer accessible. Therefore during the installation intensive test sequences were carried out in order to ensure the integrity of the connection.

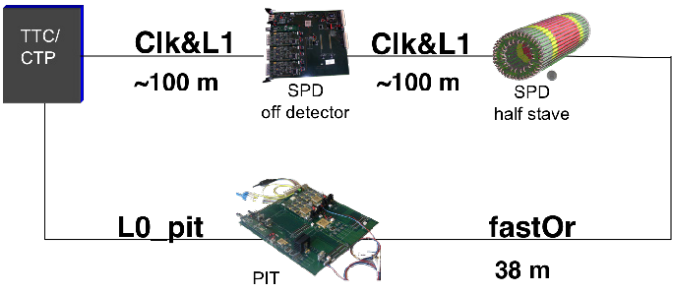

Figure 1: Simplified system block diagram.

Transient voltage suppressors (TVS) where installed as close as possible to the detector [15] in order to protect the detector modules from electrical over stress. The design and production of the cabling network started in 2005 and was terminated in 2007. The installation of the electrical and optical cables was started at the end of 2006 and completed in 2007.

I. Interlock system

The temperature of each half-stave and MCM is constantly measured with 11 sensors (1 per read-out chip and 1 per MCM). The information is sent via the optical link to the control room, where the read-out electronics and the software based DCS evaluate the temperature and control the power supplies. In addition to this interlock chain a PLC based system in the cavern reads the temperature sensors from the half-staves and acts as a direct hardwired interlock to the power supplies. The system was conceived in 2006 and installed in 2007.

III. System, commissioning and first runs

Fig. 1 shows a simplified block diagram of the SPD system. The fast-Or signals from the half-staves are processed in the PIT to form the SPD L0 trigger decision which is forwarded to the ALICE central trigger processor (CTP). Via the TTC system the clock and the trigger decision are received by the SPD off-detector electronics. Upon reception of a positive trigger decision the SPD is read-out via the off-detector electronics.

The ALICE silicon pixel detector has been installed inside the experiment in June 2007. The detector surrounds the beryllium beam pipe; the minimum distance to the inner layer modules is ~5 mm. In the following months the silicon strip and silicon drift detectors as well as the Time Projection Chamber (TPC) have been moved over the SPD. The cabling and cooling connections could be completed only in November 2007, when the mini-frame supporting the overall cabling was lowered into the cavern. Extensive tests of the electrical and optical cabling have been performed before actually powering the system to avoid damage to the detector caused by any possible cabling mistakes.

In December 2007 a two-week cosmic ray run has been carried out in which one side only of the SPD was operated. The second side could not be operated because the necessary power supply modules had not been delivered at that time. Another cosmic ray run took place in February/March 2008; this was the first time the full detector was operated. Both cosmic run periods allowed commissioning tests of the cooling system, the cable and power supplies and the detector electronics. The first cosmic events have been recorded in the SPD in February 2008. Data acquisition test and noise run tests verified that detector parameters were unchanged compared to the laboratory setup. In the full ALICE setup the SPD maximum design data taking rate of 3300 Hz was verified. Long term and high trigger rate tests allowed to examine and eliminate rare multi-buffer overflow conditions. Dedicated trigger test sequences were performed where L2 accept and reject signals were mixed. For each L2 accept event test pulses were initiated in the front end electronics. Off-line verification proved that each L2 accept was recorded whereas L2 rejects were deleted. The pixel trigger processor was then setup and thus allowed the commissioning of the detector with the pixel trigger to capture cosmic events. The first cosmic events have been recorded in the SPD in February. Since then the detector has been operated almost without interruption. Figure 2 shows an cosmic event display. Intensive trigger and DAQ tests allowed optimising the read-out electronics and control software. The first particles generated by injection tests in LHC have been recorded in the SPD in June 2008. Figure 3 shows an event display during a

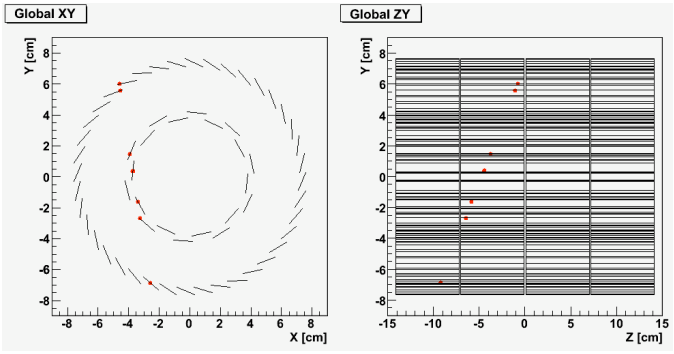

Figure 2: Event display of a cosmic ray triggered by the pixel trigger.

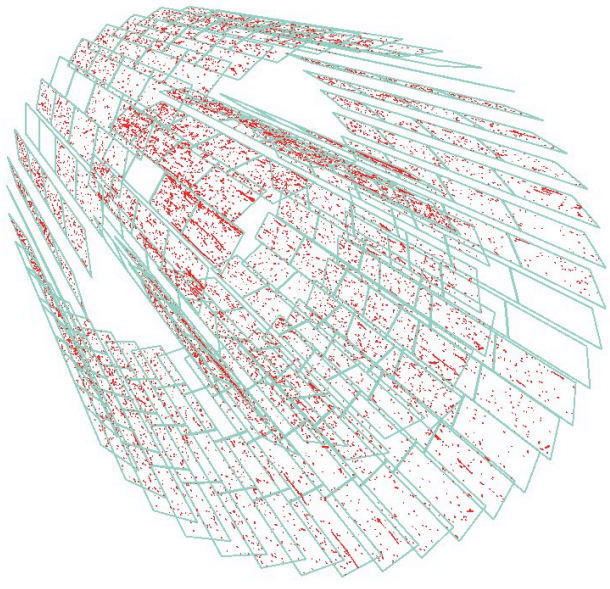
Figure 3: Event display during an beam injection.

beam injection test in August 2008.

Great effort has been put into automatic control procedures. Upon each start of an acquisition run the SPD DCS verifies the proper configuration of the electronics and resets the system in order to avoid errors due to wrong manual configuration but also to clear processes and buffers left from a run not having been terminated properly.

In the meanwhile the SPD has taken thousands of self-triggered cosmic events for geometry alignment and provided a stable trigger signal to the other ALICE detectors. The system runs stable over months. The continuing effort is dedicated to automatisation, such as power-on and -off procedures and the automatic recognition of errors or trends which might lead to errors, allowing non-experts to operate the detector.

IV. SUMMARY

The SPD system development has been successfully terminated. The system is installed and operating stably. An overview of the design and commissioning process has been given. The implementation of the SPD system was a technological challenge. The commissioning results and the performance of the system show that this challenge has been appropriately met. The experience gained shows that early R&D work for sub elements and production of building blocks such as ASICs must go very closely together with the system development in order to optimize use of resources, performance and reliability.

V. REFERENCES

[1] The ALICE Collaboration, K. Aamodt et al., The ALICE Experiment at the CERN LHC, 2008_JINST_3_S08002.

[2] Wyllie K. et al., A pixel readout chip for tracking at ALICE and particle identification at LHCb, Fifth workshop on electronics for LHC Experiment, CERN/LHCC/99-33, 29 October 1999, 93.

[3] Riedler P. et al., Production and Integration of the ALICE Silicon Pixel Detector, Nucl. Instrum. Methods Phys. Res., A 572 (2007) 128-131.

[4] Kluge, A. et al., Nuclear Science Symposium Conference Record, 2005 IEEE, Volume 2, 23-29 Oct. 2005 Page(s):761 - 764, The ALICE silicon pixel detector: electronics system integration.

[5] Faccio et al., Single Event Upset Tests of an 80 Mbit/s Optical Receiver", IEEE Trans. Nucl. Science, Vol.48, No.5, Oct 2001 and RX40 - An 80 Mbit/s Optical Receiver ASIC for the CMS digital optical link, Reference and Technical Manual http://proj-rx40.web.cern.ch/proj%2Drx40/documents/manual_oct02.pdf.

[6] Kluge A., ALICE Silicon Pixel On Detector Pilot System OPS2003 - The missing manual, ALICE internal note, ALICE-INT-2004-030.

[7] Moreira P. et al., A 1.25 Gbit/s Serializer LHC Data and Trigger optical links. Proceedings of the fifth Workshop on Electronics for LHC experiments, 1999 and Moreira, P et al., G-link and Gigabit Ethernet compliant serializer for LHC data transmission, NSS-MIC 2000, Lyon, France , 15 - 20 Oct 2000 - pages 9/6-9.

[8] Powell A.S., Analogue Pilot Testing, LHCb RICH L0 Production Readiness Review, 2004 http://akluge.web.cern.ch/akluge/work/alice/spd/spd_documents/200506powellanalogPilotTesting.pdf.

[9] de Oliveira, R., The development of the fabrication process of low mass circuits, CERN-TS internal note, TS-Note-2005-033.

[10] Pepato A. et al., The mechanics and cooling system of the ALICE silicon pixel detector. Prepared for International Workshop on Semiconductor Pixel Detectors for Particles and Imaging, Bonn, Germany, 5-8 Sep 2005. Published in Nucl. Instrum.Meth.A565:6-12,2006.

[11] Snoeys W. et al., Pixel readout electronics development for the ALICE pixel vertex and LHCb RICH detector, Proceedings of the Pixel 2000 Workshop, Genova, 5-8 June 2000, published in NIM A 465 (2001) 176-189.

[12] Boccardi A. et al., Integration and test of the ALICE SPD readout chain, 10th Workshop on Electronics for LHC and Future Experiments, Boston, MA, USA, 13 - 17 Sep 2004, pp.47-50.

[13] Aglieri Rinella G. et al., The Level 0 Pixel Trigger System for the ALICE experiment: implementation, testing and commissioning, Proceedings of TWEPP 2008.

[14] Aglieri Rinella G., Development and Implementation of the Level 0 Pixel Trigger System for the ALICE experiment, Proceedings of NSS 2007.

[15] Kluge, A., Morel M., Characterization of the SPD low voltage distribution network, to be published as ALICE internal note. http://akluge.web.cern.ch/akluge/work/alice/spd/spd_documents/20070829LVMCM070829.pdf