The VFAT Production Test Platform for the TOTEM Experiment

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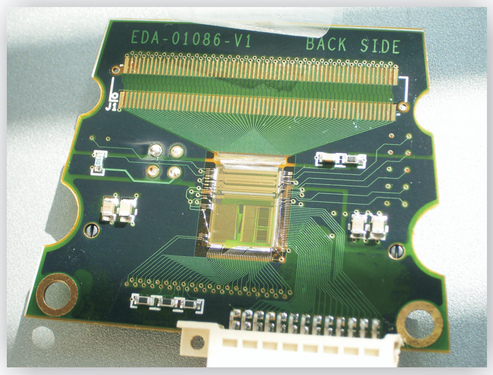
VFAT & VFAT hybrids

For the charge readout of silicon and gas detectors within the TOTEM [1] experiment of the LHC, a front-end ASIC, VFAT, has been designed.The VFAT [2,3] produces both "Trigger" and "Tracking" information.The "Trigger" information, in the form of a programmable fast "OR", can be used for trigger building.The "Tracking" information is in the form of binary "hit" channel data corresponding to a given clock period selected by a first level trigger (LV1A).

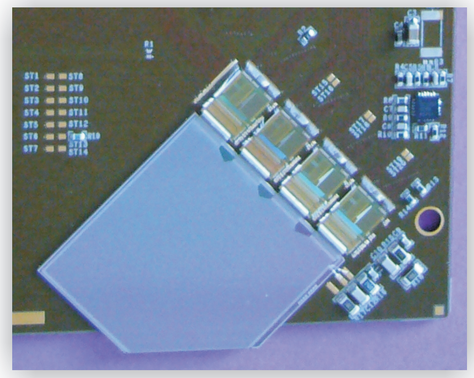
The VFAT has 128 channel inputs. Each channel contains a low noise pre-amplifier and shaper followed by a comparator. Following the comparator are the digital circuits used for generating the "Fast-OR" outputs, data storage and data packet construction.

On receipt of a trigger (occurring after a given latency period), the corresponding binary data is packaged together with time stamps and other information (i.e. ChipID, CRC) into a 192-bit data packet.

Two types of hybrids produced for TOTEM incorporate VFAT chips: The GEM/CSC gas sensor hybrid, containing 1 VFAT chip and the Roman Pot hybrid, containing 4 VFAT chips.



VFAT mounted on a gas sensor hybrid. The chip and bond wires are protected from damage by a protective cap (not shown).



A Roman Pot hybrid containing 4 VFAT chips bonded to an edgeless silicon sensor.

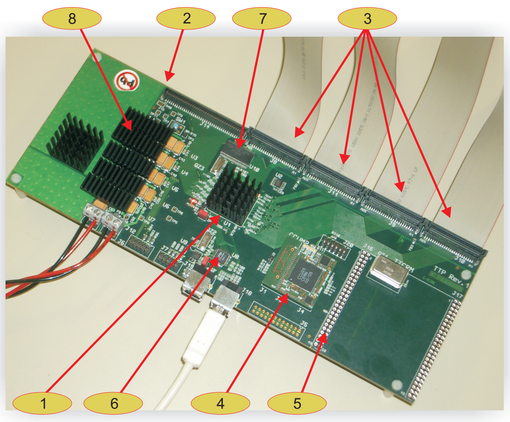
The TOTEM Test Platform (TTP)

The Totem Test Platform (TTP) was conceived to be a "light" front-end Control, Triggering and Readout system for the production test of VFAT together with the hybrid. The goal was to have a compact and portable test bench for VFAT hybrids that can be controlled by USB connection from a laptop.

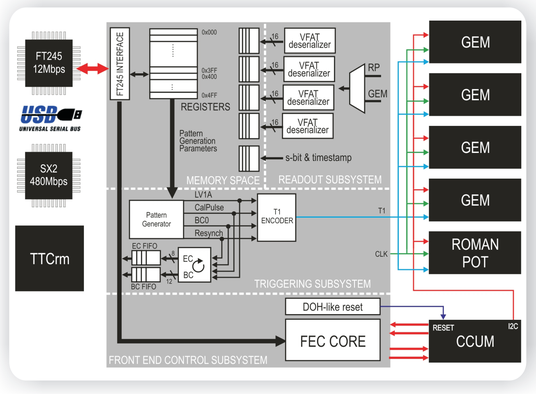
The TTP is a compact (26cm x 10 cm) card, that is based around the following components:

1. An FPGA (EP2C20F484C6N of the Cyclone II [4] FPGA family by Altera Corporation).
2. A Roman Pot hybrid socket.
3. Four GEM/CSC hybrid sockets.
4. A socket for an i2c master hybrid ("CCUM", that hosts a custom rad-hard i2c master ASIC namely CCU25 [5])
5. A socket for a clocking & triggering hybrid ("TTCrm", that hosts a custom rad-hard ASIC namely TTCrx [6])).
6. A USB 2.0 full speed interface (FT245BL [7] by FTDI ltd).
7. A USB 2.0 high-speed interface (CY7C68001-56PVC or "SX2" [8] by Cypress semiconductors).
8. Linear Regulators.

The TTP architecture is largely based on an existing test bench developed for the CMS Preshower [9].



A photograph of the TTP itemizing its main components



Block diagram of the TTP architecture.

The Testing Procedure

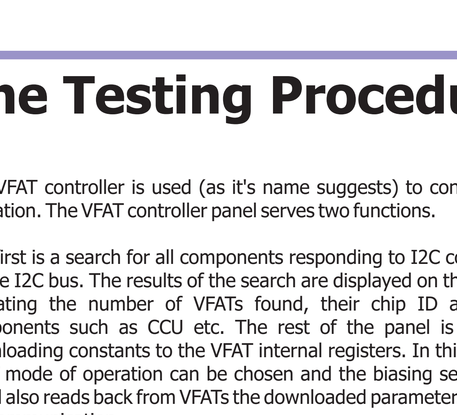
The VFAT controller is used (as it's name suggests) to control VFAT operation. The VFAT controller panel serves two functions.

The first is a search for all components responding to I2C commands on the I2C bus. The results of the search are displayed on the top line indicating the number of VFATs found, their chip ID and other components such as CCU etc. The rest of the panel is used for downloading constants to the VFAT internal registers. In this way the VFAT mode of operation can be chosen and the biasing set-up. The panel also reads back from VFATs the downloaded parameters to verify the communication.

A second VFAT Controller panel is used to command VFAT during manual tests. The third panel is used to select test procedures used in systematic chip testing.

The functions of the different routines available in the VFAT Controller are detailed in the adjacent table.

The results are summarised in a summary file as well as fits and acceptance cuts. These summary files are stored in unique directories created from VFAT IDs and measurement timestamps. For detailed study; the results can be visualised by the analysis software.

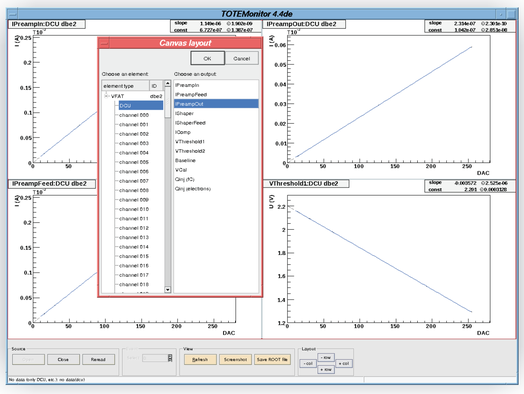


VFAT Controller first panel used for initialisation of VFATs.

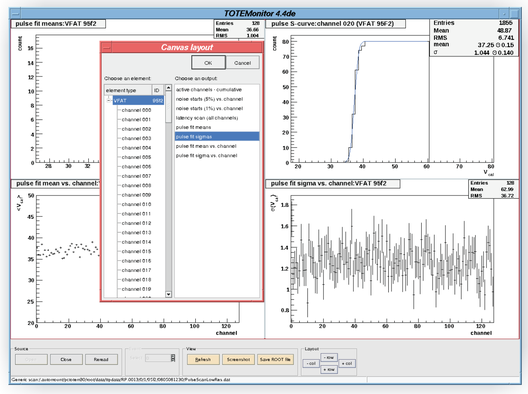
Name	Description
Power measurement	The power consumption is measured automatically for VFATs in "Sleep" and "Run" modes.
I2C Check	Writes and reads to all VFAT internal registers and verifies the consistency of results.
Data packet check	Vigorously applies multiple triggers to VFAT and checks consistency of the data packets with a reference file. This routine checks the memory logic functions such as counters, flags, CRC etc.
Mask check	Each channel is masked and input signals applied to verify "mask" functionality.
DAC scan	Routes the analog output of each DAC in turn to the DCU and scans the 8 bit DAC range. This is an important operation for calibration of the chip.
Pulse Scan	Characterisation of the analog performance such as signal to noise and threshold. A channel is selected and an input charge swept through a fixed threshold providing data for S-curve analysis. Options include polarity of signal charge and High or Low resolution. High Res. instructs VFAT to inject charge to one channel at a time while Low Res. performs the procedure on many channels simultaneously.
Binary Scan	The binary scan is a quick method for identifying excessively noisy (singing) channels or dead channels. For each channel in turn, a constant signal charge is delivered a number of times well above threshold. A channel operating correctly will show the number of hits equal to the number of signal charge pulses (100%). A singing channel will also record hits when no signal charge is applied and hence will record greater than 100% whilst a dead channel 0%.

Below shows the response of DACs following the DAC scan. From these curves a precise knowledge of the analog biases and calibration of charge delivery can be obtained.

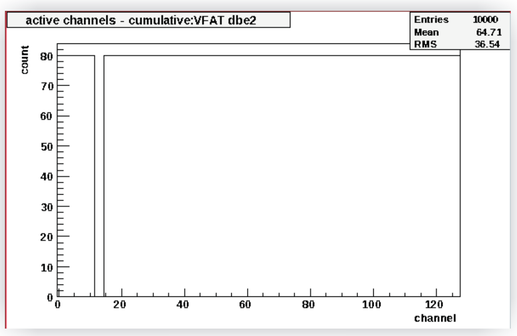
The results of the Pulse Scan can be viewed in the form of S-Curves. An S-Curve (shown in the top right hand plot below) is a histogram of hits on a selected channel as a function of input pulse amplitude. Starting below threshold with 0% of hits and continuing to well beyond threshold (to 100% of hits) an "S" is formed . An error function fit to the curve yields the noise and threshold as the sigma and mean of the fit.

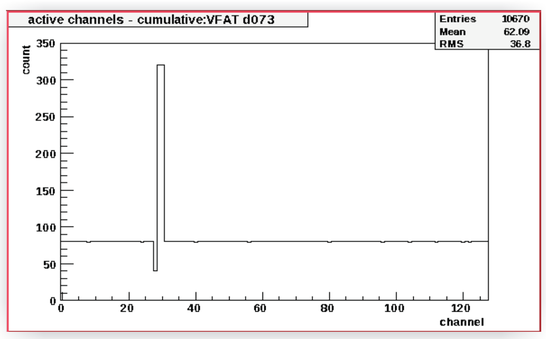


Visualisation of the response of internal VFAT DACs



Analysis showing selection of an individual channel's S-curve (top right) and the noise as a function of channel number (bottom right).





Results from a binary scan. Each of the 128 channels was pulsed 80 times in turn. A healthy channel returns 80 hits. The left hand plot identifies a dead channel (with 0 hits) and the right hand plot identifies a "singing" channel.

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