Novel Sensors With In-Pixel Charge Storage

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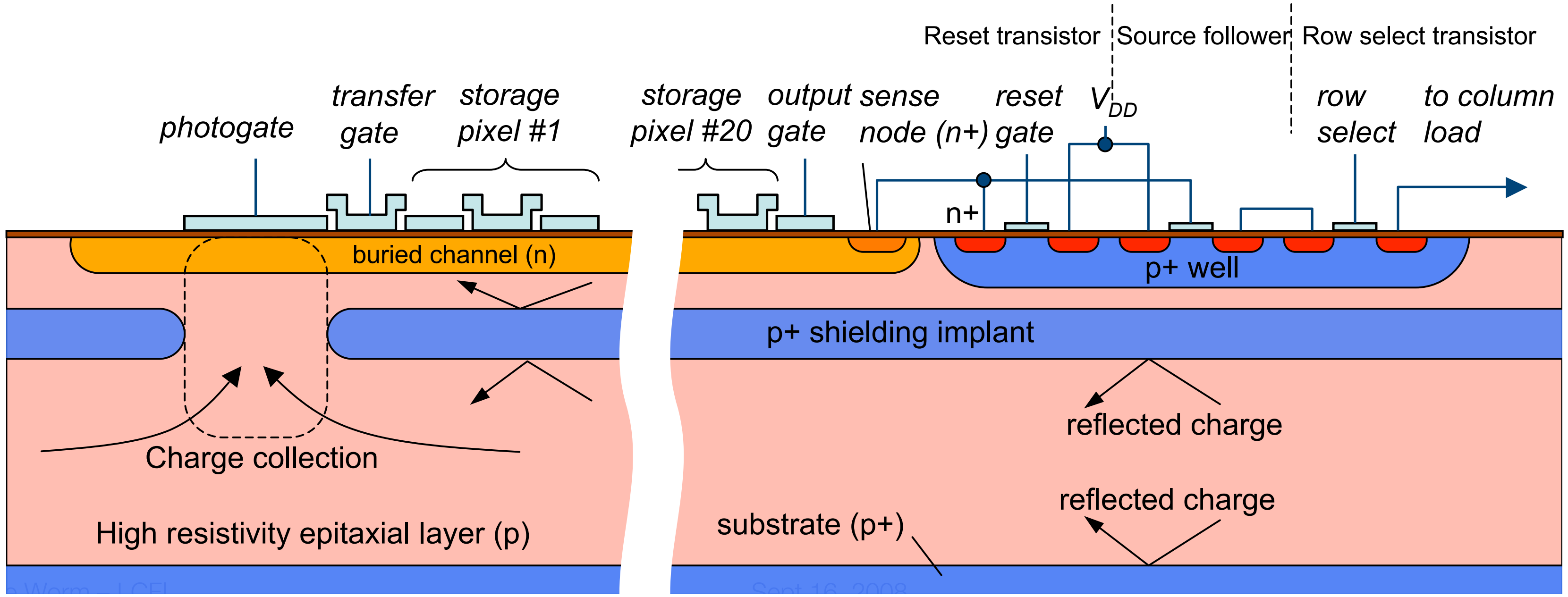
Outline

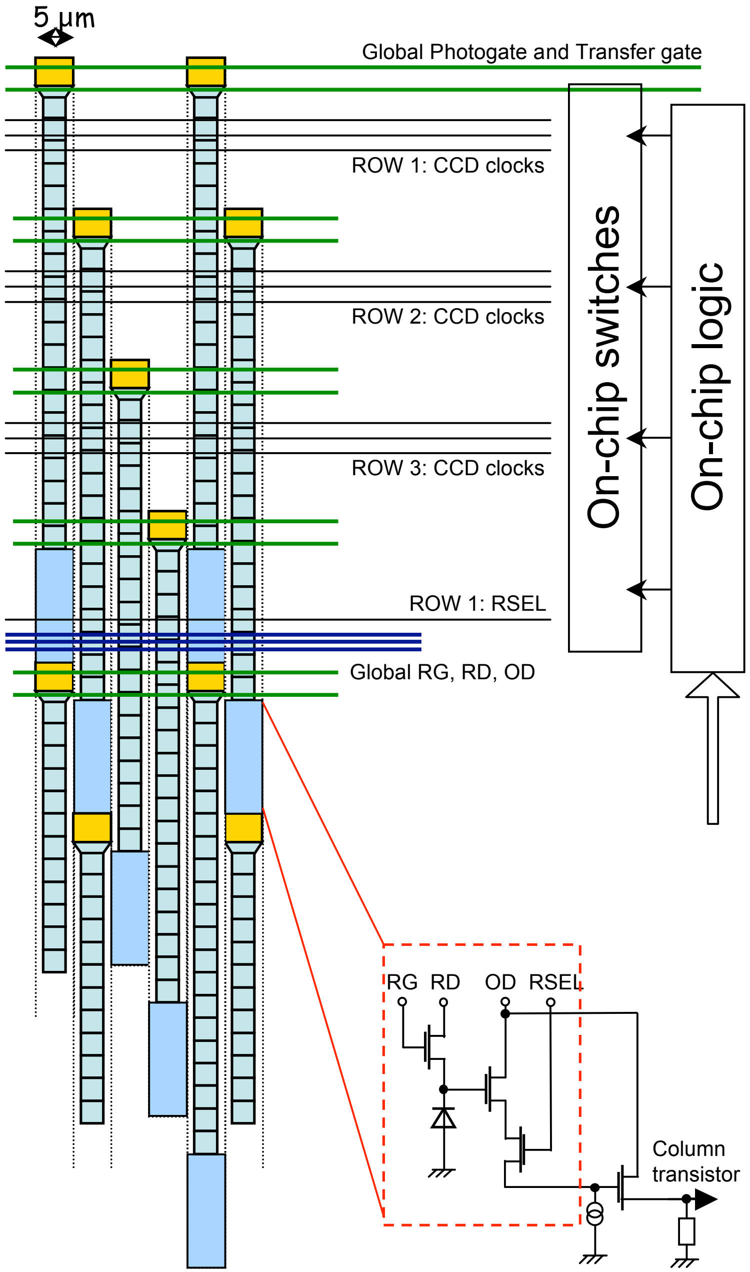
- Introduction to ISIS
- *ISIS1:* Proof of concept
- Characterization and Beam-Test
- *ISIS2:* CMOS+CCD
- Summary

In-Situ Storage Image Sensor

- ISIS Sensor details:
  - CCD-like charge storage cells in MAPS pixel, CMOS or CCD technology
  - p+ shielding implant (or epi) forms reflective barrier
  - Designed for “burst” imaging (*see* Prof. Etoh http://hydraulics.web.infoseek.co.jp)
- Operational Details
  - Charge collected at photogate
  - During active period charge is periodically shifted into short CCD register
  - During readout period charge is moved to output gate and ADC



ISIS Details



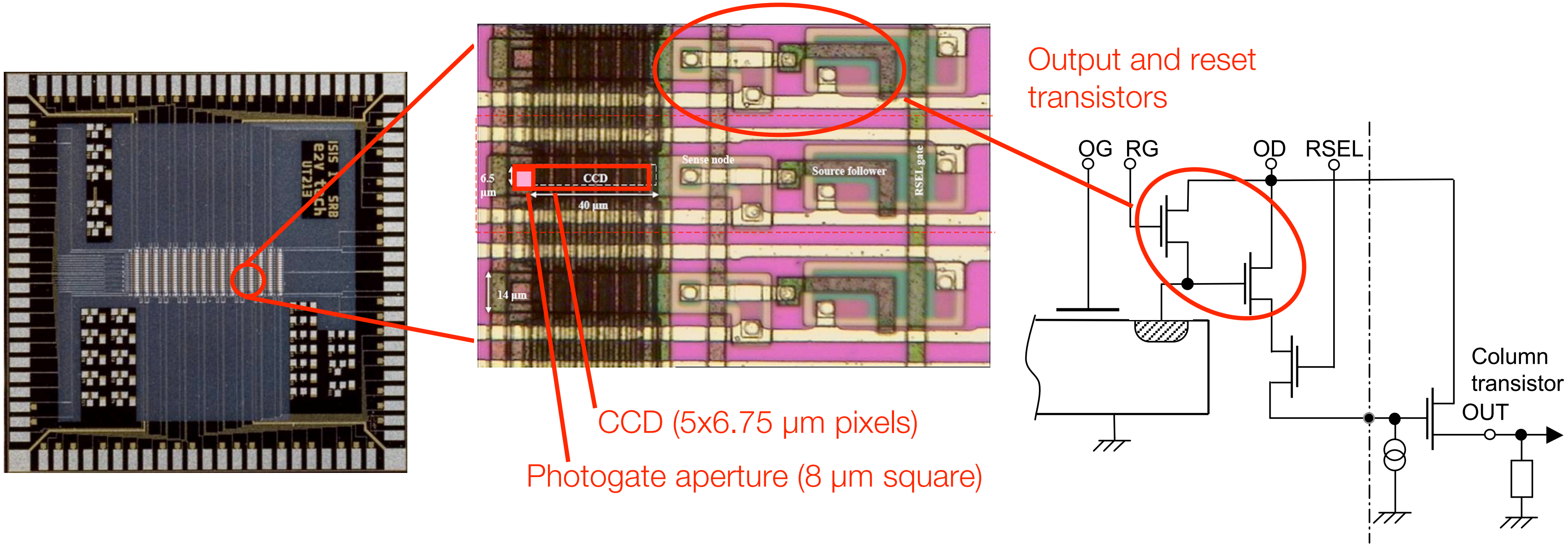
- Implementation:
  - Linear (see left) is easiest layout
  - many other arrangements possible
- Process:
  - Combines CCD and active pixel technologies
  - Deep implant or custom epi needed
  - Good charge transfer needed

ISIS and the ILC

- Developed for Particle Physics with the ILC in mind
  - 2820 bunches separated by 337ns (950 μs train), 5 Hz bunch repetition
  - ~100 hits/mm^2/bunch-train for detector at 15mm from beam
  - Aim for 0.1% X_0 per layer, implies epitaxial thinner than ~50 μm
  - *Need:* ultra-light, low power, low occupancy, burst-mode sensors
- Operational Principles:
  - Charge collected at photogate, transferred to storage pixel during bunch train
  - 20 transfers per 1 ms bunch train
  - Readout during 200 ms quiet period after bunch train
- Advantages:
  - Low frequency clock: easy to drive
  - 20 kHz during capture, 1MHz readout
  - Reduced power consumption
  - Potentially ≈100 times more radiation hard than CCD (fewer charge transfers)
  - Should be less sensitive to beam-induced RF pickup (only shift charge during active periods)

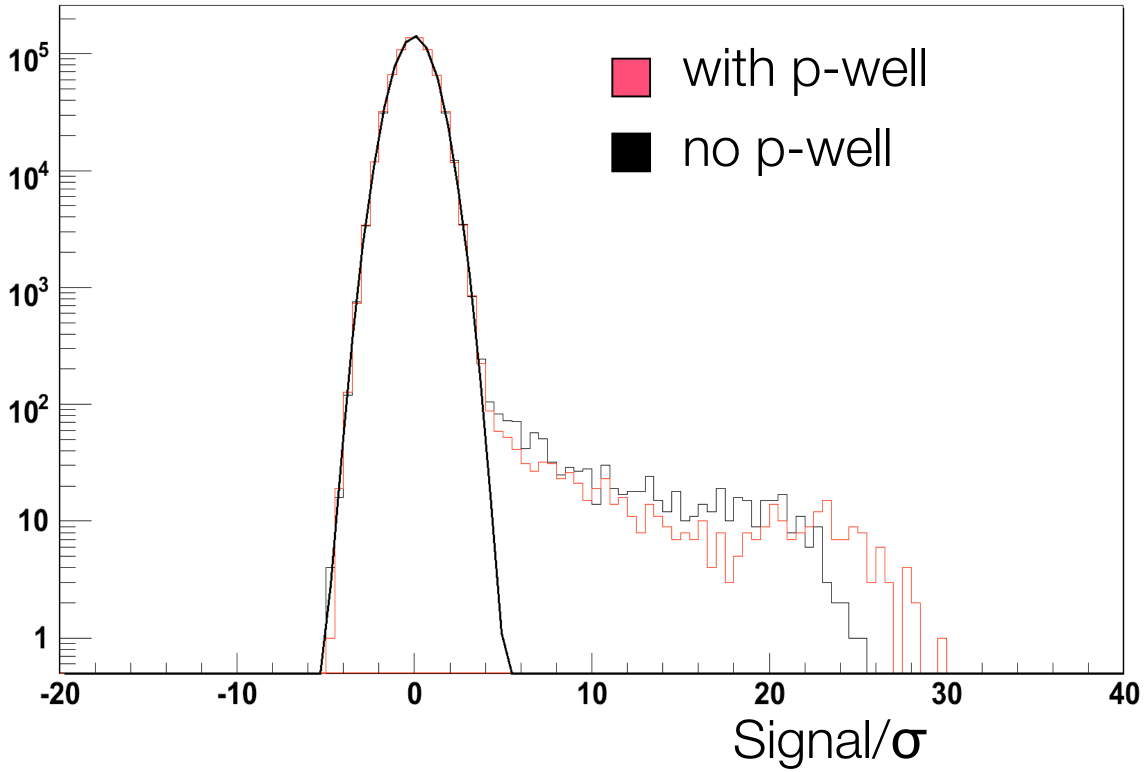
ISIS1: Particle physics “proof of principle”

- Array and Cell details
  - Produced by e2v technologies on 50 µm epi
  - 16 x 16 array of ISIS cells with 5-pixel buried channel CCD register
  - Cell pitch 40 µm x 160 µm, chip size 6.5 mm x 6.5 mm
  - Three-transistor output; no edge logic (CCD process)
  - Variants with/without p-well (no aperture in p-well; punch through)



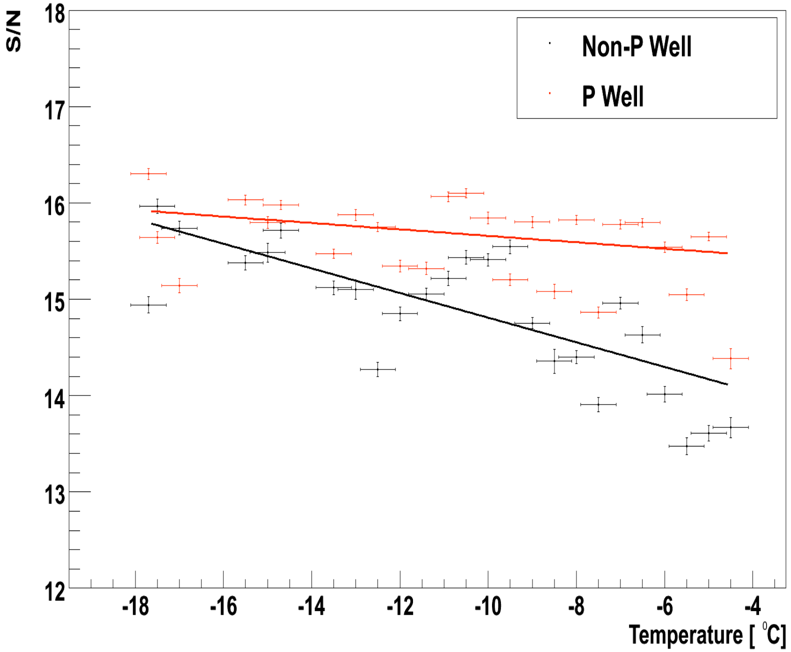
ISIS1: ^{55}Fe Spectrum

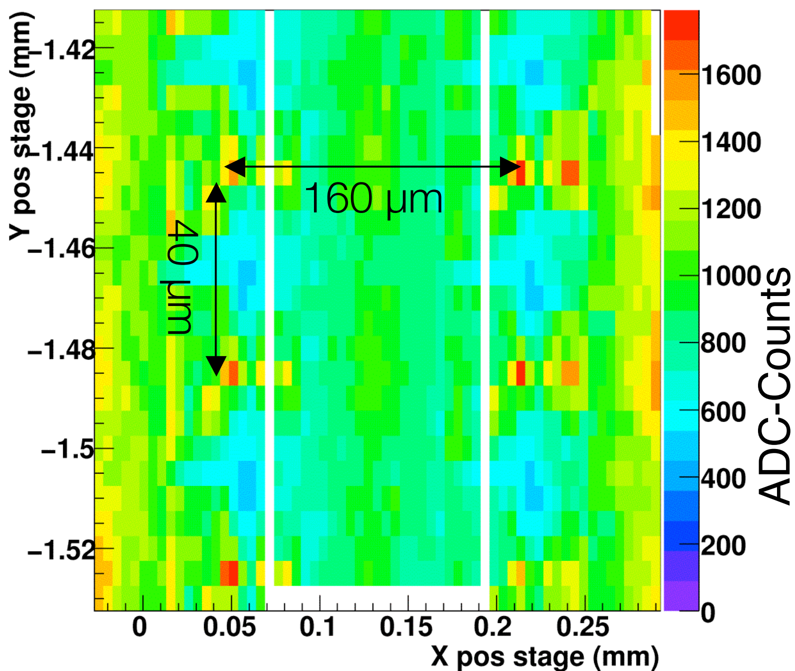
- Signal to Noise ratio, Gain
  - S/N = 16 for 6 keV photons (^{55}Fe) at -20^{o}C
  - ^{55}Fe signal ~1600 e-, Noise ~100 e-
  - Gain: 2.9 μV/e (no p-well), 2.0 μV/e (p-well)
  - Expect MIP signal ~4000 e-



ISIS1: Laser Test results

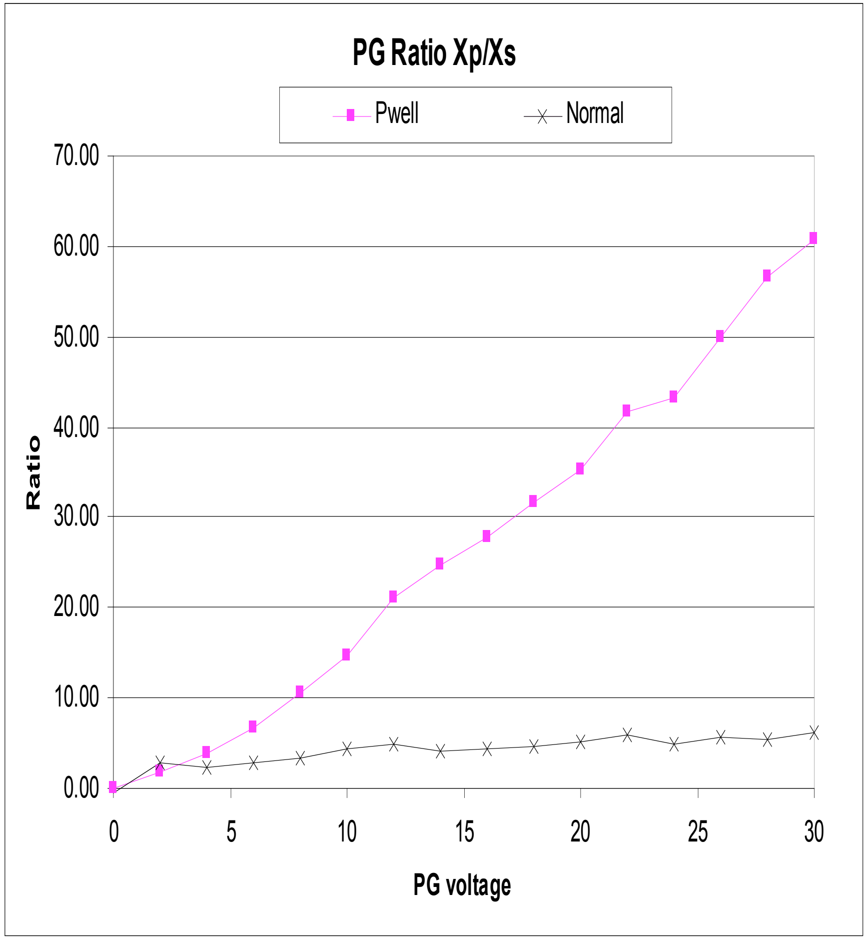
- Signal/Noise vs. Temperature
  - CCD integrates dark current – must not exceed full well capacity
  - Signal/Noise acceptable at low temps, but degrades above -20C
  - ISIS1 needs to be operated at low temperature
- Charge Collection
  - Cluster charge from laser (660 nm), illuminated from above
  - White line an artifact of scan, also large effect from top metalization
  - Results from 1062 nm laser (from below) being processed





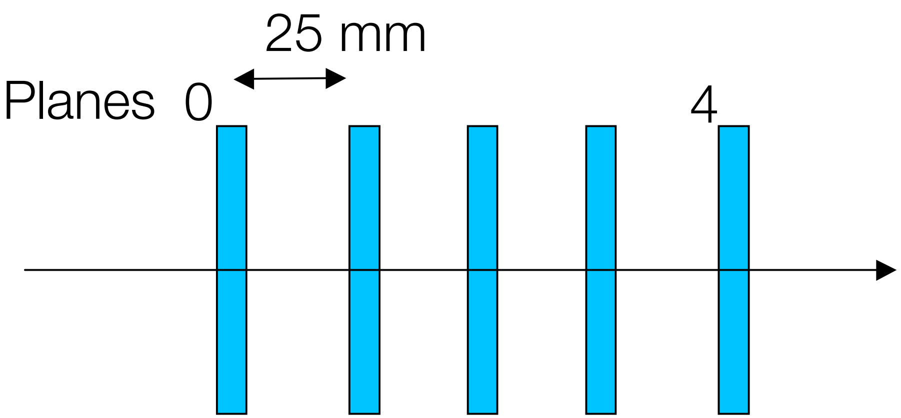
ISIS1: Function of p-well

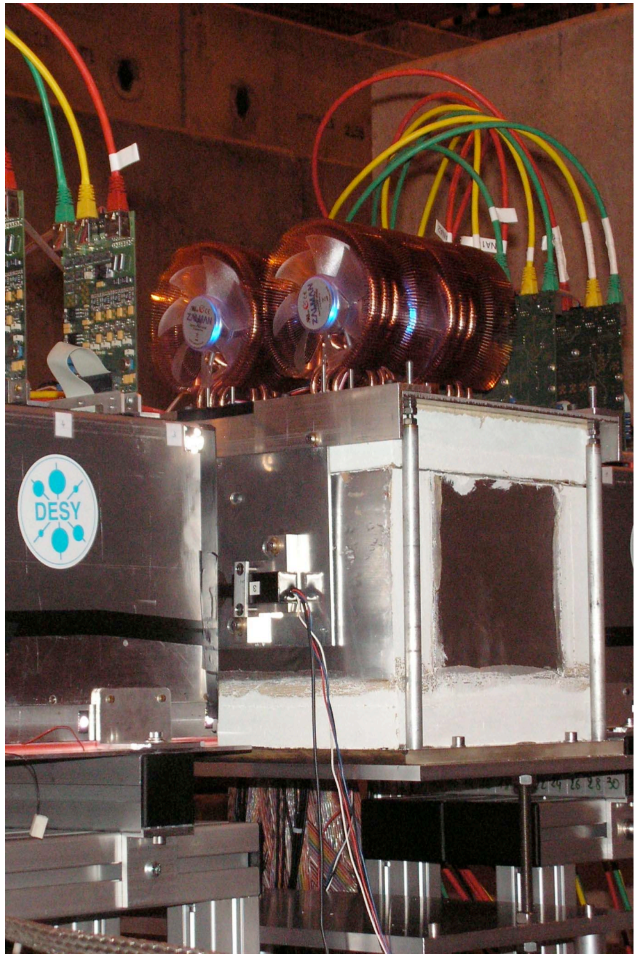
- Check function of p-well
  - Illuminate ISIS1 with ^{55}Fe source
  - Count hits as a function of photogate voltage
  - Must de-convolve hits on photogate, in memory cell, dark current, etc.
- Findings
  - Charge punched through to photogate as expected
  - P-well protects CCD register



ISIS1: Test Beam @ DESY

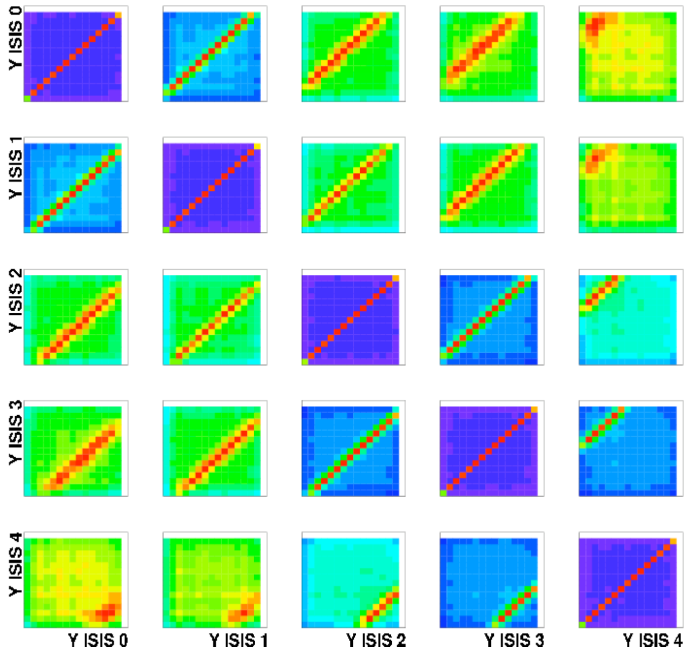
- Telescope Layout
  - Five ISIS1 sensors (non p-well) Illuminated with 6 GeV/c electrons at DESY
  - First four devices aligned very well (used for tracking studies)
- Clustering
  - Find seeds of 5σ above pedestal.
  - Add charge from eight neighbouring pixels (2σ cut)

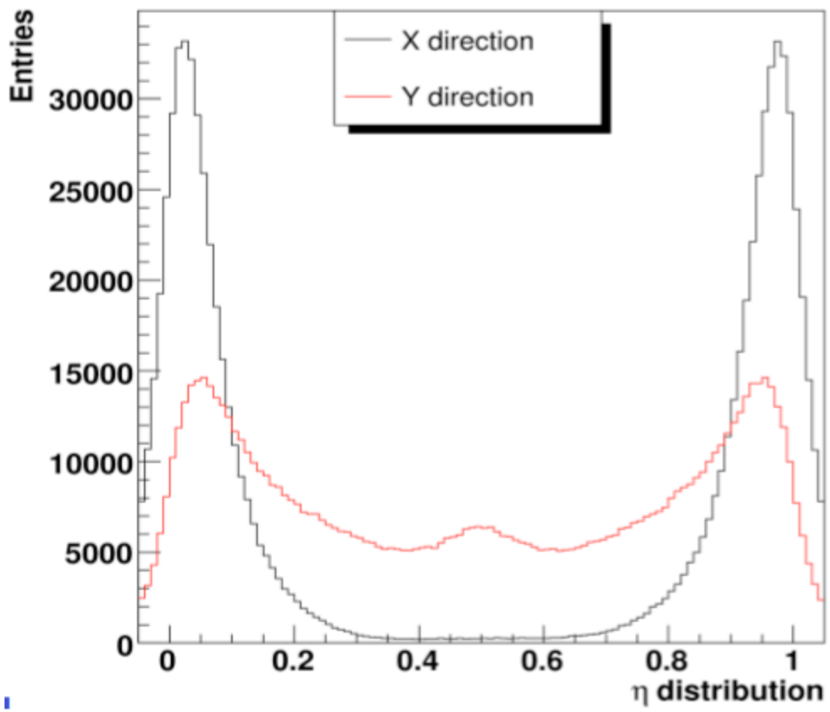




ISIS1 Test Beam: Track Finding/Fitting

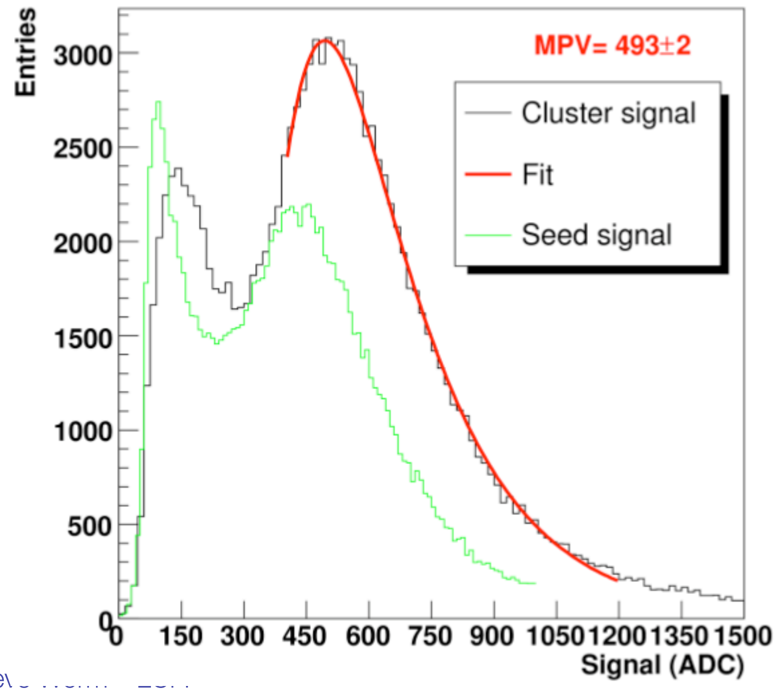
- Correlation of hits vs. plane
  - "y" (pixel short side) direction shown
  - "x" direction similar
  - Good correlation: definitely seeing tracks
- Track fitting routine
  - Form cluster from seed and highest neighbour
  - η distribution = Qright / (Qright+Qleft)
  - η then used to calculate hit position
  - Little charge sharing in "x" (long) direction

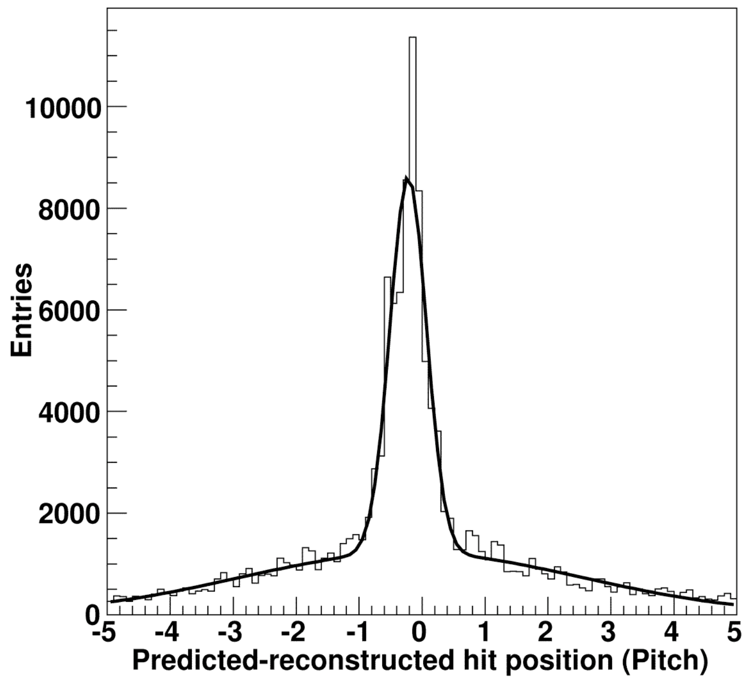




ISIS1 Test Beam: Resolution and Cluster

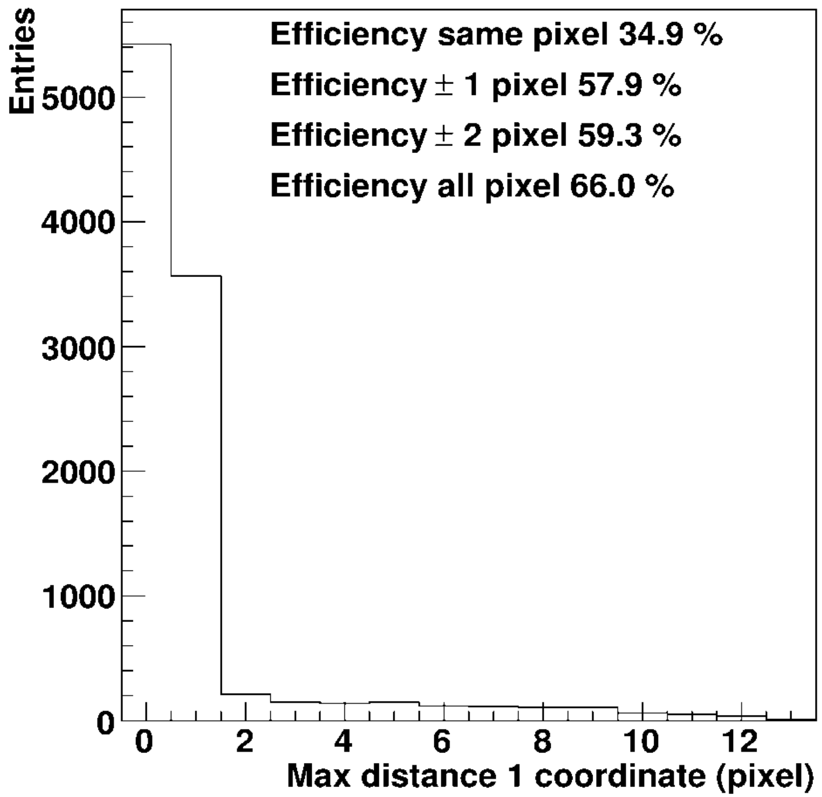
- Cluster Charge
  - Hits clear: most probable = 3.9 ke-
  - Peak structure caused by: noise, charge spreading over many pixels, charge lost to output structures
- Tracking Resolution
  - Using sensors 0,1,3; calculate distance to hit in sensor 2
  - Subtract effect of multiple scattering
  - Corrected resolution in “y” (short pixel direction) = 9.4±0.2 μm.
  - Negligible charge sharing in “x”



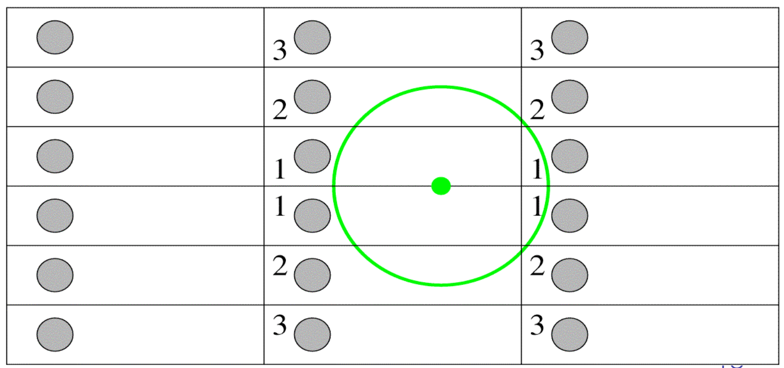


ISIS1 Test Beam: Hit Efficiency

- Hit Efficiency
  - 35% of tracks have a hit in right pixel
  - 59% of tracks have hit within 2 pixels
  - Low efficiency due to 1:4 geometry and charge collection by output structures

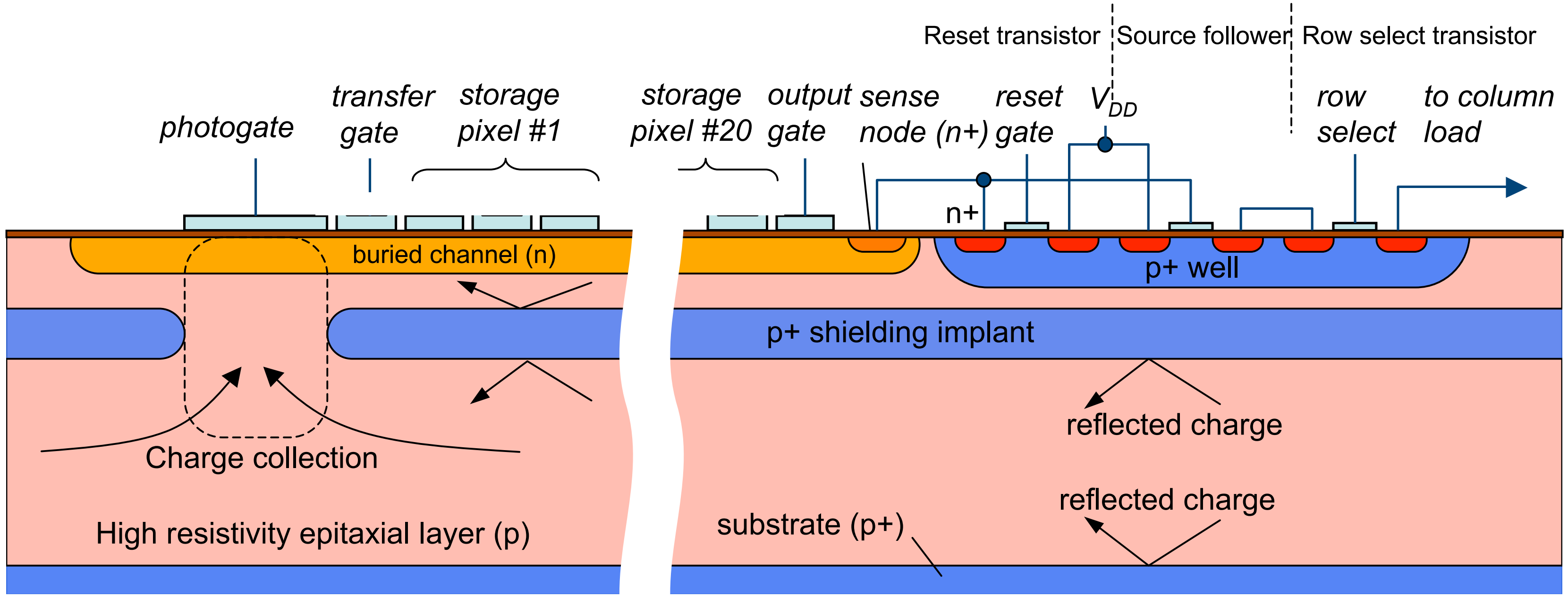


- ISIS1 Geometry
  - 4:1 aspect results in significant charge sharing
  - In worst case: only ~7% of charge collected by highest signal photo-gate: would need SNR of 70 for a MIP to pass 5σ cut



ISIS2

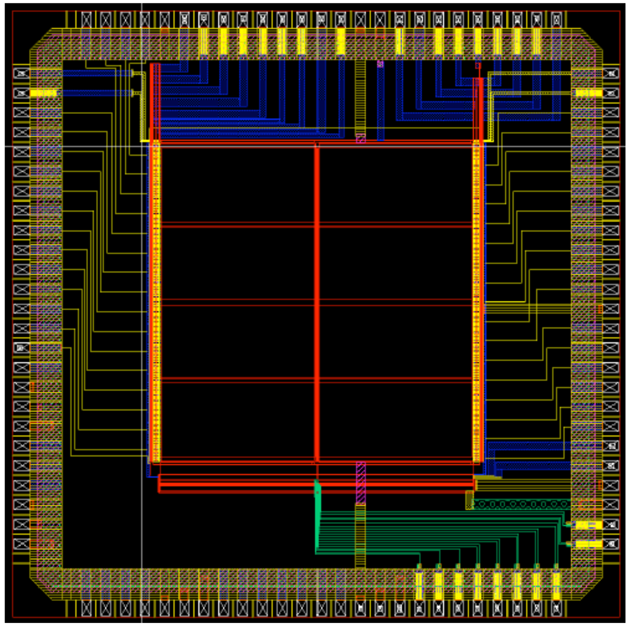
- First CMOS-based ISIS design
  - Made by Jazz Semiconductor; May submission, August finish
  - Using modified 0.18 μm process, ≥100 Ωcm epi
- Important process features:
  - Dual-gate processes (1.8V/5V)
  - Two new implants: CCD buried channel implant and the deep p+
  - Single, non-overlapping poly for transfer (very small gap)

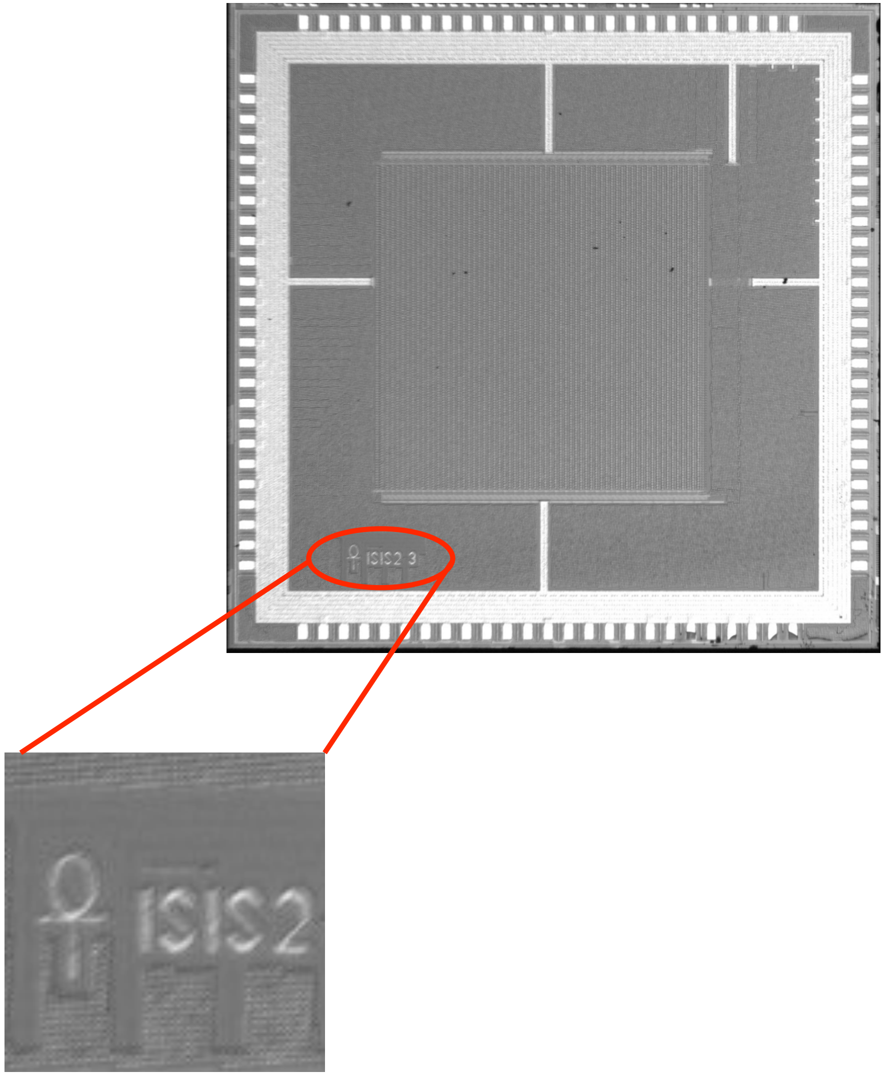


ISIS2: Details

- ISIS2 layout details
  - 80 μm x 10 μm pixel, staggered: 20 μm x 40 μm effective geometry
  - 20 CCD storage cells in each pixel, analogue readout possible
  - Area of 1 cm^2 (four 5x5 mm^2 tiles) in MPW
  - Buried channel for CCD 5 μm wide (could have been narrower)
  - Only 3 metal layers used
  - CCD gates: doped polysilicon, no overlaps
- Moderate-sized devices made, with many variants
  - No deep-p implant variant
  - Varied buried channel implant profiles (dose, energy)
  - Apertures such as p-well opening varied openings to test sensitivity
  - Layout features, geometries largely the same

ISIS2: Pictures





Summary

- *ISIS1:* Image Sensor with In-situ Storage demonstrator
  - Successfully tested "Proof of Principle" for particle physics
  - Self contained telescope used for tracking, proof of deep-p
  - Next: CERN testbeam (120 GeV/c π) and laser scan (660/1062 nm)
- *ISIS2:* implemented in CMOS, testing later this month
  - Back from dicing; test structures off for SIMS
  - Many interesting variants to test (especially buried channel and apertures near photogate)
  - Implementation of CCD in mostly-standard CMOS
- *ISIS3:* expect some indication of funding in coming weeks

Exciting developments… now in CMOS and ready to test!

Thanks

LCFI and UK's *PPARC/STFC* for funding

DESY for providing test-beam

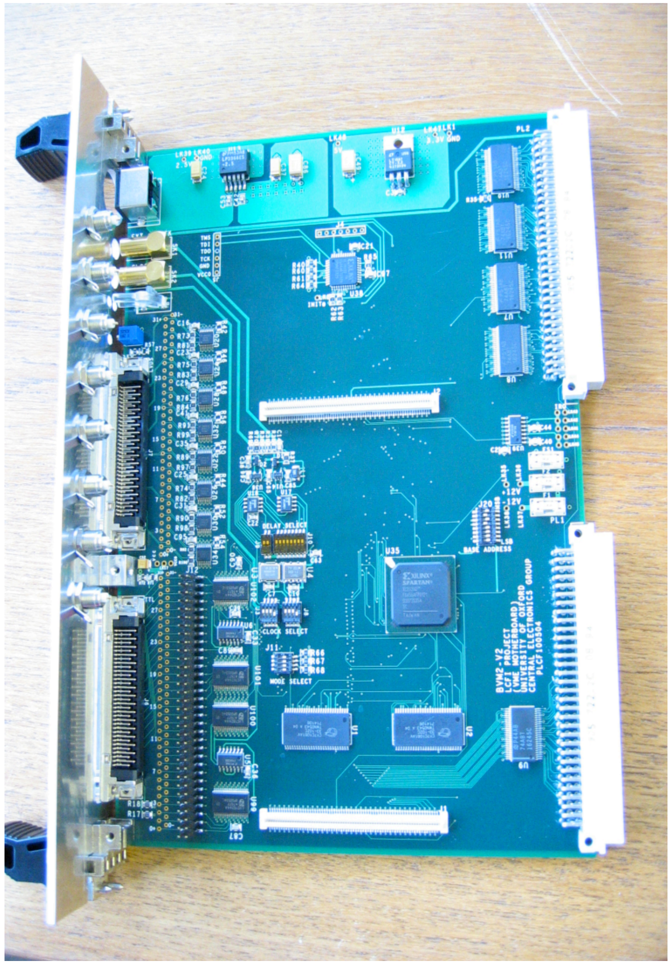
EUDET (EU FP7 program) for providing assistance at DESY test-beam and travel support

Arjun Karroy at Jazz Semiconductor for ISIS2 picture

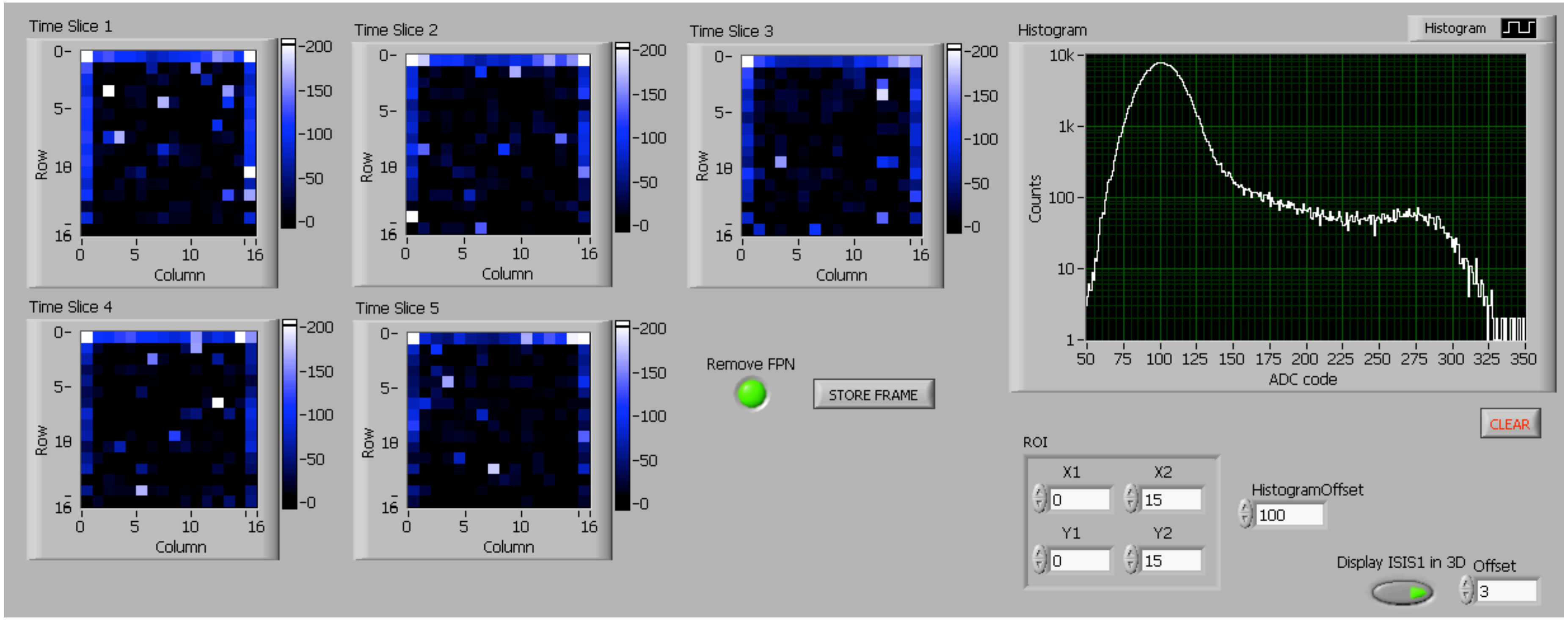
Dave Cussans for many ISIS1 testbeam slides!

ISIS1: Readout and DAQ

- DAQ Features
  - Correlated double sampling
  - Sixteen analogue outputs multiplexed onto four CAEN 14bit V1724 ADCs
  - VME based system using Labview to control
  - Control signals driven by custom sequencer - BVM2



Initial tests of ISIS1 (^{55}Fe)



- Tests with ^{55}Fe source
  - Top row and two side columns are not protected; collect diffusing charge
  - The bottom row is protected by the output circuitry
  - ISIS1 with and without p-well both work OK
  - New ISIS1 chips with p-well have been received, now under test