# Design and Characterisation of a Fast Architecture Providing Zero Suppressed Digital Output Integrated in a High Resolution CMOS Pixel Sensor for the STAR Vertex Detector and the EUDET Beam Telescope

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*Abstract*

CMOS Monolithic Active Pixel Sensors (MAPS) have demonstrated their strong potential for tracking devices, particularly for flavour tagging. They are foreseen to equip several vertex detectors and beam telescopes. Most applications require high read-out speed, imposing sensors to feature digital output with integrated zero suppression. The most recent development of MAPS at IPHC and IRFU addressing this issue will be reviewed. An architecture will be presented, combining a pixel array, column-level discriminators and zero suppression circuits. Each pixel features a preamplifier and a correlated double sampling (CDS) micro-circuit reducing the temporal and fixed pattern noises. The sensor is fully programmable and can be monitored. It will equip experimental apparatus starting data taking in 2009/2010.

## I. Introduction

Subatomic physics experiments express a growing need for very high performance flavour tagging, with emphasis on short lived particles (e.g. charmed mesons) through their decay vertex. This calls for an excellent vertexing and tracking system in order to reconstruct the secondary vertices and to measure precisely the momenta of tracks. This translates into the need to improve the system's accuracy by typically an order of magnitude with respect to the existing state of the art.

The existing pixel technologies are not adequate for this new challenging requirement level, associated to a highly granular, ultra-light, radiation tolerant, fast and poly-layer vertex detector installed very close to the beam interaction point. CMOS MAPS provide an attractive trade-off between granularity, material budget, readout speed, radiation tolerance and power dissipation, which may suit the ambitioned vertexing performances.

MAPS are developed since several years for this goal. One of their most specific aspects is that the sensitive volume and the front-end read-out electronics are integrated on the same substrate. The charges generated by an impinging particle in the, typically 5 to 15 µm thin, epitaxial layer underneath the readout electronics are collected through thermal diffusion by regularly implanted N-well/P-epi diodes. These charges are then converted, "in situ", to voltage signal at the capacitance of the sensing diode. The signal can then be treated by the integrated readout electronics. Being fabricated in standard CMOS processes available through many commercial microelectronics foundries, they are attractive for their cost effectiveness and the fast multi-project run turn-over.

MAPS tracking performances are now well established [1]. Thanks to their particularly low equivalent noise charge (ENC), the most probable value (MPV) of the signal-to-noise ratio (S/N) ranges from 15 to 30, depending on the pixel size (Fig. 1a). A detection efficiency exceeding 99.5% was demonstrated, even in the case of a pitch as large as 40 µm, at an operation temperature of up to 40 °C (Fig. 1b). The single point resolution was measured from ~1 µm for a 10 µm pixel pitch up to ~3 µm for a 40 µm pitch, for sensors with analogue readout.

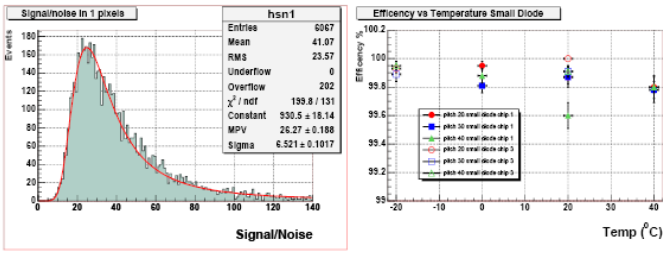


Figure 1: Pixels analogue readout performance

Although analogue readout MAPS show excellent performances, they suffer from moderate readout speed in case of a large amount of pixel information transfer need. Numerous application domains require simultaneously high granularity and fast read-out speed. Integrating signal processing functionalities inside the sensor, such as CDS, ADC (Analogue to Digital Converter), data zero suppression circuitry are then facing severe constraints from the pixel dimensions, readout speed and power consumption. A prototype sensor Mimosa16 [2], with 24 integrated column-level discriminators, had been realised to check detection performances for sensors with digital readout. Figure 2 shows the detection efficiency, the single point resolution and the average fake rate as a function of the discriminator threshold. The detection efficiency is nearly 100 % up to a threshold

value of 6 mV, corresponding to ~6 times the noise standard deviation, with a fake rate below $10^{-5}$ and a spatial resolution better than 5 µm. The latter is better than a pure digital resolution (pixel pitch of 25 µm) thanks to charge sharing among pixels in a cluster due to thermal diffusion.

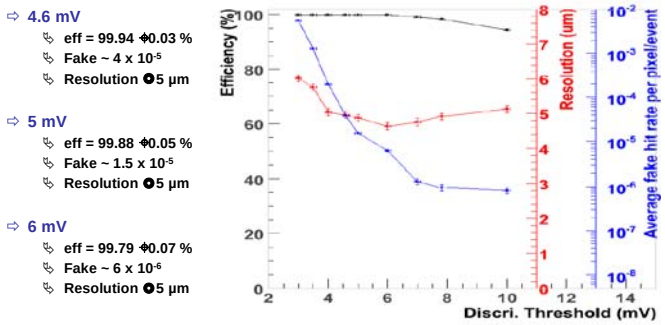


Figure 2: Mimosa16: Pixel digital readout performance

These results lead to confirm the choice of a new CMOS MAPS architecture combining, on the same substrate, a pixel array occupying an active area of reticle size, column-level discriminators for analogue-to-digital conversion and a zero suppression circuit for data sparsification.

MAPS are foreseen for several applications, ranging from subatomic physics experiments up to bio-medical imaging devices. Their first use inside a vertex detector coincides with the upgrade of the STAR experiment at RHIC. MAPS also equip the beam telescope of an EU project, called EUDET, underlying the R&D for the ILC (International Linear Collider) vertex detector.

In the first part of the paper, the applications both for the STAR vertex detector upgrade and the EUDET beam telescope will be presented with their technical requirements. In the second part, the architecture of MAPS optimised for these applications, developed by the IPHC-Strasbourg and IRFU-Saclay collaboration, will be discussed in detail.

## II. Examples of MAPS Applications

### A. *STAR Heavy Flavor Tracker (HFT) upgrade*

The STAR upgrade is designed to allow for direct topological reconstruction of D (and B) mesons through the identification of decay vertices displaced from the primary interaction vertex by 100-150 µm [3]. In order to achieve a vertex pointing resolution of about, or better than, 30 µm, two nearly cylindrical MAPS layers with averaged radii of about 2.5 and 8 cm, will be inserted in the existing detector (Fig.3). No space will be available for a sophisticated cooling system. Only simple air flow can be used, meaning that MAPS sensors have to be operated at room temperature. The power consumption of MAPS should therefore be in the order of 100 mW/cm$^2$. Moreover, multiple coulomb scattering concerns impose to keep the material budget per layer as low as ~ 0.3% of radiation length. All sensors should therefore be thinned down to 50 µm. The final pixel sensors, expected to be operated with Au + Au collisions at a RHIC II luminosity of ~ 8 x $10^{27}$ cm$^{-2}$s$^{-1}$, will face a hit density in the order of $10^6$ hits/s/cm$^2$ in the inner layer. The total ionising dose was estimated to 150 - 300 kRad per year and the non-ionising radiation dose should mainly come from an annual flux of 3–12 x $10^{12}$ charged pions per cm$^2$ traversing the inner layer [4].

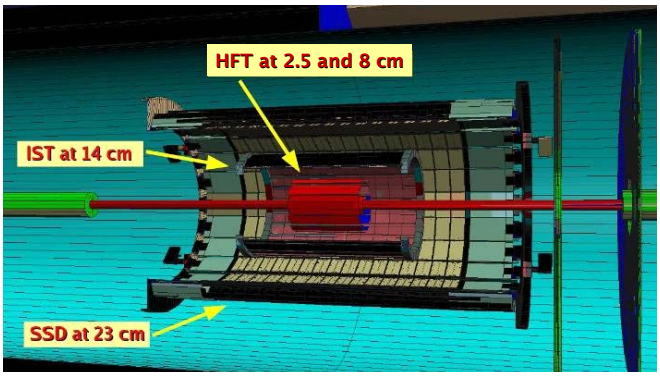


Figure 3: STAR upgrade

The HFT vertex development is a three step process. The first step was achieved by operating successfully a MAPS telescope prototype in the STAR environment during the 2007 Au + Au RHIC run [5]. The telescope consists of three planes, each made of a MimoSTAR2 chip [6]. Each chip provides a 128 x 128 pixel array with 30 µm x 30 µm pixels. With its serial analogue outputs, MimoSTAR2 was a first generation sensor. The second step, foreseen in 2009, consists in equipping three sectors (~30 % of the surface) of the HFT with second generation MAPS, named “Phase1”. They feature a 640 x 640 pixel array with 30 µm pitch. This sensor, ready for fabrication, contains on-chip CDS and column level discriminators. The readout is in rolling shutter mode with an integration time of 640 µs. Finally in 2010, the whole HFT vertex detector will be equipped with still faster and more granular sensors, named “Ultimate”. They will contain all attributes of Phase1 sensors, complemented with a faster rolling shutter clock which allows decreasing the integration time to 200 µs. An integrated zero suppression circuitry will be implemented in the sensor. The Ultimate chip will have a 1152 x 1024 pixel array with 18.4 µm x 18.4 µm pixels.

### B. *EUDET telescope*

The aim of EUDET is to provide to the scientific community an infrastructure exploiting R&D on the different detectors for the future international linear collider (ILC). It covers three main activities relating to vertexing, tracking and calorimetry R&D, together with networking activities supporting information exchange. The vertexing activity aims to construct a CMOS pixel beam telescope with six planes of sensors to be operated at the DESY electron test beam facility. The beam telescope, providing an extrapolated resolution better than 2 µm, is to be used for a wide range of R&D applications and quite different devices under test (DUT), from small (a few millimetres) to large (up to one meter) size.

In order to minimise the risk, the construction of the telescope was organised in two stages. In the first stage, a demonstrator telescope (Fig. 4), exploiting the existing CMOS MAPS sensors with analogue readout, has been realised. It is successfully operated since 2007 [7]. In 2009, the final telescope will be equipped with sensors providing an active surface 4 times larger and a readout speed (~100 µs) about an order magnitude faster than the previous one. The sensors will have a 1152 x 576 pixel array with 18.4 µm pitch, and will be

equipped with integrated CDS, fully digital fast readout and integrated data zero suppression circuitry. Their architecture will be extended to the Ultimate sensor for STAR.

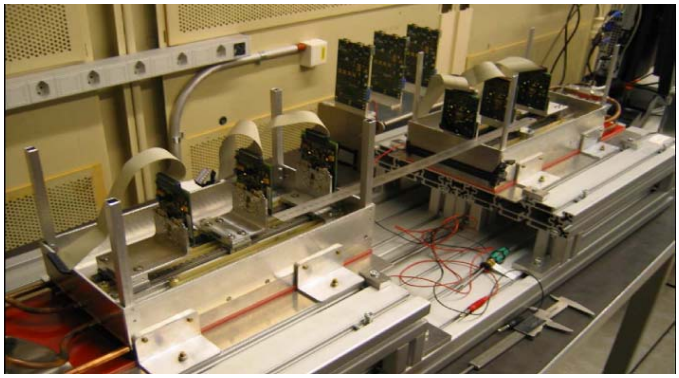

Figure 4: EUDET demonstrator telescope

## III. Fast Readout Architecture

The development of this architecture is based on two separate prototyping lines: one addressing the upstream part of the signal detection and processing chain, and one devoted to data sparsification and formatting. Two prototype circuits, Mimosa22 and SUZE, were fabricated in the AMS CMOS 0.35µm technology, addressing these two research lines. The sensor exploring the signal sensing and analogue processing features 128 columns of 576 pixels ended with a discriminator. Each pixel (18.4 µm x 18.4 µm) contains a pre-amplifier and a CDS circuitry. The sparsification chip incorporates the zero suppression logic and the output memories needed for the EUDET beam telescope and the STAR vertex detector upgrade. In the proposed architecture, the pixel array is read out in rolling shutter mode, the row being selected sequentially by a shift register. The design is organised according to three main issues:

- Increasing the S/N at pixel-level
- Analogue to digital conversion at column end level
- Zero suppression at chip edge level

### *A. Pixels*

Pixel-level amplification and CDS are necessary to increase the S/N in order to perform column-level digitisation. The CDS suppresses low frequency noise, including reset and fixed pattern noise (FPN). The difficulty of in-pixel signal processing is that only NMOS transistors can be used, since any additional N-well used to host PMOS transistors would compete for charge collection with the sensing N-well diodes.

The pixel architecture is illustrated in figure 5. A preamplifier stage is implemented nearby the sensing diode. It is active only when the row is selected to be read, which reduces significantly the power consumption. A serially connected capacitor, using a MOSCAP, and a clamping switch are used for the double sampling. A source follower and a row select switch are employed to output the signal. For such a large pixel array (~2 x 2 $cm^2$), an additional group switch is implemented in the design. In each column, groups of 16 pixels have a single connection to the common data bus to reduce the column line capacitance. RD and CALIB are column-level commands and are used to memorise the output signal level and the reference level of the pixel output stage respectively. This second double sampling operation reduces the pixel to pixel dispersion. The timing diagram of 16 clock cycles up to 100 MHz and more details on CDS operation can be found in [8].

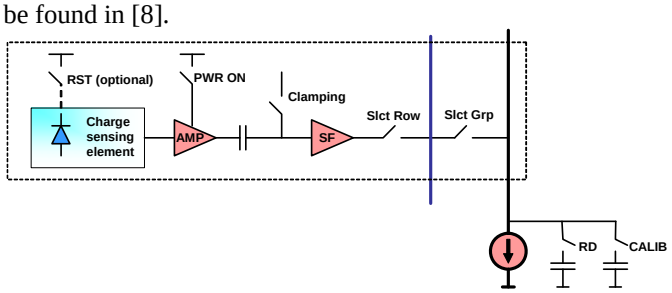


Figure 5: Pixel topology

Figure 6 represents the in-pixel amplifier design evolution, which has the following objectives:

- to reach maximal S/N for a given N-well sensing diode size;
- to minimise the power consumption;
- to squeeze the pixel to pixel dispersion.

Figure 6(a) shows a standard common source (CS) amplifier. The gain performance is improved by implementing an additional transistor M4 for biasing the load transistor M3, as shown in figure 6(b). The AC gain of this structure has been increased, but the DC operating point and the DC gain are almost unchanged, which makes the circuit more resistant to process variation. A still more robust pixel is shown in Fig. 6(c), where a negative low frequency feedback was introduced to decrease amplification gain variations due to process variations. In addition, the feedback ensures biasing of the self biased diodes [9].

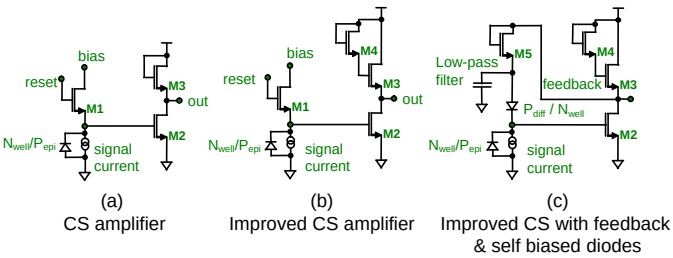


Figure 6: Pixel amplification

The three pixel variants been implemented in the prototype chip Mimosa22, and tested with an $^{55}Fe$ source (5.9 keV X-ray) at 20 °C. The power consumption per pixel, in the activated row to be read out, is about 200 µW. Table 1 illustrates the measured performances. Figure 7 shows the measured temporal noise and FPN of the three pixels as a function of the ionising radiation dose to which the sensor was exposed. The feedback self biased structure (Fig. 6(c)) exhibits the best behaviour, with the smallest temporal noise increase and a FPN remaining essentially unchanged.

Table 1: Performances of the measured Mimosa22 sensor

| Pixel types | Diode size ($\mu m^2$) | CVF* ($\mu V/e^-$) | ENC ($e^-$) |
|---|---|---|---|
| CS (a) | 15.21 | 57.3 | 13.3 ⌖0.1 |
| Improved CS (b) | 15.21 | 57.3 | 13.0 ⌖0.1 |
| Feedback & self biased (c) | 14.62 | 55.8 | 12.3 ⌖0.1 |

* CVF: Charge- to-Voltage conversion Factor

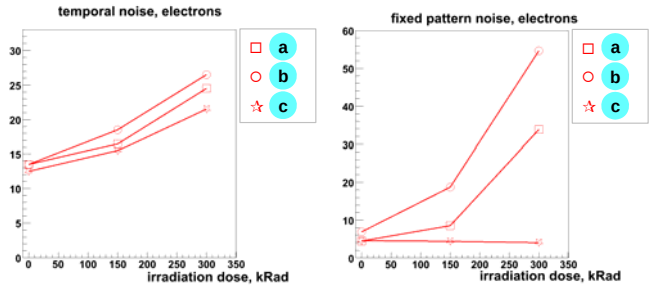


Figure 7: Temporal noise & FPN of Mimosa22 as a function of irradiation dose (10 keV X-Ray)

Increasing the inherent tolerance against ionising radiation damages belongs to the main pixel design goals. At the pixel circuit level, the transistor serially connected to the sensing diode should be an enclosed layout transistor (ELT) surrounded by a guard ring to minimise the drain-source leakage current. As far as the sensing diode is concerned, the thick oxide surrounding it by default needs to be removed by introducing a pseudo-gate ring. The performance of this radiation tolerant diode design has already been reported in [10]. One should note that the results presented both in table 1 and Fig. 7 use amplifiers coupled to radiation tolerant N-well diodes.

The effect of the damage of non ionising radiation can be alleviated by decreasing the pixel pitch and the integration time and by enlarging the sensing diode area [11]. This favours, in this design, a pixel pitch below 20 µm.

## B. *Analogue to Digital Conversion*

Column-level ADCs will be implemented below the pixel array. According to the rolling shutter readout mode, pixel signals (1152) of the selected row are transmitted to the bottom of the pixel array. The 1152 ADCs have to convert those signals to digital data at the row readout speed. Thus a high speed ADC with low power consumption and small layout size is required. The choice of the number of bits depends on the required spatial resolution and on the pixel size. The requirement on the spatial resolution of a single plane sensor, for the EUDET beam telescope, is about 5 µm. It is even less critical (< 10 µm) for the STAR application. In this case, the best solution is to choose a 1 bit ADC: a discriminator, for its lower power consumption and simplicity. All column-level discriminators (1152) use a common threshold value for comparisons. It will be adjustable and set to its optimal value (~5-6 times the noise standard deviation) to ensure ~100% of detection efficiency and low fake rate (~$10^{-4}$).

The column-level discriminator design has been shown in detail in [8]. Considering the small value of the analogue signal, it is mandatory to use an offset compensated amplifying stage (Fig. 8) which corrects the residual offset of the discriminator. The power consumption per discriminator is below 250 µW.

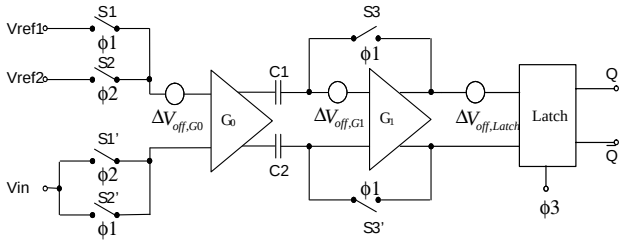


Figure 8: Architecture of the column-level discriminator

The 128 column-level discriminators implemented in Mimosa22 were evaluated by scanning the common threshold voltage. The "S" curves were fitted with an error function to extract the offset, temporal noise and FPN.

Figure 9 shows the discriminator's "S" curve. The extracted temporal noise and FPN are 0.3 and 0.2 mV respectively.

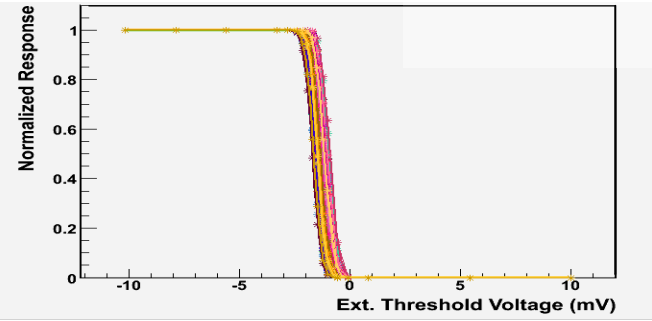


Figure 9: Discriminator "S" curves of the measured Mimosa22

Figure 10 displays the noise performances of the pixel array associated with discriminators. It is shown that the temporal noise comes mainly from the pixel array and column-level discriminators contribute mainly to the FPN.

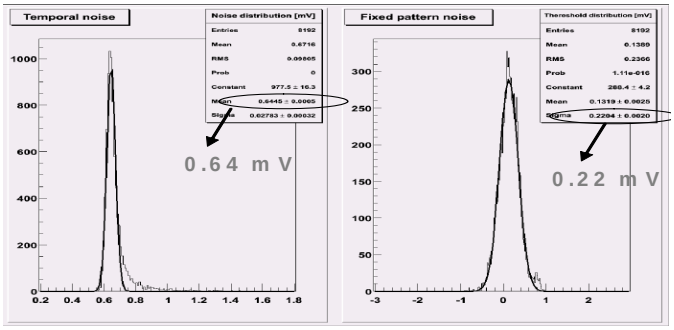


Figure 10: Pixel & Discriminator noise of the measured Mimosa22

Mimosa22 was tested with ~120 GeV pion beam at CERN-SPS. The preliminary results show that the detection efficiency is better than 99.5 % for a threshold value corresponding to about 6.5 times the noise standard deviation. The spatial resolution is better than 4 µm while the fake rate is below $10^{-4}$.

## C. *Zero suppression*

The raw data flow of MAPS for STAR and EUDET may reach up to several Gbits/s per chip. The zero suppression circuitry is based on row by row sparse data scan readout and is organised in pipeline mode in 3 stages. This allows a data compression factor ranging from 10 up to 1000, depending on the hit density per frame. In the 1st stage, the 1152 column

terminations are distributed over 18 banks (see Figure 11) which perform a parallel scan, based on a priority look ahead (PLA) encoding. This allows finding up to N states per bank which result from the encoding of up to 4 contiguous hit pixels (discriminator output set to "1"). This stage handles also the column address encoding and the continuity of the algorithm between the adjacent banks for the entire row. The 2nd stage combines the outcomes of 18 banks of PLA. Its multiplexing logic accepts up to M states per row and adds row and bank addresses. The choice of values for N and M depend on the hit density. The outcome is stored in the 3rd stage, i.e. a memory made of 2 foundry's IP buffers, with a capacity up to 48 Kbits. The 2 buffers allow a continuous readout. While one buffer stores the compressed data of a frame, the other is read out via two LVDS transmitters at a frequency of up to 160 MHz. The memory capacity and the transfer frequency are adapted to each application.

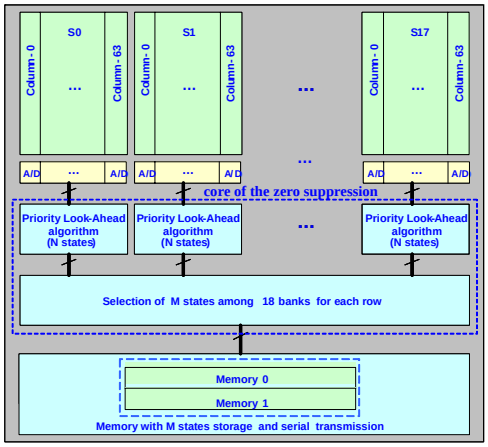


Figure 11: Block diagram of the sensor readout architecture

A reduced scaled prototype, SUZE [12], has been realised to verify the concept above. It incorporates all the logic needed to read out a pixel array for the STAR and EUDET applications. All critical paths of the design were checked in the laboratory. The result shows that the zero suppression circuit decodes correctly column and row addresses of a hit pixel with no information loss. The estimated digital power consumption for the full size logic is about 135 mW.

### *D. General considerations*

For such reticule size chips, one has to focus on design optimisation in order to improve the trade-off between power consumption and speed. For example, the power of the row sequencer (RS) drives metal lines of 2 cm for the control of the pixels. It has to be carefully checked to ensure correct timing with minimum consumption. Due to a 4-metal levels limited process, the RS has been implemented at left hand of the pixel array (~350 µm wide). This creates a dead, but still acceptable, region in the detection zone when the MAPS are abutted in order to encompass a large detection area. The total power for the RS with its clock distribution is about 10 mW, which leads to a total consumption ~140 mW/cm$^2$ for the Ultimate sensor, ~40 % in excess of the STAR final goal. Studies in progress will improve this parameter.

The testability is another point to be considered. Several test points will be implemented in the design all along the data path, i.e. pixels, discriminators, zero suppression circuit and data transmission. These MAPS will be programmable, like previous sensors [6], via a boundary scan controller, for bias supplies and test mode settings.

For the MAPS used for the STAR vertex upgrade, some additional tests like Single Event Upset (SEU) and Single Event Latch-up (SEL), have still to be performed. Some digital circuit layout may have to be redesigned consecutively, especially the memory IP block.

## IV. Conclusion

In this paper, a fast readout architecture of MAPS which integrates on-chip data sparsification has been presented. Its feasibility was verified with two prototypes. The readout speed reaches 10 kframe/s. This architecture seems to be an optimum choice for the chosen process technology. The final MAPS for the EUDET telescope will be sent to fabrication before the end of this year and the ultimate sensors for the STAR upgrade in 2009.

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