Contribution ID: **93** Type: **Oral**

Design and Characterisation of a Fast Architecture Providing Zero Suppressed Digital Output Integrated in a High Resolution CMOS Pixel Sensor for the STAR Vertex Detector and the EUDET Beam Telescope

Tuesday 16 September 2008 11:50 (25 minutes)

CMOS Monolithic Active Pixel Sensors (MAPS) have demonstrated their strong potential for tracking devices, particularly for flavour tagging. They are foreseen to equip several vertex detectors and beam telescopes. Most applications require high read-out speed, requiring sensors featuring digital output with integrated zero suppression. The most recent development of MAPS at IPHC and IRFU addressing this issue will be reviewed. An architecture will be presented, combining a pixel array, column-level discriminators and zero suppression circuits. Each pixel features a preamplifier and a signal processing circuit (CDS) reducing the temporal and fixed pattern noise. The sensor is fully programmable and can be monitored. It will equip experimental apparatus starting data taking in 2009/2010.

Summary

Subatomic physics experiments express a growing need for very high performance flavour tagging, with emphasis on short lived particles (e.g. charmed mesons) poorly accessible through their decay vertex with existing pixel technologies. The trend is therefore to go significantly beyond the tagging performances achieved up to now, relying on a highly granular, thin, radiation tolerant, fast and multi-layer vertex detector installed very close to the beam interaction point.

MAPS are developed since several years in order to fulfil this requirement, based on their intrinsically attractive trade-off between granularity, material budget, radiation tolerance and read-out speed. One of their most specific aspects is that the sensitive volume and the front-end read-out electronics are integrated on the same substrate. Being fabricated in standard CMOS processes available through many commercial microelectronics foundries; they are attractive for their cost effectiveness and the fast multi project run turn over.

MAPS were retained for several applications, ranging from subatomic physics experiments to bio-medical imaging devices. Their first use inside a vertex detector is associated to the upgrade of the STAR experiment at RHIC. MAPS also equip the beam telescope of an EU project, called EUDET, underlying the R&D for the ILC (International Linear Collider) vertex detector. The most recent steps of the development of MAPS for these applications achieved at IPHC-Strasbourg and IRFU-Saclay will be presented.

Numerous application domains require simultaneously high granularity and fast read-out speed. Integrating signal processing functionalities inside the sensor, such as CDS (Correlated Double Sampling), AD converter, data zero suppression circuitry is then facing severe constraints from the pixel dimensions, readout speed and power consumption. The purpose of the contribution is to show a new CMOS MAPS architecture combining on the same substrate a pixel array with 18.4 µm pitch occupying an active area of about 2x2 cm2, column-level discriminators for analogue-to-digital conversion and a zero suppression circuit for data sparsification. Each pixel contains an amplifier and a CDS micro-circuit achieving temporal and fixed pattern noise reduction. The sensor is fully programmable and can be monitored via a JTAG controller.

The development of this architecture is based on 2 separate prototyping lines: one addressing the upstream part of the signal detection and processing chain, and one devoted to data sparsification and formatting. 2 prototype circuits were fabricated in the AMS CMOS 0.35µm technology addressing these two research lines. The sensor exploring the signal sensing and analogue processing features 128 columns of 576 pixels ended with a discriminator. Each pixel contains a pre-amplifier and a CDS circuitry. The sparsification chip incorporates the zero suppression logic and the output memories needed for the EUDET beam telescope and the STAR vertex detector upgrade.

The contribution to the workshop includes a description of the architecture of both chips and an overview of some prominent tests results.

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Session Classification: Parallel session A1 - ASICs