

A prototype ASIC buck converter for LHC upgrades

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Abstract

Given the larger number of channels and the need for reduced material budget in the SLHC trackers, alternatives to the present power distribution scheme have to be explored. In this context we are envisaging a new architecture based on custom switching converters able to work in the high radiation and high magnetic field environment of the experiments. A prototype converter has been designed and integrated in an ASIC. This includes the fundamental building blocks of a buck converter that can be used in later and more complete designs and even in different topologies. Design techniques and functional tests of the prototype will be discussed.

I. INTRODUCTION

In view of a possible upgrade of LHC trackers where the number of channels will increase and the front end (FE) circuits will probably require larger supply current at lower voltage, it is necessary to evaluate alternative power distribution schemes.

A promising approach consists in the distribution of power through a higher voltage bus (up to 12V) to DC-DC converters positioned closed to the FE electronics. These locally convert the bus voltage to the low voltage needed by the FE chips, reducing the current in the bus by a factor close to the voltage conversion ratio, hence decreasing the power lost in the cables.

Commercial components are not targeted to work in the harsh experiment environment characterized by high radiation (more than 100Mrad in total dose) and high magnetic field (up to 4T). It is therefore necessary to develop a custom inductor-based switching converter where tolerance to radiation and magnetic field are specifically addressed.

As proposed in [1], a very attractive power distribution scheme based on DC-DC converters is composed by two different conversion stages. In particular, the first stage converts the 10V from off-detector power supplies to the voltages required for the analog (2.5V) and digital (1.8V) intermediate bus. This paper will present the development of a first prototype of a dc-dc converter for this conversion stage. Design techniques used for the stability of the feedback loop will be presented and layout specificities will be discussed.

II. DC-DC BUCK CONVERTER

The first prototype of the DC-DC converter integrates the basic building blocks of the buck converter that can be used in later and more complete designs and also in different converter topologies. It contains the two power switches and the control circuit. It is designed in a high voltage 0.35 μm CMOS technology usually employed in automotive applications. Radiation tolerance can be achieved with the use of custom-modified layouts. Magnetic tolerance can be achieved using air core inductors that avoid magnetic core saturation, although at the price of introducing constraints in the design of the converter (mostly the switching frequency) [2]. This first prototype was designed for a maximum output current of 2A.

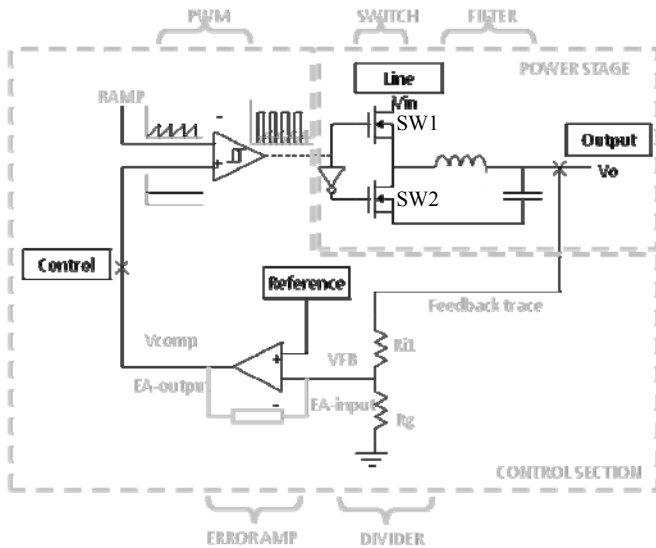
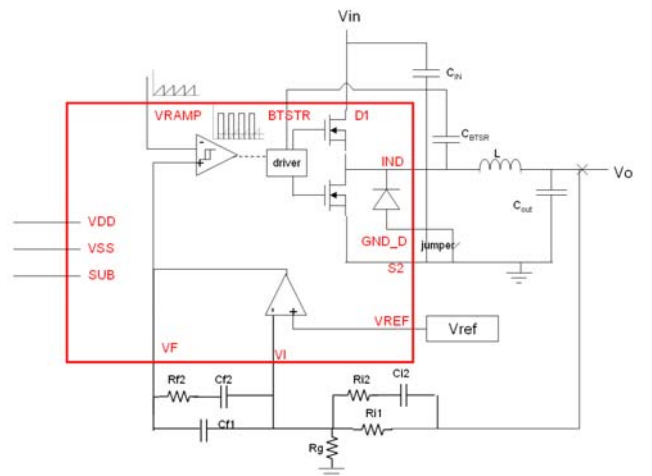


Fig. 1: Main blocks of the step-down DC/DC converter feedback loop



2: First DC-DC converter prototype with integrated control circuit

The converter can be divided into basic building blocks as shown in Fig 1. The power stage contains the two power transistors (SW1 and SW2) and their drivers. The control

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section is composed by a voltage divider, an error amplifier (EA), a comparator, a voltage reference and a ramp generator. The voltage divider shifts the output voltage to a value that is comparable with the reference voltage (usually 1.2V). The EA amplifies the difference between its inputs and this signal is compared to the saw-tooth ramp. This produces at the output of the comparator the duty cycle modulation necessary to drive properly the power transistors.

In this prototype the EA, the comparator and the drivers are integrated, whereas the ramp generator, the voltage reference and some passive components of the control circuit are external. They will be integrated in a later version of the converter. This was done in order to have more freedom for testing purposes, as it enables to vary the switching frequency, the compensation network to stabilize the feedback loop, the input and load voltage and the load current.

Figure 2 summarizes the blocks actually integrated in the prototype described here by encircling them within a red box.

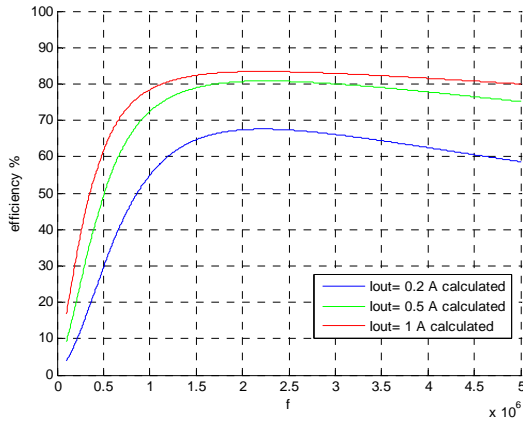


Fig. 3: Efficiency vs frequency and I_{out} . Fixed parameters are $V_{in}=10V$, $V_{out}=2.5V$ and $L=538nH$.

III. DESIGN OF THE CONVERTER

Other than the specifications in terms of input and output voltage and output current, the design of the converter requires that a choice is made in terms of switching frequency and size of the power transistors. The value of these parameters can be chosen to optimise the efficiency that is calculated considering all the conversion losses. These can be classified in different categories: conduction losses (due to the current flowing into the equivalent series resistance (ESR) of the inductor and capacitors and into the on-resistance of the switches), switching losses (due to the simultaneous variation of I_{ds} and V_{ds} during commutation of the power MOS), driving losses (due to the cycling charging and discharging of the switches' capacitances) and losses of the control circuitry. All these losses are strongly technology dependent, therefore a complete parameter extraction of the selected technology was carried out to allow for a meaningful evaluation.

The estimate of all losses can be used to compute the efficiency of the converter for varying frequency and output load, as shown in Fig. 3. It appears that the best compromise is a frequency in the range 1-3MHz.

The design of the converter follows the division of the converter in two main building blocks. The following subsections will explain the design methodology for the power transistors and the control circuit.

A. Power transistors

The power transistors design is one of the crucial parts of the development of the converter. It is necessary to optimize the

dimension to reduce the switching and conductive losses as much as possible. Studies in this direction were already presented [3] together with radiation tolerance results.

As already done for the frequency, it is possible to calculate the efficiency for different dimension of the switches and for different output currents. Fig.4 shows that a good compromise for the different currents is reached for a transistor width close to 0.2m. This leads to an on-resistance of 165mOhm for a gate capacitance of 2nF.

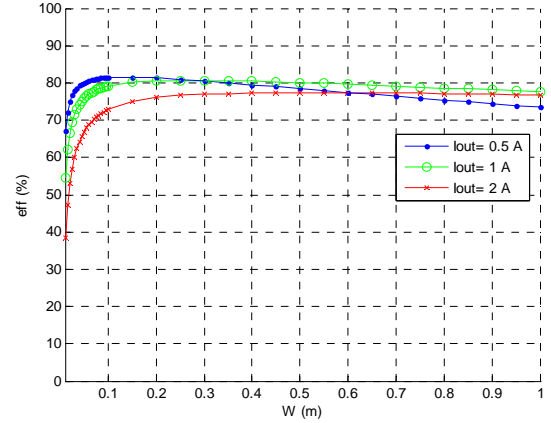


Fig. 4: Efficiency vs transistors width and I_{out} . Fixed parameters are $V_{in}=10V$, $V_{out}=2.5V$ and $L=538nH$.

B. Control circuit

The control section has to be properly studied in order to compensate for the disturbances caused by input line voltage and output load current variations and hence to ensure stability over a wide frequency range (bandwidth of the converter control loop). This means that the control circuit is able to maintain the output voltage stable for disturbances whose frequency is comprised in the bandwidth of the control loop.

We can notice that an increase of this bandwidth improves the stability of the converter, making the fidelity band of the voltage regulator wider. The second advantage, probably most important, of larger bandwidth is the raise of the speed of the voltage regulator to react to and compensate for input line and output load perturbations.

Nevertheless, an upper limit for the control circuit bandwidth is represented by the switching frequency f_s because the feedback loop does not have to be sensitive to the output ripple generated by the converter itself. In reality, such upper limit is rather in the range of $f_s/10$ due to op-amp limited bandwidth (ideally infinitive).

The control circuit design requires a system level model of the converter. The small signal model of the converter is normally used to analyze the variations of the output voltage around the desired steady-state value. This analysis was developed in [4]. The design of the control circuit can be divided in two main tasks: the design of the ASIC blocks (error amplifier, comparator, level shifter and bootstrap) and the choice of the external compensation network components. They will now be shortly expanded.

1) Error amplifier

The error amplifier (EA) circuit is a key point in the design of the control loop because its realization can produce considerable shifts on the transfer function. It is necessary to design the EA with a bandwidth larger than the one desired for the full control loop, otherwise this last will be reduced. Moreover, the gain has to be very high (at least 70dB) to

avoid errors on the value of the output dc voltage [3]. In this design the EA is implemented with a Miller amplifier with a DC gain of 80dB and a bandwidth of 15Mhz. The power dissipated by this element is around 6mW.

2) Comparator

The comparator generates the PWM modulation from the output of the EA and the sawtooth ramp. The latter has very high frequency components, hence the comparator needs to have a very large bandwidth to avoid distortions of the output signal possibly affecting the width of the PWM modulation. The comparator was implemented as a 3 cascaded stages amplifier with a bandwidth of 100Mhz and a dc gain of 50dB.

3) Non overlapping driver

The signal provided by the comparator is used to generate the drive signal of the two power switches. It is necessary to avoid any overlap of the two gate control signals to prevent shoot-through between the input node and ground at every cycle which could damage or at least drastically affect the efficiency of the converter. The correct timing of the two gate signals is depicted in Fig.5.

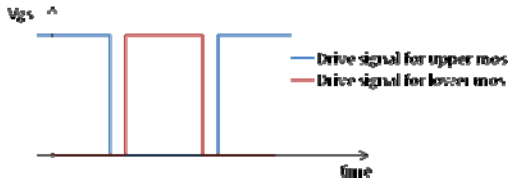


Figure 5: example of non overlapping gate signals

4) Level shifter and bootstrap circuit

The driving of the SW1 is difficult because the source of this transistor is connected to the output node, which is cyclically connected to V_{in} or ground. A special circuit is needed to shift the signal referred to ground (generated by the non overlapping driver) and refer it to the source potential. This can be done by a level shifter in combination with a bootstrap circuit. Basically the circuit maintains a capacitance (called bootstrap capacitor) charged to 3.3 V and it connects this capacitance between source and gate of the power MOS to switch it on. To switch it off the level shifter circuit connects the gate to the source.

5) Driver of the power transistor

The driving circuit needs to be able to switch on and off the transistor in few nanoseconds; therefore the drivers were carefully sized to cope with this requirement.

6) External compensation network

The compensation network is necessary to increase the bandwidth of the control loop and its DC gain. Three different compensation networks are available; they have been explained in [4].

For this development a type 3 compensation network is used in order to achieve a crossover frequency of 200Khz with a phase margin of 70°. The value of these passive components can be found using the equations given in [4].

IV. CIRCUIT LAYOUT

The design of the layout must take into account different issues. First of all the NMOS transistors have to be custom modified to increase their radiation tolerance. Low-voltage NMOS transistors in the control circuit are modified with standard ELT techniques [5][6][7] whilst high-voltage transistors require a slightly modified enclosed topology.

Given the large current flowing (up to 4 A) in the power transistors their layout was studied to minimize the resistance between input and output terminals. The layout was also optimized to maintain low gate resistance to achieve short propagation delay of the gate signals.

Multiple unit cells have been used for the design of these large transistors. This allows a more uniform distribution of the current over the different cells, hence a more efficient use of each cell. It also has the benefit that many more drain contacts are available, which improves the possibilities for routing and help increasing the yield of the circuit. The choice of the dimensions of the unit cell is driven by the necessity to compromise the occupied area and the time propagation of the gate signal. With this technology the resistance of the polysilicon and the gate capacitance set the maximum dimensions of the width of each transistors finger at 50 μm in order to have a gate rise-fall time below about 2ns (simulation). The optimum choice of 8 fingers for the unit cell, each with $W=50 \mu\text{m}$, yields a W of 400 μm . The 0.2 m width transistor is hence composed of 512 unit cells.

The external pad needs to be placed in order to decrease parasitic capacitance, resistance and inductance and to simplify the PCB design.

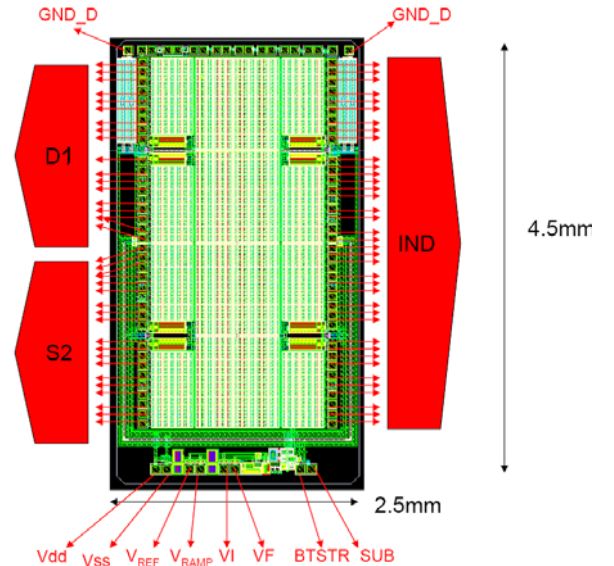


Figure 6: layout of the DC-DC prototype

The power transistors switch very fast and the speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit and lead to device over-voltage stress. To partially decrease the injection of these spikes to ground a decoupling capacitor can be placed on PCB really close to the ASIC. To facilitate this placement in the layout D1 (connected to V_{in}) of SW1 (Fig.2 and Fig.6) is placed close to the source S2 of the SW2 which is connected to ground.

Techniques to reduce coupling to substrate noise were adopted. Such noise is mainly due to the use of vertical high-voltage transistors whose drain is a buried layer physically close to the substrate. Since the drain potential moves from input voltage (10V) to ground, capacitive coupled noise is injected into the substrate and can disturb the control logic circuits. In order to avoid noise injection the available triple well option was used. As an additional precaution, all the control circuitry is positioned far from the switching transistor (on the bottom in Figure 4.)

V. PCB DESIGN

The PCB was developed, produced and mounted in RWTH, Aachen.



Figure 7 : image of the PCB containing the ASIC prototype

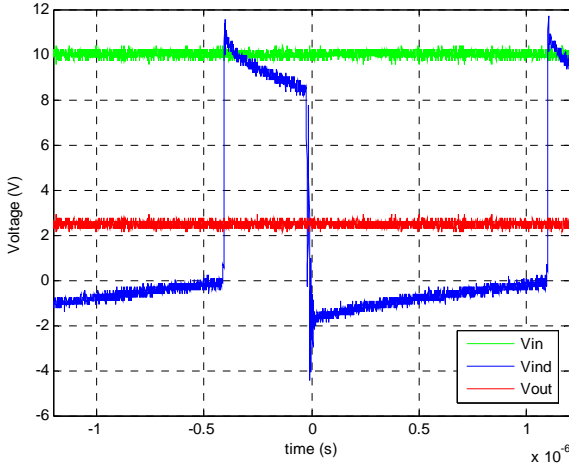


Figure 8: waveforms of the most important converter nodes

The PCB is depicted in Fig. 7. Inside the red circle the ASIC is bonded directly on PCB and covered by a globetop layer. High-frequency decoupling ceramic capacitors are located as close as practicable to their decoupling target (for example the input and output line), making use of the shortest connection paths to reduce inductive loops. It is mandatory to locate the components associated with the feedback circuit close to their respective controller pins, since they belong to a high-impedance circuit loop, sensitive to EMI pick-up. The area of node IND (Fig.2 and Fig.6) was kept as low as possible to decrease the capacitive coupling to the ground plane.

VI. MEASUREMENT ON THE PROTOTYPE

The prototype converter was manufactured and measured to verify its performance in terms of efficiency and noise emission. Fig.8 shows an example waveform, measured with an oscilloscope, of the input and output voltage and the voltage at the inductor node. The measured output ripple is 30mVpp.

A. Efficiency measurements

Fig.9 and Fig.10 show the calculated (lines) and measured (dots) efficiency of the buck converter for different loads at room temperature. In Fig.10 the efficiency is also shown when the converter is cooled with CO₂ ice. The measured efficiency is obtained by the output/input power ratio.

For Vin=5V (Fig. 9) the simulated and measured efficiencies are similar for frequencies up to 600Khz. For higher frequencies the measured efficiency drops. The same behaviour but with a higher drop can be appreciated in Fig 10 where Vin=10V. At 1Mhz and Iout=1A the measured efficiency is around 10% lower than the estimate.

Our hypothesis concerning the origin of this discrepancy is not yet fully confirmed. We suspect an overlap in the signals driving the gate of the two switches, because of which a large current (proportional to $V_{in}/(R_{onSW1}+R_{onSW2})$) flows to ground for few nanosecond at each cycle, leading to an additional loss. In this case the efficiency should be inversely proportional to V_{in} and f_{sw} , in agreement with our observations. Further measurements will be carried on to verify this hypothesis.

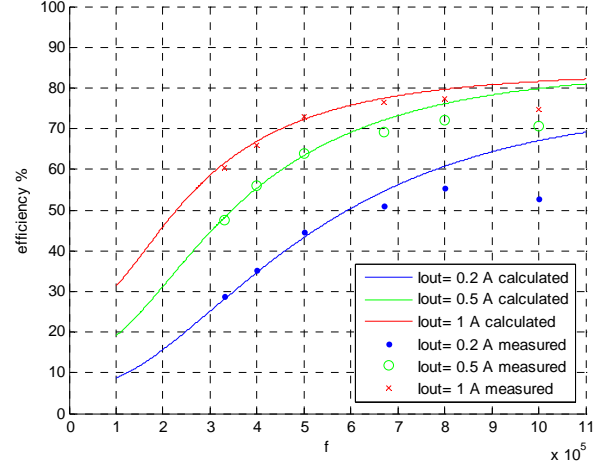


Figure 9: Efficiency vs frequency with Vin=5V, Vout=2.5V and L=538nH

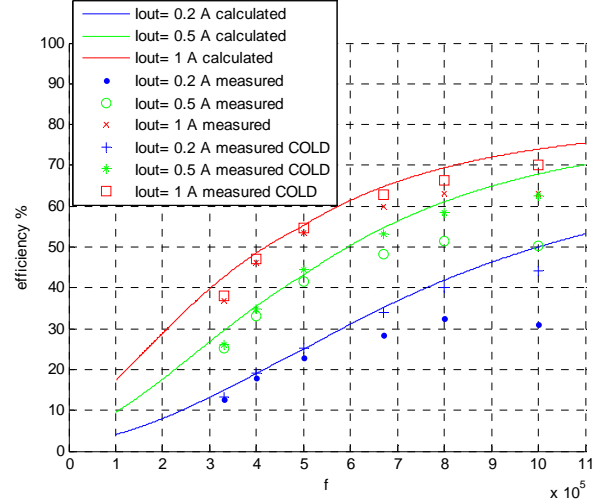


Figure 10: Efficiency vs frequency with Vin=10V, Vout=2.5V and L=538nH

It should be pointed out that in the absence of specific cooling the temperature of the converter in our tests is much higher than 27°C, since the converter is dissipating a large amount of power (up to 1W).

If a cooling system is used, at lower temperature the resistance of the power transistors and of their driver decreases, leading respectively to lower conduction losses and faster switching time. This could possibly reduce the overlap of the gate signals, effectively decreasing losses.

To see the effect of lower temperature the PCB was cooled down by forming CO₂ ice on its back side. The measured efficiencies in such condition are labelled “cold” in Fig.9. It is possible to appreciate the sensitive increase in efficiency.

B. Noise Measurements

Output common mode noise measurements were carried out at CERN on the reference test bench of the ESE group [8], [9]. Fig.11 and Fig.12 show the output common mode noise current in dBuA vs the frequency for an output voltage of 2.5 V, a load current of 1A and a switching frequency of 1Mhz.

The input voltage is set at 5V for Fig. 11 and 10V for Fig.12.

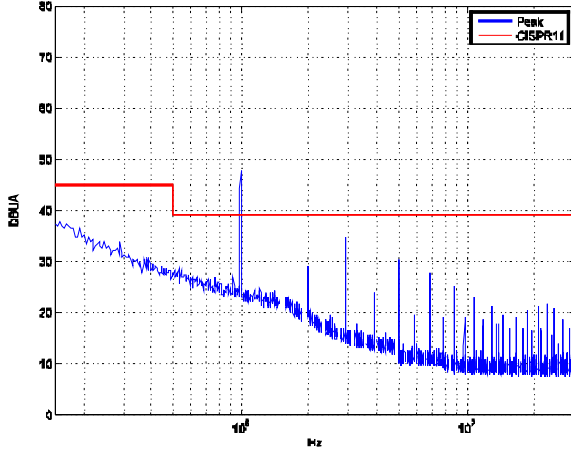


Figure 11: common mode noise current vs frequency with $V_{in}=5V$, $V_{out}=2.5V$ and $L=538nH$

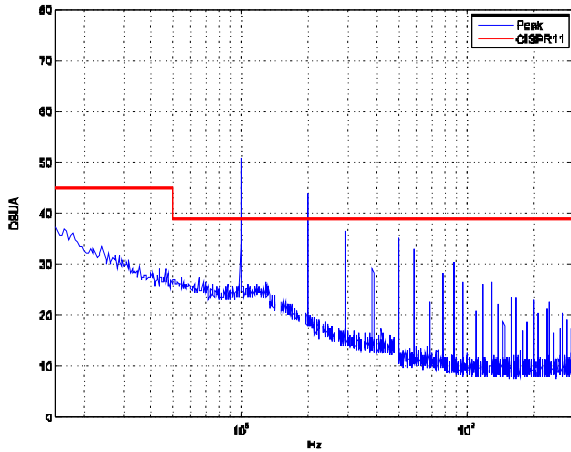


Figure 12: common mode noise current vs frequency with $V_{in}=10V$, $V_{out}=2.5V$ and $L=538nH$

The highest peak coincides with the switching frequency and all the other harmonics are present. The red line represents the limit of the CISPR Standards [6]. This can help to fix a limit and compare the results when converters parameters are changed. When the ratio V_{out}/V_{in} is close to 0.5 the duty cycle tends to 50% and we can see a decrease of the even harmonics (Fig. 11). This can be explained through the study of the FFT of a square wave. If the duty cycle is 50% we have complete cancellation of the even harmonics. Compared to other prototypes with commercial components these noise performances are promising for a first prototype. This prototype was used to power two different silicon strip front-end modules [10][11], in one of the cases without penalties to the noise performance.

VII. CONCLUSIONS

In view of a new power distribution scheme in the SLHC detectors, we have shown how to integrate a simple DC-DC stepdown converter that copes with the magnetic field requirements of the SLHC environment. The main building blocks of this first prototype, in particular the control circuit whose performance is very satisfactory, will be used in more mature versions of the converter, and are usable also in different converter topologies. Measurements of common mode noise are also encouraging, since the performance is

comparable with the one measured for commercial components.

The origin of the lower efficiency measured with respect to our estimate has to be investigated further to confirm our hypothesis on gate signals overlap, and shall be eliminated in further prototypes. Radiation tests are also foreseen, although the available radiation data on the used technology indicate that our objectives in terms of radiation tolerance can not be met by the power switches used in this design.

Work has started in view of the integration of the sawtooth generator, the reference voltage and the compensation network on-chip in the next prototyping cycle.

VIII. ACKNOWLEDGEMENTS

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