



A prototype ASIC buck converter for LHC upgrades

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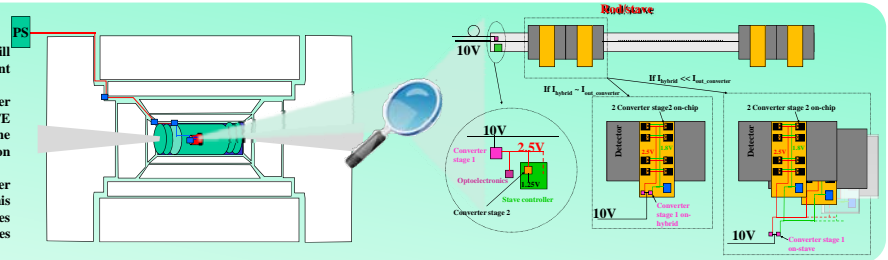


Abstract

Given the larger number of channels and the need for reduced material budget in the SLHC trackers, alternatives to the present power distribution scheme have to be explored. In this context we are envisaging a new architecture based on custom switching converters able to work in the high radiation and high magnetic field environment of the experiments. A prototype of the converter has been designed and integrated in an ASIC. This includes the fundamental building blocks of a buck converter that can be used in later and more complete designs and even in different topologies. Design techniques, functional and radiation tests of the prototype will be discussed.

INTRODUCTION

In view of a possible upgrade of LHC tracker where the number of channels will increase and the front end (FE) circuits will probably require larger supply current at lower voltage, it is necessary to evaluate alternative power distribution scheme. A promising approach consists in the distribution of power through a higher voltage bus (up to 24V) to DC-DC converters positioned close to the FE electronics. These locally convert the bus voltage to the low voltage needed by the FE, reducing the current in the bus by a factor close to the voltage conversion ratio, hence decreasing the power lost in the cables. In this context we are developing a custom inductor-based switching converter where tolerance to radiation and magnetic field are specifically addressed. In this paper a first prototype of this dc-dc converter will be shown. Design techniques used for the stability of the feedback loop will be presented and layout specificities will be discussed.

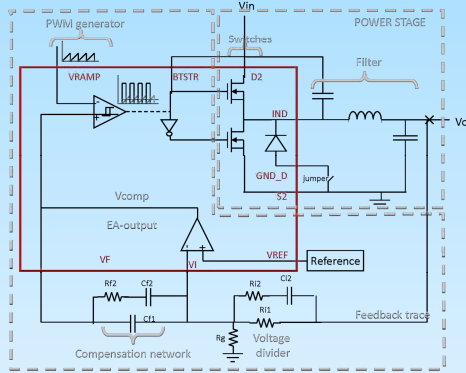


DC/DC BUCK ARCHITECTURE

The first prototype of the DC-DC converter integrates the basic building blocks of the buck converter that can be used in later and more complete designs and in different converter topologies.

Features

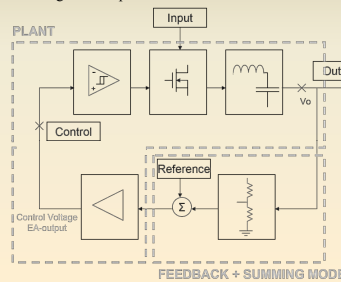
- designed in a high voltage 0.35 μm CMOS technology.
- Radiation tolerance up to 200Mrad
- High Magnetic field tolerance
- VIN and Power Rail Operation from +3.3V to +24V
- 14MHz Bandwidth Error Amplifier with 10V/ μs Slew Rate
- External oscillator Programmable from 250kHz to 1MHz
- External voltage reference (nominally 1.2V)
- Remote Voltage Sensing with Unity Gain
- Output current up to 1.5A and output voltage range from 1.25 to Vin



Main building blocks of a buck DC-Dc converter with voltage regulation

FEEDBACK LOOP ANALYSIS

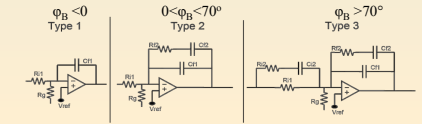
The action of the feedback control is to regulate the output voltage through the duty cycle in order to compensate for the disturbances caused by input line voltage and output load current variations. The small signal model of the converter is used, (needs to pay attention on validity region)



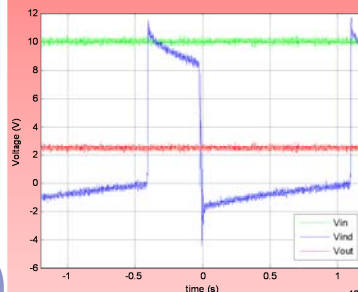
The open and closed loop transfer function need to be calculated. Phase and gain margins are figure of merit of linear dynamic system stability calculation

A compensation network can be set around the error amplifier to improve stability at higher frequency.

Three type of compensation network can be used depending on the wanted phase boost ϕ_B



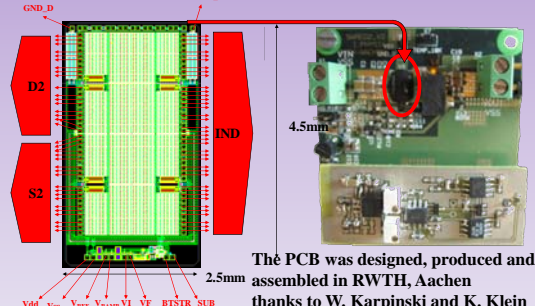
WAVEFORMS



Measurements of the waveform were improved with the oscilloscope. This figure shows the waveform of the input and output voltage and the voltage at the inductor node. The measured output ripple is 30mVpp.

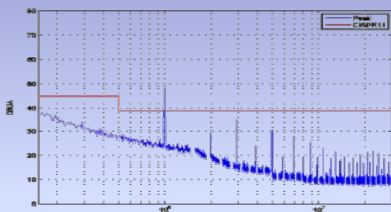
DESIGN OF ASIC AND PCB

The ASIC contains the two power transistors with the control circuit and the drivers. Each power transistor has an on resistance of 165mOhm and a gate capacitance of 2nF. The total area is around 11mm². The position of the bonding pad is studied to reduce the resistance and to facilitate the integration on PCB.

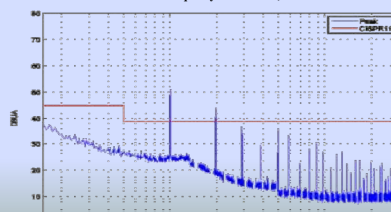


NOISE MEASUREMENT

Output common mode noise measurements were carried out at CERN on the testbench of ESE group. The red line figure is the limits of the CISPR Standards. The highest peak coincides with the switching frequency and all the other harmonics are present. This can be explained through the study of the FFT of a square wave. If the duty cycle is of the 50% we have complete cancellation of the even harmonics.



Common mode noise current vs frequency with Vin=5V, Vout=2.5V and L=538nH



Common mode noise current vs frequency with Vin=10V, Vout=2.5V and L=538nH

EFFICIENCY RESULTS

The following plots show the comparison between calculated and tested efficiency. It is possible to appreciate that for Vin=5V the simulated and measured efficiency are really closed in particular for load of 0.5 A and 1A. In the case of Vin=10V there is some difference between the measurement and the simulation for all the loads. Studies are ongoing to understand the source of this difference. First analysis shows that the efficiency is strongly dependent to temperature. All the data shown here are taken with the converter under cooling, otherwise the efficiency will drop dramatically.

