FPGA MEZZANINE UPGRADE

Xilinx Virtex FPGA Families

<table>
<thead>
<tr>
<th>Xilinx Family</th>
<th>Virtex</th>
<th>Virtex-E</th>
<th>Virtex-2</th>
<th>Virtex-4</th>
<th>Virtex-5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Year</td>
<td>1999</td>
<td>2000</td>
<td>2001</td>
<td>2004</td>
<td>2006</td>
</tr>
<tr>
<td>Technology</td>
<td>220 nm</td>
<td>180 nm</td>
<td>130 nm</td>
<td>90 nm</td>
<td>65 nm</td>
</tr>
<tr>
<td>Core power</td>
<td>2.5V</td>
<td>1.8V</td>
<td>1.5V</td>
<td>1.2V</td>
<td>1.0V</td>
</tr>
</tbody>
</table>

Advantages of Virtex-5:
- Higher performance due to 65nm technology
- More flexible basic slice (4 LUT + 4 Flip-flops)
- Better clocking routing
- More embedded memory
- Four sub-families:
  - General purpose LX
  - Serial connection oriented LXT
  - Signal processing oriented SXT
  - Embedded applications oriented FXT
- Potential ability to self-correct single event errors and detect double errors using the Internal Configuration Access Port

Disadvantages:
- Less user input/output pins available for similar packages (compare with Virtex-2)

<table>
<thead>
<tr>
<th>Package</th>
<th>User i/o, Virtex-2 XC2V1500/2000/3000</th>
<th>User i/o, Virtex-5 XC5VLX30/50/85/110</th>
<th>User i/o, Virtex-2 XC2V4000/6000/8000</th>
<th>User i/o, Virtex-5 XC5VLX50/85/110</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>27 x 27 mm FG676/FF676</td>
<td>35 x 35 mm FF1152/FF1153</td>
<td>824/824/824</td>
<td>560/560/800</td>
</tr>
</tbody>
</table>

Conclusion:
- ~50% performance sorting "4",
- Sorting "4" the fastest
- Pin compatible solution (low cost)

MEZZANINE GIGABIT LINK